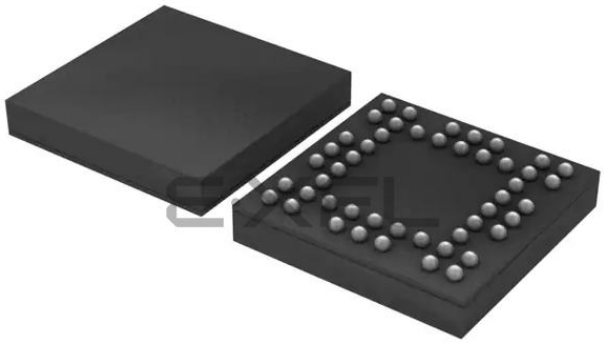

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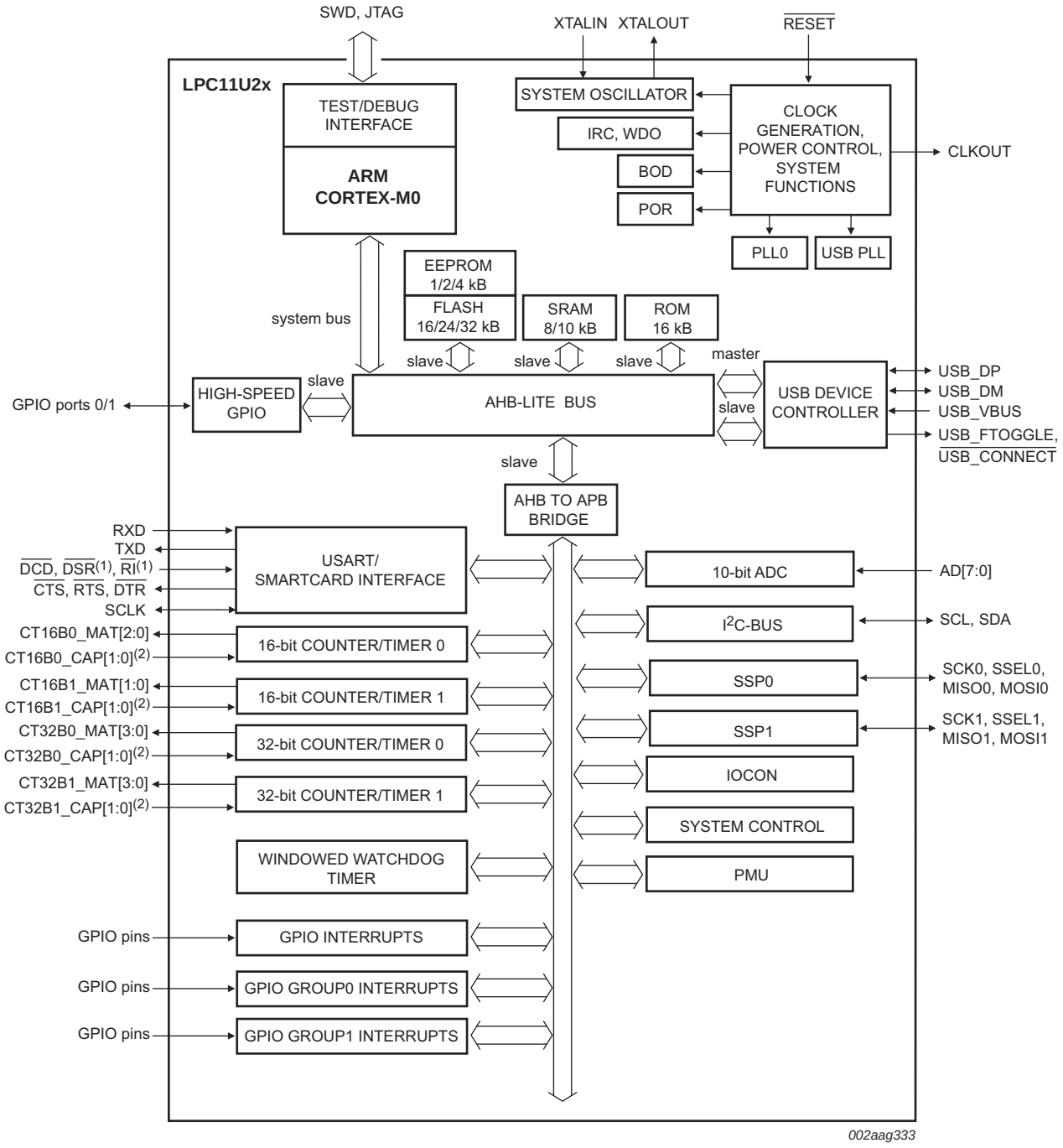
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFBGA
Supplier Device Package	48-TFBGA (4.5x4.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u24fet48-301

5. Block diagram



(1) Not available on HVQFN33 packages.

(2) CT32B1_CAP1 available on TFBGA48/LQFP64 packages only. CT16B0_CAP1 and CT16B1_CAP1 available on LQFP64 packages only. CT32B0_CAP1 available on LQFP48/TFBGA48/LQFP64 packages only.

Fig 1. Block diagram

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_5/SDA	11	H3	16	21 [4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/$\overline{\text{USB\_CONNECT}}$/SCK0	15	H6	22	29 [3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	16	G7	23	30 [5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
PIO0_8/MISO0/CT16B0_MAT0	17	F8	27	36 [3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/CT16B0_MAT1	18	F7	28	37 [3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/CT16B0_MAT2	19	E7	29	38 [3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/CT32B0_MAT3	21	D8	32	42 [6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/CT32B1_CAP0	22	C7	33	44 [6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
					-	I/O	**PIO_12 —** General purpose digital input/output pin.
					-	I	**AD1 —** A/D converter, input 1.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/CT32B1_MAT0	23	C8	34	45 [6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
					-	I/O	**PIO0_13 —** General purpose digital input/output pin.
					-	I	**AD2 —** A/D converter, input 2.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	B7	35	46 [6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
					-	I/O	**PIO0_14 —** General purpose digital input/output pin.
					-	I	**AD3 —** A/D converter, input 3.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	B6	39	52 [6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
					-	I/O	**PIO0_15 —** General purpose digital input/output pin.
					-	I	**AD4 —** A/D converter, input 4.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	26	A6	40	53 [6]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin. In Deep power-down mode, this pin functions as the WAKEUP pin with 20 ns glitch filter. Pull this pin HIGH externally to enter Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
					-	I	**AD5 —** A/D converter, input 5.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	A3	45	60 [3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	B3	46	61 [3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
					-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	B2	47	62 [3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
					-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	F2	9	11 [3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	G4	17	22 [3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	E8	30	40 [6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
					-	I	**AD6 —** A/D converter, input 6.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	23 [3]	I; PU	I/O	**PIO1_17 —** General purpose digital input/output pin.
					-	I	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	28 [3]	I; PU	I/O	**PIO1_18 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					-	O	**TXD —** Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	1	B1	2	3 [3]	I; PU	I/O	**PIO1_19 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	-	H1	13	18 [3]	I; PU	I/O	**PIO1_20 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	-	G8	26	35 [3]	I; PU	I/O	**PIO1_21 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	-	A7	38	51 [3]	I; PU	I/O	**PIO1_22 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	-	H4	18	24 [3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	G6	21	27 [3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	A1	1	2 [3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	-	G2	11	14 [3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	-	G1	12	15 [3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	-	H7	24	31 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	D7	31	41 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.

7.12.1 Features

- The I^2C-interface is an I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC11U2x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 General purpose external event counter/timers

The LPC11U2x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.

- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.15 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.16 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

7.16.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

7.17.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U2x, use the system oscillator to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.17.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.17.2 System PLL and USB PLL

The LPC11U2x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.17.3 Clock output

The LPC11U2x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.17.4 Wake-up process

The LPC11U2x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

7.17.5 Power control

The LPC11U2x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.17.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin. The LPC11U2x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11U2x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

7.17.6 System control

7.17.6.1 Reset

Reset has four sources on the LPC11U2x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

7.17.6.2 Brownout detection

The LPC11U2x includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.17.6.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11Uxx user manual*.

There are three levels of Code Read Protection:

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Pin capacitance						
C_{io}	input/output capacitance	pins configured for analog function	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	-	-	2.5	pF
		pins configured as GPIO	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ V_{DD} ≤ 3.6 V. Guaranteed by design.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[5] BOD disabled.

[6] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the SYSCON block.

[7] USB_DP and USB_DM pulled LOW externally.

[8] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

[11] Including voltage on outputs in 3-state mode.

[12] V_{DD} supply voltage must be present.

[13] 3-state outputs go into 3-state mode in Deep power-down mode.

[14] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[15] To V_{SS}.

[16] Includes external resistors of 33 Ω ± 1 % on USB_DP and USB_DM.

Table 6. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	±1.5	LSB
E_O	offset error	[4]	-	-	±3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

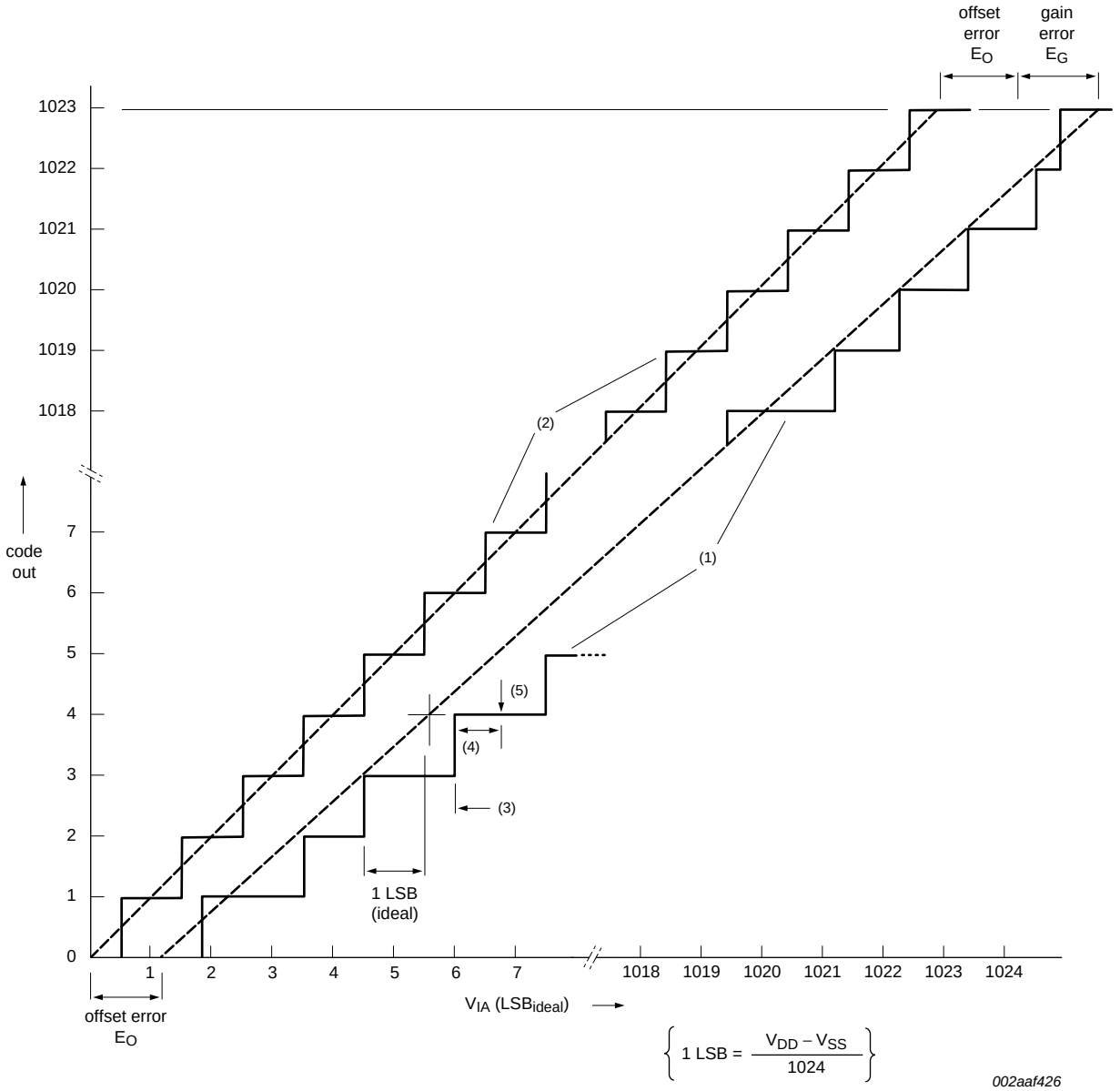
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

Table 8. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.
USB	-	-	1.2	-

10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11Uxx user manual.*

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][7][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

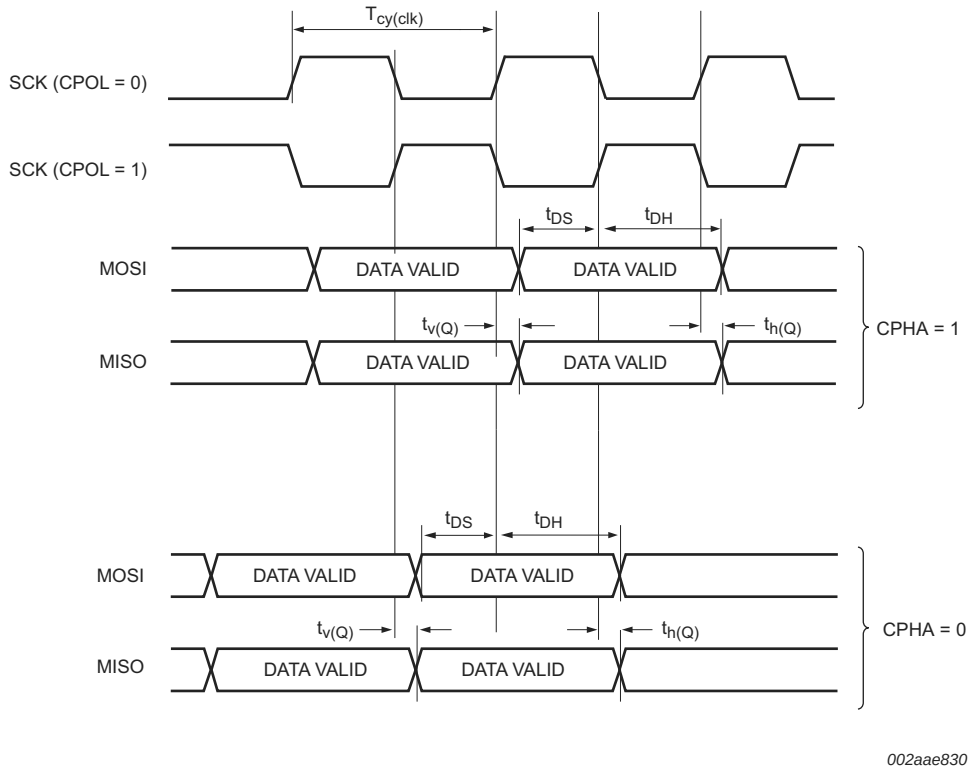


Fig 25. SSP slave timing in SPI mode

10.7 USB interface

Table 17. Dynamic characteristics: USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	8.5	-	13.8	ns
t_f	fall time	10 % to 90 %	7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	109	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 26	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 26	−2	-	+5	ns
t_{JR1}	receiver jitter to next transition		−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	−9	-	+9	ns
t_{EOPR}	EOP width at receiver	must accept as EOP; see Figure 26 [1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

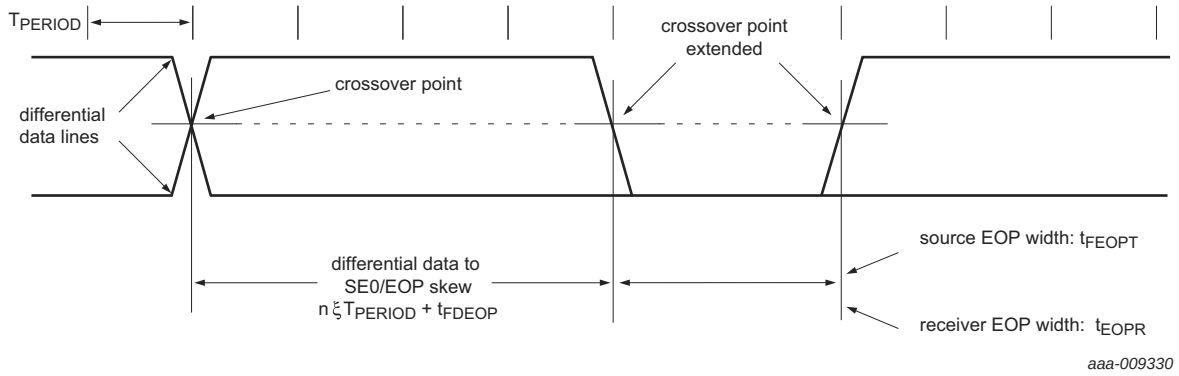


Fig 26. Differential data-to-EOP transition skew and EOP width

11. Application information

11.1 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 27) or bus-powered device (see Figure 28).

On the LPC11U2x, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

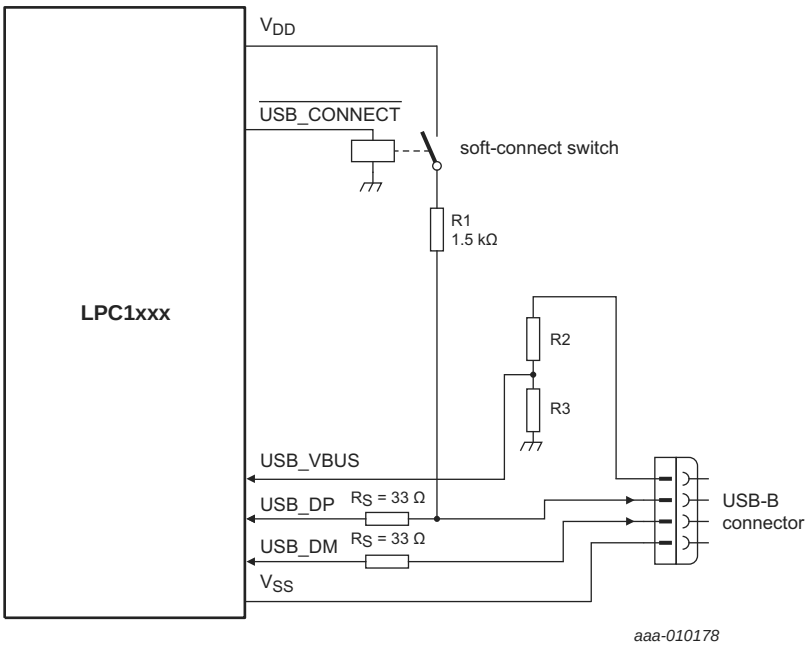


Fig 27. USB interface on a self-powered device where USB_VBUS = 5 V

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 28). The USB_CONNECT function can additionally be connected as shown in Figure 27 to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic.

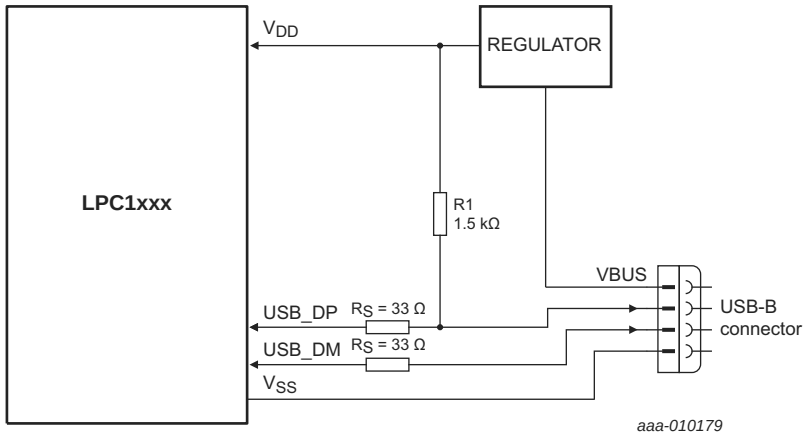


Fig 28. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 28 is used, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block to ensure that the USB_CONNECT signal can still be controlled by software. For details on the soft-connect feature, see the *LPC11U2x user manual* (Ref. 1).

Remark: When a self-powered circuit is used without connecting VBUS, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) and provide software that can detect the host presence through some other mechanism before enabling USB_CONNECT and the soft-connect feature. Enabling the soft-connect without host presence will lead to USB compliance failure.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

11.4 Standard I/O pad configuration

Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

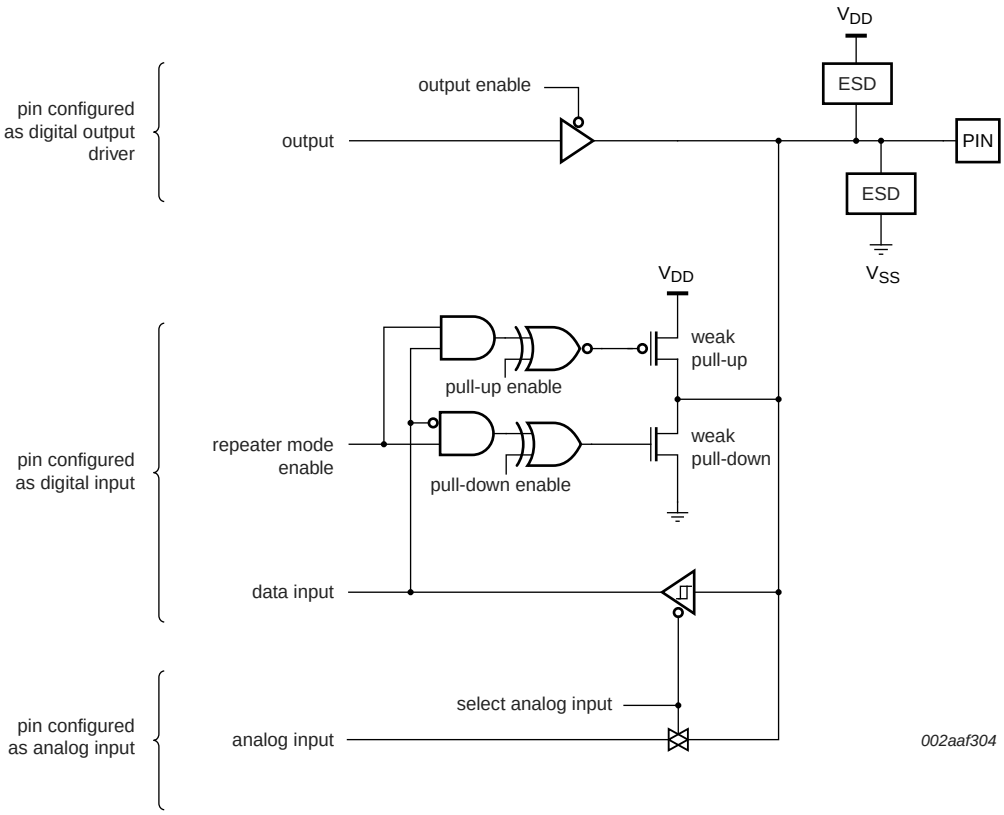
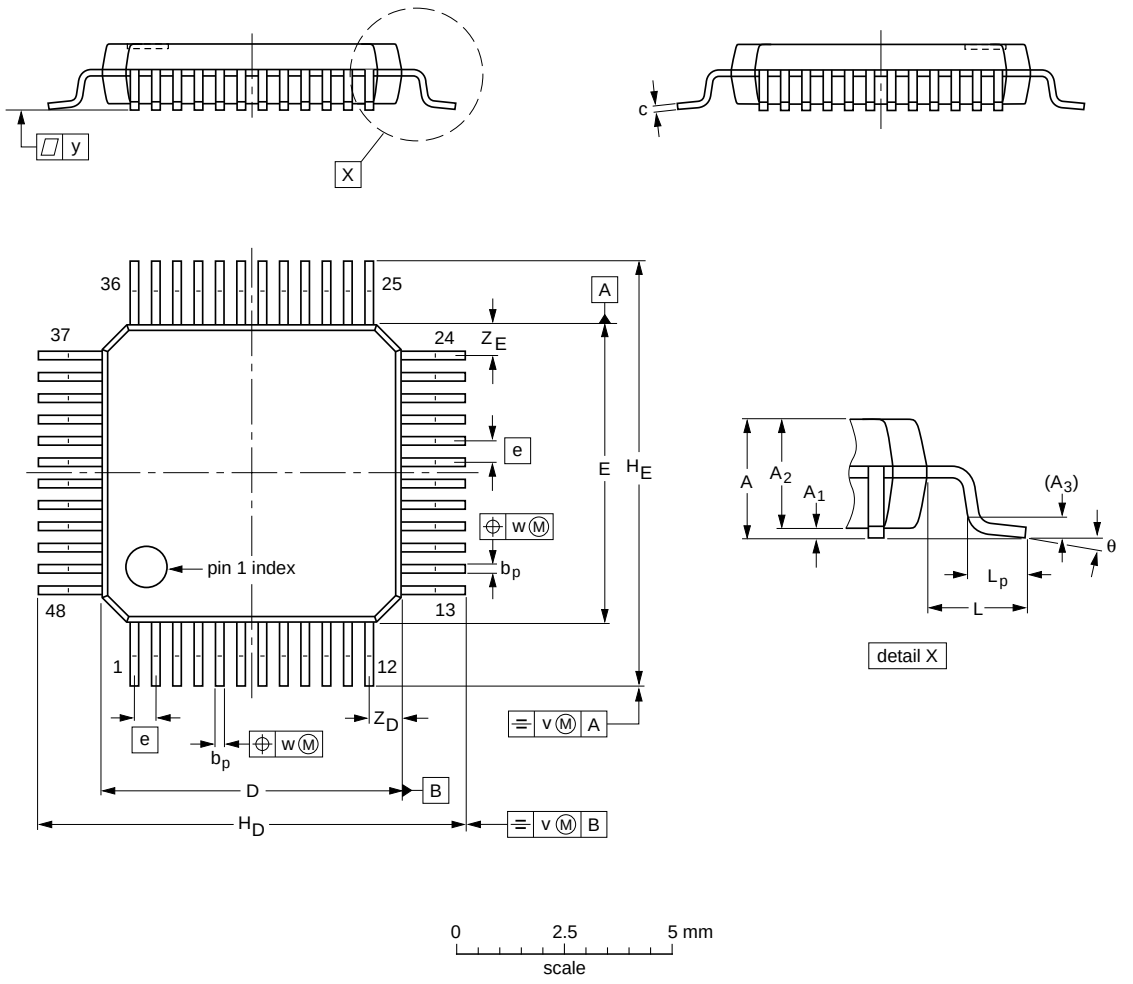


Fig 31. Standard I/O pad configuration

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 36. Package outline LQFP48 (SOT313-2)