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Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	95
Number of Gates	14000
Voltage - Supply	3V ~ 3.6V, 4.5V ~ 5.5V
Mounting Type	-
Operating Temperature	-55°C ~ 125°C (TC)
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a42mx09-pg132m

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Power Matters.*

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies
 only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

1.3 **Revision 13.0**

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This
 marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

1.6 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

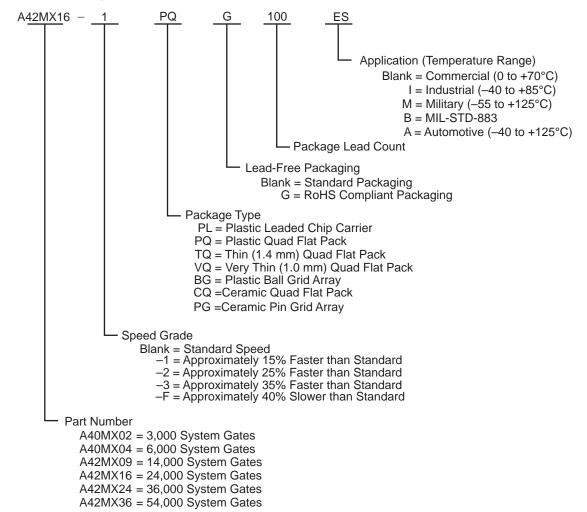
- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)



2.3 Ordering Information

The following figure shows ordering information. All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

Figure 1 • Ordering Information





3.3.7 Low Power Mode

42MX devices have been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when exiting Low Power Mode. I/Os can be driven during LP mode, and clock pins should be driven HIGH or LOW and should not float to avoid drawing current. To exit LP mode, the LP pin must be pulled LOW for over 200 µs to allow for charge pumps to power up, and device initialization will begin.

3.4 Power Dissipation

The general power consumption of MX devices is made up of static and dynamic power and can be expressed with the following equation.

3.4.1 General Power Equation

P = [ICCstandby + ICCactive]*VCCI + IOL*VOL*N + IOH*(VCCI - VOH)*M

EQ 1

where:

- ICCstandby is the current flowing when no inputs or outputs are changing.
- ICCactive is the current flowing due to CMOS switching.
- IOL, IOH are TTL sink/source currents.
- VOL, VOH are TTL level output voltages.
- N equals the number of outputs driving TTL loads to VOL.
- M equals the number of outputs driving TTL loads to VOH.

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

3.4.2 Static Power Component

The static power due to standby current is typically a small component of the overall power consumption. Standby power is calculated for commercial, worst-case conditions. The static power dissipation by TTL loads depends on the number of outputs driving, and on the DC load current. For instance, a 32-bit bus sinking 4mA at 0.33V will generate 42mW with all outputs driving LOW, and 140mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

3.4.3 Active Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. Dynamic power consumption is frequency-dependent and is a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitances due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by the equation:

Power(
$$\mu$$
W) = C_{EO}^* VCCA2* F(1)

EQ 2

where:

C_{EQ} = Equivalent capacitance expressed in picofarads (pF)



Figure 13 • Silicon Explorer II Setup with 42MX

Serial Connection to Windows PC

Silicon Explorer II

Span

Table 8 • Device Configuration Options for Probe Capability

Security Fuse(s) Programmed	Mode	PRA, PRB ¹	SDI, SDO, DCLK ¹
No	LOW	User I/Os ²	User I/Os ²
No	HIGH	Probe Circuit Outputs	Probe Circuit Inputs
Yes	_	Probe Circuit Secured	Probe Circuit Secured

^{1.} Avoid using SDI, SDO, DCLK, PRA and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

3.4.7 Design Consideration

It is recommended to use a series 70Ω termination resistor on every probe connector (SDI, SDO, MODE, DCLK, PRA and PRB). The $70~\Omega$ series termination is used to prevent data transmission corruption during probing and reading back the checksum.

3.4.8 IEEE Standard 1149.1 Boundary Scan Test (BST) Circuitry

42MX24 and 42MX36 devices are compatible with IEEE Standard 1149.1 (informally known as Joint Testing Action Group Standard or JTAG), which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic MX boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers and instruction register (Figure 14, page 18). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and some optional instructions. Table 9, page 18 describes the ports that control JTAG testing, while Table 10, page 18 describes the test instructions supported by these MX devices.

Each test section is accessed through the TAP, which has four associated pins: TCK (test clock input), TDI and TDO (test data input and output), and TMS (test mode selector).

The TAP controller is a four-bit state machine. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles.

42MX24 and 42MX36 devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

^{2.} If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. See the Pin Descriptions, page 83 for information on unused I/O pins



A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$MaximumPowerAllowed = \frac{Max \cdot junction \ temp \cdot (^{\circ}C) - Max \cdot ambient \ temp \cdot (^{\circ}C)}{\theta_{ja}(^{\circ}(C/W))} = \frac{150^{\circ}C - 70^{\circ}C}{(28^{\circ}C)/W} = 2.86W$$

EQ 5

The maximum power dissipation for military-grade devices is a function of θ_{jc} . A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$MaximumPowerAllowed = \frac{Max \cdot junction \ temp \cdot (^{\circ}C) - Max \cdot ambient \ temp \cdot (^{\circ}C)}{\theta_{jc}(^{\circ}(C/W))} = \frac{150^{\circ}C - 125^{\circ}C}{(6.3^{\circ}C)/W} = 3.97W$$

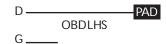
EQ 6

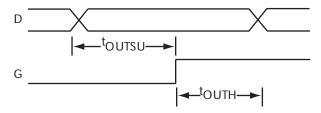
Table 27 • Package Thermal Characteristics

			θ_{ja}			
Plastic Packages	Pin Count	$\theta_{ extsf{jc}}$	Still Air	1.0 m/s 200 ft/min.	2.5 m/s 500 ft/min.	Units
Plastic Quad Flat Pack	100	12.0	27.8	23.4	21.2	°C/W
Plastic Quad Flat Pack	144	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	160	10.0	26.2	22.8	21.1	°C/W
Plastic Quad Flat Pack	208	8.0	26.1	22.5	20.8	°C/W
Plastic Quad Flat Pack	240	8.5	25.6	22.3	20.8	°C/W
Plastic Leaded Chip Carrier	44	16.0	20.0	24.5	22.0	°C/W
Plastic Leaded Chip Carrier	68	13.0	25.0	21.0	19.4	°C/W
Plastic Leaded Chip Carrier	84	12.0	22.5	18.9	17.6	°C/W
Thin Plastic Quad Flat Pack	176	11.0	24.7	19.9	18.0	°C/W
Very Thin Plastic Quad Flat Pack	80	12.0	38.2	31.9	29.4	°C/W
Very Thin Plastic Quad Flat Pack	100	10.0	35.3	29.4	27.1	°C/W
Plastic Ball Grid Array	272	3.0	18.3	14.9	13.9	°C/W
Ceramic Packages						
Ceramic Pin Grid Array	132	4.8	25.0	20.6	18.7	°C/W
Ceramic Quad Flat Pack	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack	256	2.0	20.0	16.5	15.0	°C/W



Figure 27 • Output Buffer Latches

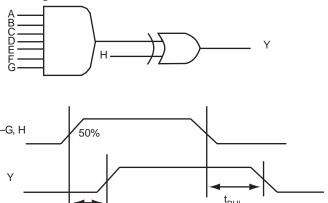




3.10.4 Decode Module Timing

The following figure shows decode module timing.

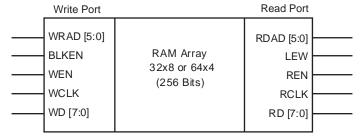
Figure 28 • Decode Module Timing



3.10.5 SRAM Timing Characteristics

The following figure shows SRAM timing characteristics.

Figure 29 • SRAM Timing Characteristics



3.10.6 Dual-Port SRAM Timing Waveforms

The following figures show dual-port SRAM timing waveforms.



Table 34 • A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (continued) (Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J = 70^{\circ}C$)

			-3 Sp	peed	–2 Sp	peed	–1 Sp	eed	Std S	peed	−F Sp	eed	
Parame	eter / Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Input N	Module Propagation	Delays											
t _{INYH}	Pad-to-Y HIGH			0.7		8.0		0.9		1.1		1.5	ns
t _{INYL}	Pad-to-Y LOW			0.6		0.7		8.0		1.0		1.3	ns
Input N	Module Predicted Ro	outing Dela	ıys ¹										
t _{IRD1}	FO = 1 Routing De	lay		2.1		2.4		2.2		3.2		4.5	ns
t _{IRD2}	FO = 2 Routing De	lay		2.6		3.0		3.4		4.0		5.6	ns
t _{IRD3}	FO = 3 Routing De	lay		3.1		3.6		4.1		4.8		6.7	ns
t _{IRD4}	FO = 4 Routing De	lay		3.6		4.2		4.8		5.6		7.8	ns
t _{IRD8}	FO = 8 Routing De	lay		5.7		6.6		7.5		8.8		12.4	ns
Global	Clock Network												
t _{CKH}	Input Low to HIGH	FO = 16 FO = 128		4.6 4.6		5.3 5.3		6.0 6.0		7.0 7.0		9.8 9.8	ns
t _{CKL}	Input High to LOW	FO = 16 FO = 128		4.8 4.8		5.6 5.6		6.3 6.3		7.4 7.4		10.4 10.4	ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.1		3.4 3.6		4.8 5.1		ns
t _{PWL}	Minimum Pulse Width LOW	FO = 16 FO = 128	2.2 2.4		2.6 2.7		2.9 3.01		3.4 3.6		4.8 5.1		ns
t _{CKSW}	Maximum Skew	FO = 16 FO = 128		0.4 0.5		0.5 0.6		0.5 0.7		0.6 0.8		0.8 1.2	ns
t _P	Minimum Period	FO = 16 FO = 128	4.7 4.8		5.4 5.6		6.1 6.3		7.2 7.5		10.0 10.4		ns
f _{MAX}	Maximum Frequency	FO = 16 FO = 128		188 181		175 168		160 154		139 134		83 80	MHz



Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

			−3 S	peed	-2 S _I	peed	-1 S	peed	Std S	Speed	−F Sp	peed	
Paramet	ter / Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Input Mo	odule Propagation Dela	ys											
t _{INYH}	Pad-to-Y HIGH			1.5		1.6		1.8		2.17		3.0	ns
t _{INYL}	Pad-to-Y LOW			1.2		1.3		1.4		1.7		2.4	ns
t _{INGH}	G to Y HIGH			1.8		2.0		2.3		2.7		3.7	ns
t _{INGL}	G to Y LOW			1.8		2.0		2.3		2.7		3.7	ns
Input Mo	odule Predicted Routing	g Delays ²											
t _{IRD1}	FO = 1 Routing Delay			2.8		3.2		3.6		4.2		5.9	ns
t _{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.0		4.7		6.6	ns
t _{IRD3}	FO = 3 Routing Delay			3.5		3.9		4.4		5.2		7.3	ns
t _{IRD4}	FO = 4 Routing Delay			3.9		4.3		4.9		5.7		8.0	ns
t _{IRD8}	FO = 8 Routing Delay			5.2		5.8		6.6		7.7		10.8	ns
Global C	Clock Network												
t _{CKH}	Input LOW to HIGH	FO = 32 FO = 256		4.1 4.5		4.5 5.0		5.1 5.6		6.0 6.7		8.4 9.3	ns ns
t _{CKL}	Input HIGH to LOW	FO = 32 FO = 256		5.0 5.4		5.5 6.0		6.2 6.8		7.3 8.0		10.2 11.2	ns ns
t _{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 256	1.7 1.9		1.9 2.1		2.1 2.3		2.5 2.7		3.5 3.8		ns ns
t _{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 256	1.7 1.9		1.9 2.1		2.1 2.3		2.5 2.7		3.5 3.8		ns ns
t _{CKSW}	Maximum Skew	FO = 32 FO = 256		0.4 0.4		0.5 0.5		0.5 0.5		0.6 0.6		0.9 0.9	ns ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.0		0.0		0.0		0.0		0.0		ns ns
t _{HEXT}	Input Latch External Hold	FO = 32 FO = 256	3.3 3.7		3.7 4.1		4.2 4.6		4.9 5.5		6.9 7.6		ns ns
t _P	Minimum Period	FO = 32 FO = 256	5.6 6.1		6.2 6.8		6.7 7.4		7.8 8.5		12.9 14.2		ns ns
f _{MAX}	Maximum Frequency	FO = 32 FO = 256		177 161		161 146		148 135		129 117		77 70	MHz MHz



Table 39 • A42MX09 Timing Characteristics (Nominal 3.3 V Operation) (continued)(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

		−3 S	peed	-2 S _I	peed	-1 S	peed	Std S	Speed	−F S _I	oeed	
Parame	ter / Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
CMOS	Output Module Timing ⁵											
t _{DLH}	Data-to-Pad HIGH		3.4		3.8		5.5		6.4		9.0	ns
t _{DHL}	Data-to-Pad LOW		4.1		4.5		4.2		5.0		7.0	ns
t _{ENZH}	Enable Pad Z to HIGH		3.7		4.1		4.6		5.5		7.6	ns
t _{ENZL}	Enable Pad Z to LOW		4.1		4.5		5.1		6.1		8.5	ns
t _{ENHZ}	Enable Pad HIGH to Z		6.9		7.6		8.6		10.2		14.2	ns
t _{ENLZ}	Enable Pad LOW to Z		7.5		8.3		9.4		11.1		15.5	ns
t _{GLH}	G-to-Pad HIGH		5.8		6.5		7.3		8.6		12.0	ns
t _{GHL}	G-to-Pad LOW		5.8		6.5		7.3		8.6		12.0	ns
t _{LSU}	I/O Latch Set-Up	0.7		0.8		0.9		1.0		1.4		ns
t _{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading		8.7		9.7		10.9		12.9		18.0	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading		12.2		13.5		15.4		18.1		25.3	ns
d _{TLH}	Capacity Loading, LOW to HIGH		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacity Loading, HIGH to LOW		0.05		0.05		0.06		0.07		0.10	ns/pF

^{1.} For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn} , t_{CO} + t_{RD1} + t_{PDn} , or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.

Table 40 • A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J = 70^{\circ}$ C)

		-3 Speed	-2 Speed	-1 Speed	Std Speed	-F Speed	
Parame	eter / Description	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Units
Logic I	Module Propagation Delays ¹						
t _{PD1}	Single Module	1.4	1.5	1.7	2.0	2.8	ns
t _{CO}	Sequential Clock-to-Q	1.4	1.6	1.8	2.1	3.0	ns
t _{GO}	Latch G-to-Q	1.4	1.5	1.7	2.0	2.8	ns
t _{RS}	Flip-Flop (Latch) Reset-to-Q	1.6	1.7	2.0	2.3	3.3	ns
Logic I	Module Predicted Routing Delays	s ²					
t _{RD1}	FO = 1 Routing Delay	0.8	0.9	1.0	1.2	1.6	ns
t _{RD2}	FO = 2 Routing Delay	1.0	1.2	1.3	1.5	2.1	ns

^{2.} Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

^{3.} Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.

^{4.} Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

^{5.} Delays based on 35 pF loading.



Table 41 • A42MX16 Timing Characteristics (Nominal 3.3 V Operation) (continued) (Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J = 70^{\circ}$ C)

			−3 S	peed	–2 Sp	peed	-1 S	peed	Std S	Speed	−F Sp	eed	
Paramet	er / Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	5.3 6.2		5.9 6.9		6.7 7.9		7.8 9.2		11.0 12.9		ns ns
t _{CKSW}	Maximum Skew	FO = 32 FO = 384		0.5 2.2		0.5 2.4		0.6 2.7		0.7 3.2		1.0 4.5	ns ns
t _{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0		0.0		0.0		0.0		0.0		ns ns
t _{HEXT}	Input Latch External Hold	FO = 32 FO = 384	3.9 4.5		4.3 4.9		4.9 5.6		5.7 6.6		8.0 9.2		ns ns
t _P	Minimum Period	FO = 32 FO = 384	7.0 7.7		7.8 8.6		8.4 9.3		9.7 10.7		16.2 17.8		ns ns
f _{MAX}	Maximum Frequency	FO = 32 FO = 384		142 129		129 117		119 108		103 94		62 56	MHz MHz
TTL Out	put Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH			3.5		3.9		4.4		5.2		7.3	ns
t _{DHL}	Data-to-Pad LOW			4.1		4.6		5.2		6.1		8.6	ns
t _{ENZH}	Enable Pad Z to HIGI	1		3.8		4.2		4.8		5.6		7.8	ns
t _{ENZL}	Enable Pad Z to LOW	I		4.2		4.6		5.3		6.2		8.7	ns
t _{ENHZ}	Enable Pad HIGH to 2	Z		7.6		8.4		9.5		11.2		15.7	ns
t _{ENLZ}	Enable Pad LOW to 2	7		7.0		7.8		8.8		10.4		14.5	ns
t _{GLH}	G-to-Pad HIGH			4.8		5.3		6.0		7.2		10.0	ns
t _{GHL}	G-to-Pad LOW			4.8		5.3		6.0		7.2		10.0	ns
t _{LCO}	I/O Latch Clock-to-Ou (Pad-to-Pad), 64 Cloc			8.0		8.9		10.1		11.9		16.7	ns
t _{ACO}	Array Clock-to-Out (Pad-to-Pad), 64 Cloc	ck Loading		11.3		12.5		14.2		16.7		23.3	ns
d _{TLH}	Capacitive Loading, L HIGH	.OW to		0.04		0.04		0.05		0.06		0.08	ns/pF
d _{THL}	Capacitive Loading, F LOW	HIGH to		0.05		0.05		0.06		0.07		0.10	ns/pF
CMOS C	output Module Timing ⁵												
t _{DLH}	Data-to-Pad HIGH			4.5		5.0		5.6		6.6		9.3	ns
t _{DHL}	Data-to-Pad LOW			3.4		3.8		4.3		5.1		7.1	ns
t _{ENZH}	Enable Pad Z to HIGH	1		3.8		4.2		4.8		5.6		7.8	ns
t _{ENZL}	Enable Pad Z to LOW	I		4.2		4.6		5.3		6.2		8.7	ns
t _{ENHZ}	Enable Pad HIGH to	Z		7.6		8.4		9.5		11.2		15.7	ns
t _{ENLZ}	Enable Pad LOW to 2	7		7.0		7.8		8.8		10.4		14.5	ns
t _{GLH}	G-to-Pad HIGH			7.1		7.9		8.9		10.5		14.7	ns
t _{GHL}	G-to-Pad LOW			7.1		7.9		8.9		10.5		14.7	ns
t _{LCO}	I/O Latch Clock-to-Ou (Pad-to-Pad), 64 Cloc			8.0		8.9		10.1		11.9		16.7	ns



4 Package Pin Assignments

The following figures and tables give the details of the package pin assignments.

Figure 38 • PL44

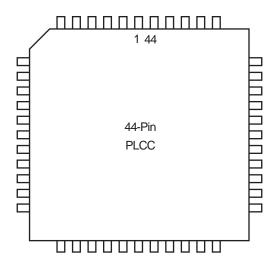


Table 47 • PL44

	PL44		
1/O	Pin Number	A40MX02 Function	A40MX04 Function
VCC VCC	1	I/O	I/O
1/O	2	I/O	I/O
1/O	3	VCC	VCC
I/O	4	I/O	I/O
I/O	5	I/O	I/O
1/O	6	I/O	I/O
I/O	7	I/O	I/O
GND GND GND 11 I/O I/O 12 I/O I/O 13 I/O I/O 14 VCC VCC 15 I/O I/O 16 VCC VCC 17 I/O I/O 18 I/O I/O 19 I/O I/O	8	I/O	I/O
1	9	I/O	I/O
1/O	10	GND	GND
3	11	I/O	I/O
14 VCC VCC 15 I/O I/O 16 VCC VCC 17 I/O I/O 18 I/O I/O 19 I/O I/O	12	I/O	I/O
15 I/O I/O 16 VCC VCC 17 I/O I/O 18 I/O I/O 19 I/O I/O	13	I/O	I/O
16 VCC 17 I/O 18 I/O 19 I/O	14	VCC	VCC
17 I/O I/O 18 I/O I/O 19 I/O I/O	15	I/O	I/O
8	16	VCC	VCC
9 I/O I/O	17	I/O	I/O
	18	I/O	I/O
20 I/O I/O	19	I/O	I/O
	20	I/O	I/O



Figure 39 • PL68

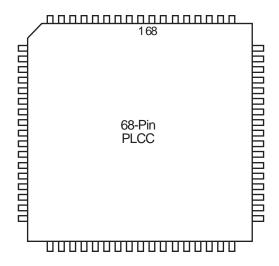


Table 48 • PL68

A40MX02 Function	A40MX04 Function
I/O	I/O
I/O	I/O
I/O	I/O
VCC	VCC
I/O	I/O
GND	GND
GND	GND
I/O	I/O
VCC	VCC
I/O	I/O
I/O	I/O
	I/O



Table 52 • PQ160

PQ160			
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function
21	CLKA, I/O	CLKA, I/O	CLKA, I/O
22	I/O	I/O	I/O
23	PRA, I/O	PRA, I/O	PRA, I/O
24	NC	I/O	WD, I/O
25	I/O	I/O	WD, I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	NC	I/O	I/O
29	I/O	I/O	WD, I/O
30	GND	GND	GND
31	NC	I/O	WD, I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	VCCI	VCCI
36	I/O	I/O	WD, I/O
37	I/O	I/O	WD, I/O
38	SDI, I/O	SDI, I/O	SDI, I/O
39	I/O	I/O	I/O
40	GND	GND	GND
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	GND	GND	GND
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	NC	I/O	I/O
53	I/O	I/O	I/O
54	NC	VCCA	VCCA
55	I/O	I/O	I/O
56	I/O	I/O	I/O
		VCCA	VCCA



Table 54 • PQ240

Pin Number A42MX36 Function 163 WD, I/O 164 WD, I/O 165 I/O 166 QCLKA, I/O 167 I/O 168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 198 I/O 199	PQ240		
164 WD, I/O 165 I/O 166 QCLKA, I/O 167 I/O 168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 188 I/O 189 I/O 190 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 197 I/O 197 I/O	Pin Number	A42MX36 Function	_
165 I/O 166 QCLKA, I/O 167 I/O 168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 197 I/O 198 I/O	163	WD, I/O	
166 QCLKA, I/O 167 I/O 168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 188 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 197 I/O 198 I/O 198 I/O	164	WD, I/O	
167 I/O 168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 195 I/O 196 I/O 198 I/O	165	I/O	
168 I/O 169 I/O 170 I/O 171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 198 I/O	166	QCLKA, I/O	
169	167	I/O	
170	168	I/O	
171 I/O 172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 188 I/O 190 I/O 191 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 197 I/O 198 I/O	169	I/O	
172 VCCI 173 I/O 174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	170	I/O	
173	171	I/O	
174 WD, I/O 175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 188 I/O 190 I/O 191 I/O 191 I/O 192 VCCI 193 I/O 196 I/O 197 I/O 198 I/O	172	VCCI	
175 WD, I/O 176 I/O 177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 196 I/O 197 I/O 198 I/O	173	I/O	
176	174	WD, I/O	
177 I/O 178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	175	WD, I/O	
178 TDI, I/O 179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	176	I/O	
179 TMS, I/O 180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	177	I/O	
180 GND 181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 196 I/O 197 I/O 198 I/O	178	TDI, I/O	
181 VCCA 182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 196 I/O 197 I/O 198 I/O	179	TMS, I/O	
182 GND 183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	180	GND	
183 I/O 184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	181	VCCA	
184 I/O 185 I/O 186 I/O 187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 198 I/O	182	GND	
185 I/O 186 I/O 187 I/O 188 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	183	I/O	
186 I/O 187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	184	I/O	
187 I/O 188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	185	I/O	
188 I/O 189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	186	I/O	
189 I/O 190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	187	I/O	
190 I/O 191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	188	I/O	
191 I/O 192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	189	I/O	
192 VCCI 193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	190	I/O	
193 I/O 194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	191	I/O	
194 I/O 195 I/O 196 I/O 197 I/O 198 I/O	192	VCCI	
195 I/O 196 I/O 197 I/O 198 I/O	193	I/O	
196 I/O 197 I/O 198 I/O	194	I/O	
197 I/O 198 I/O	195	I/O	
198 I/O	196	I/O	
	197	I/O	
199 I/O	198	I/O	
	199	I/O	_



Table 57 • TQ176

TQ176					
Pin Number	A42MX09 Function	A42MX16 Function	A42MX24 Function		
121	NC	NC	I/O		
122	I/O	I/O	I/O		
123	I/O	I/O	I/O		
124	NC	I/O	I/O		
125	NC	I/O	I/O		
126	NC	NC	I/O		
127	I/O	I/O	I/O		
128	I/O	I/O	I/O		
129	I/O	I/O	I/O		
130	I/O	I/O	I/O		
131	I/O	I/O	I/O		
132	I/O	I/O	I/O		
133	GND	GND	GND		
134	I/O	I/O	I/O		
135	SDI, I/O	SDI, I/O	SDI, I/O		
136	NC	I/O	I/O		
137	I/O	I/O	WD, I/O		
138	I/O	I/O	WD, I/O		
139	I/O	I/O	I/O		
140	NC	VCCI	VCCI		
141	I/O	I/O	I/O		
142	I/O	I/O	I/O		
143	NC	I/O	I/O		
144	NC	I/O	WD, I/O		
145	NC	NC	WD, I/O		
146	I/O	I/O	I/O		
147	NC	I/O	I/O		
148	I/O	I/O	I/O		
149	I/O	I/O	I/O		
150	I/O	I/O	WD, I/O		
151	NC	I/O	WD, I/O		
152	PRA, I/O	PRA, I/O	PRA, I/O		
153	I/O	I/O	I/O		
154	CLKA, I/O	CLKA, I/O	CLKA, I/O		
155	VCCA	VCCA	VCCA		
156	GND	GND	GND		



Table 58 • CQ208

Pin Number A42MX36 Function 74 I/O 75 I/O 76 I/O 77 I/O 78 GND 79 VCCA 80 VCCI 81 I/O 82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O <	CQ208		
75	Pin Number	A42MX36 Function	
76 I/O 77 I/O 78 GND 79 VCCA 80 VCCI 81 I/O 82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	74	I/O	
77	75	I/O	
78 GND 79 VCCA 80 VCCI 81 I/O 82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 88 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 104 I/O 105 GND 100 I/O 108 I/O 109 I/O	76	I/O	
79 VCCA 80 VCCI 81 I/O 82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	77	I/O	_
80 VCCI 81 I/O 82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	78	GND	
81	79	VCCA	
82 I/O 83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	80	VCCI	
83 I/O 84 I/O 85 WD, I/O 86 WD, I/O 87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	81	I/O	
84	82	I/O	
85 WD, I/O 86 WD, I/O 87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	83	I/O	
86 WD, I/O 87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	84	I/O	
87 I/O 88 I/O 89 I/O 90 I/O 91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	85	WD, I/O	
88	86	WD, I/O	
89	87	I/O	
90	88	I/O	
91 QCLKB, I/O 92 I/O 93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	89	I/O	
92	90	I/O	
93 WD, I/O 94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	91	QCLKB, I/O	
94 WD, I/O 95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	92	I/O	
95 I/O 96 I/O 97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O	93	WD, I/O	
96	94	WD, I/O	
97 I/O 98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	95	I/O	
98 VCCI 99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	96	I/O	
99 I/O 100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	97	I/O	
100 WD, I/O 101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	98	VCCI	
101 WD, I/O 102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	99	I/O	
102 I/O 103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	100	WD, I/O	
103 TDO, I/O 104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	101	WD, I/O	
104 I/O 105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	102	I/O	
105 GND 106 VCCA 107 I/O 108 I/O 109 I/O	103	TDO, I/O	
106 VCCA 107 I/O 108 I/O 109 I/O	104	I/O	
107 I/O 108 I/O 109 I/O	105	GND	
108 I/O 109 I/O	106	VCCA	
109 I/O	107	I/O	
	108	I/O	
110 I/O	109	I/O	
	110	I/O	



Table 61 • PG132

A42MX09 Function	
I/O	
I/O	
I/O	
VSV	
I/O	
BININ	
BINOUT	
I/O	
	I/O



Table 61 • PG132

PG132	
Pin Number	A42MX09 Function
B3	I/O
A2	I/O
C3	DCLK
B5	GNDA
E12	GNDA
J2	GNDA
M9	GNDA
B9	GNDI
C5	GNDI
E11	GNDI
F4	GNDI
J3	GNDI
J11	GNDI
L5	GNDI
L9	GNDI
C9	GNDQ
E3	GNDQ
K12	GNDQ
D7	VCCA
G3	VCCA
G10	VCCA
L7	VCCA
C7	VCCI
G2	VCCI
G11	VCCI
K7	VCCI