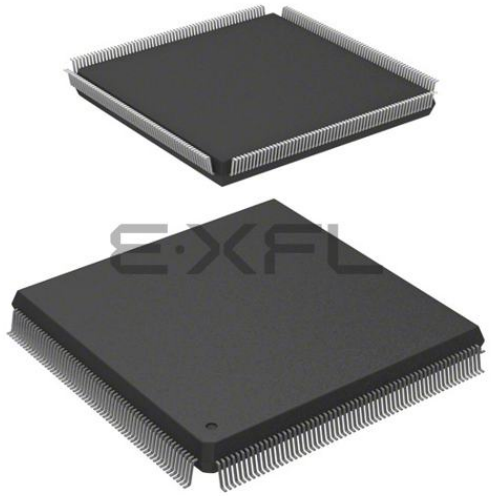

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Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	2560
Number of I/O	202
Number of Gates	54000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a42mx36-1pqg240

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Tables

2.4 Plastic Device Resources

Table 2 • **Plastic Device Resources**

	User I/Os											
Device	**PLCC 44-Pin**	**PLCC 68-Pin**	**PLCC 84-Pin**	**PQFP 100-Pin**	**PQFP 144-Pin**	**PQFP 160-Pin**	**PQFP 208-Pin**	**PQFP 240-Pin**	**VQFP 80-Pin**	**VQFP 100-Pin**	**TQFP 176-Pin**	**PBGA 272-Pin**
A40MX02	34	57	–	57	–	–	–	–	57	–	–	–
A40MX04	34	57	69	69	–	–	–	–	69	–	–	–
A42MX09	–	–	72	83	95	101	–	–	–	83	104	–
A42MX16	–	–	72	83	–	125	140	–	–	83	140	–
A42MX24	–	–	72	–	–	125	176	–	–	–	150	–
A42MX36	–	–	–	–	–	–	176	202	–	–	–	202

Note: Package Definitions: PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

2.5 Ceramic Device Resources

Table 3 • **Ceramic Device Resources**

	User I/Os			
Device	**CPGA 132-Pin**	**CQFP 172-Pin**	**CQFP 208-Pin**	**CQFP 256-Pin**
A42MX09	95			
A42MX16		131		
A42MX36			176	202

Note: Package Definitions: CQFP = Ceramic Quad Flat Pack

Table 23 • **DC Specification (5.0 V PCI Signaling)[1]**

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C_{IN}	Input Pin Capacitance			10	—	10	pF
C_{CLK}	CLK Pin Capacitance		5	12	—	10	pF
L_{PIN}	Pin Inductance			20	—	< 8 nH[4]	nH

1. PCI Local Bus Specification, Version 2.1, Section 4.2.1.1.
2. Maximum rating for VCCI –0.5 V to 7.0 V
3. VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V.
4. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

Table 24 • **AC Specifications (5.0V PCI Signaling)***

			PCI		MX		
Symbol	**Parameter**	**Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
ICL	Low Clamp Current	–5 < VIN ≤ –1	–25 + (VIN +1) /0.015		–60	–10	mA
Slew (r)	Output Rise Slew Rate	0.4 V to 2.4 V load	1	5	1.8	2.8	V/ns
Slew (f)	Output Fall Slew Rate	2.4 V to 0.4 V load	1	5	2.8	4.3	V/ns

Note: *PCI Local Bus Specification, Version 2.1, Section 4.2.1.2.

Figure 22 • **AC Test Loads**

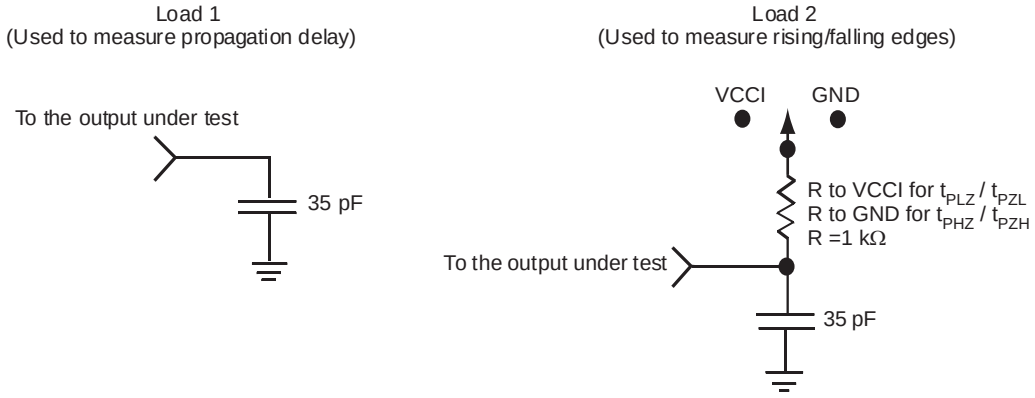


Figure 23 • **Input Buffer Delays**

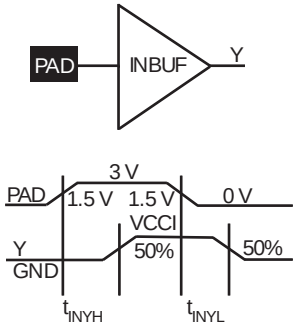


Figure 24 • **Module Delays**

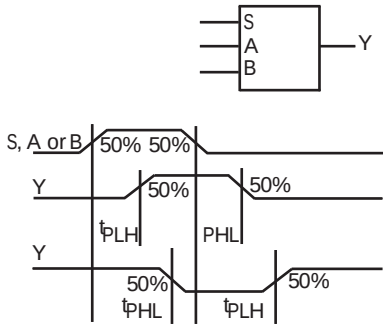


Table 34 • **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
(Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.3		3.8		4.3		5.1		7.2	ns
t_{DHL}	Data-to-Pad LOW		4.0		4.6		5.2		6.1		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH		3.7		4.3		4.9		5.8		8.0	ns
t_{ENZL}	Enable Pad Z to LOW		4.7		5.4		6.1		7.2		10.1	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.1	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.02		0.03		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.03		0.03		0.04		0.06	ns/pF
CMOS Output Module Timing[4]												
t_{DLH}	Data-to-Pad HIGH		3.9		4.5		5.1		6.05		8.5	ns
t_{DHL}	Data-to-Pad LOW		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZH}	Enable Pad Z to HIGH		3.4		3.9		4.4		5.2		7.3	ns
t_{ENZL}	Enable Pad Z to LOW		4.9		5.6		6.4		7.5		10.5	ns
t_{ENHZ}	Enable Pad HIGH to Z		7.9		9.1		10.4		12.2		17.0	ns
t_{ENLZ}	Enable Pad LOW to Z		5.9		6.8		7.7		9.0		12.6	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.04		0.05		0.07	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02		0.03		0.03		0.04	ns/pF

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

Table 35 • **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
(Worst-Case Commercial Conditions, VCC = 3.0 V, T_J = 70°C)

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Propagation Delays												
t_{PD1}	Single Module		1.7		2.0		2.3		2.7		3.7	ns
t_{PD2}	Dual-Module Macros		3.7		4.3		4.9		5.7		8.0	ns
t_{CO}	Sequential Clock-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch G-to-Q		1.7		2.0		2.3		2.7		3.7	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		1.7		2.0		2.3		2.7		3.7	ns
Logic Module Predicted Routing Delays[1]												

Table 43 • **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)**

Parameter / Description		–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Logic Module Sequential Timing[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.0		2.3		2.7		3.7	ns
t_{GO}	Latch Gate-to-Output		3.4		1.9		2.1		2.5		3.4	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.4		0.5		0.6		0.7		0.9		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset-to-Output		2.0		2.2		2.5		2.9		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.6		0.7		0.8		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	4.6		5.2		5.8		6.9		9.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.1		6.8		7.7		9.0		12.6		ns
Input Module Propagation Delays												
t_{INPY}	Input Data Pad-to-Y		1.4		1.6		1.8		2.2		3.0	ns
t_{INGO}	Input Latch Gate-to-Output		1.8		1.9		2.2		2.6		3.6	ns
t_{INH}	Input Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up	0.7		0.7		0.8		1.0		1.4		ns
t_{ILA}	Latch Active Pulse Width	6.5		7.3		8.2		9.7		13.5		ns

Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL Output Module Timing[5] (continued)													
t_{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
CMOS Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			4.8		5.3		5.5		6.4		9.0	ns
t_{DHL}	Data-to-Pad LOW			3.5		3.9		4.1		4.9		6.8	ns
t_{ENZH}	Enable Pad Z to HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{ENZL}	Enable Pad Z to LOW			3.4		4.0		5.0		5.8		8.2	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.2		8.0		9.0		10.7		14.9	ns
t_{ENLZ}	Enable Pad LOW to Z			6.7		7.5		8.5		9.9		13.9	ns
t_{GLH}	G-to-Pad HIGH			6.8		7.6		8.6		10.1		14.2	ns
t_{GHL}	G-to-Pad LOW			6.8		7.6		8.6		10.1		14.2	ns
t_{LSU}	I/O Latch Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.7		8.5		9.6		11.3		15.9	ns
t_{ACO}	Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O			14.8		16.5		18.7		22.0		30.8	ns
d_{TLH}	Capacitive Loading, LOW to HIGH			0.05		0.05		0.06		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, HIGH to LOW			0.04		0.04		0.05		0.06		0.08	ns/pF
t_{HEXT}	Input Latch External Hold	FO = 32	3.9		4.3		4.9		5.7		8.1		ns
		FO = 486	4.6		5.2		5.8		6.9		9.6		ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32	7.8		8.7		9.5		10.8		18.2		ns
		FO = 486	8.6		9.5		10.4		11.9		19.9		ns

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

Table 45 • A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, T_J = 70°C)

Parameter / Description			–3 Speed		–2 Speed		–1 Speed		Std Speed		–F Speed		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Module Predicted Routing Delays[2]													
t_{IRD1}	FO = 1 Routing Delay			2.8		3.1		3.5		4.1		5.7	ns
t_{IRD2}	FO = 2 Routing Delay			3.2		3.5		4.1		4.8		6.7	ns
t_{IRD3}	FO = 3 Routing Delay			3.7		4.1		4.7		5.5		7.7	ns
t_{IRD4}	FO = 4 Routing Delay			4.2		4.6		5.3		6.2		8.7	ns
t_{IRD8}	FO = 8 Routing Delay			6.1		6.8		7.7		9.0		12.6	ns
Global Clock Network													
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 635		4.6 5.0		5.1 5.6		5.7 6.3		6.7 7.4		9.3 10.3	ns ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 635		5.3 6.8		5.9 7.6		6.7 8.6		7.8 10.1		11.0 14.1	ns ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 635	2.5 2.8		2.7 3.1		3.1 3.5		3.6 4.1		5.1 5.7		ns ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 635	2.5 2.8		2.7 3.1		3.1 3.5		3.6 4.1		5.1 5.7		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 635		1.0 1.0		1.2 1.2		1.3 1.3		1.5 1.5		2.2 2.2	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 635	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 635	4.0 4.6		4.4 5.2		5.0 5.9		5.9 6.9		8.2 9.6		ns ns
t_P	Minimum Period ($1/f_{MAX}$)	FO = 32 FO = 635	9.2 9.9		10.2 11.0		11.1 12.0		12.7 13.8		21.2 23.0		ns ns
f_{MAX}	Maximum Datapath Frequency	FO = 32 FO = 635		108 100		98 91		90 83		79 73		47 44	MHz MHz
TTL Output Module Timing[5]													
t_{DLH}	Data-to-Pad HIGH			3.6		4.0		4.5		5.3		7.4	ns
t_{DHL}	Data-to-Pad LOW			4.2		4.6		5.2		6.2		8.6	ns
t_{ENZH}	Enable Pad Z to HIGH			3.7		4.2		4.7		5.5		7.7	ns
t_{ENZL}	Enable Pad Z to LOW			4.1		4.6		5.2		6.1		8.5	ns
t_{ENHZ}	Enable Pad HIGH to Z			7.34		8.2		9.3		10.9		15.3	ns
TTL Output Module Timing[5]													
t_{ENLZ}	Enable Pad LOW to Z			6.9		7.6		8.7		10.2		14.3	ns
t_{GLH}	G-to-Pad HIGH			4.9		5.5		6.2		7.3		10.2	ns
t_{GHL}	G-to-Pad LOW			4.9		5.5		6.2		7.3		10.2	ns
t_{LSU}	I/O Latch Output Set-Up		0.7		0.7		0.8		1.0		1.4		ns
t_{LH}	I/O Latch Output Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O			7.9		8.8		10.0		11.8		16.5	ns

Table 47 • **PL44**

PL44		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
21	GND	GND
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	CLK, I/O	CLK, I/O
34	MODE	MODE
35	VCC	VCC
36	SDI, I/O	SDI, I/O
37	DCLK, I/O	DCLK, I/O
38	PRA, I/O	PRA, I/O
39	PRB, I/O	PRB, I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	GND	GND
44	I/O	I/O

Figure 39 • **PL68**

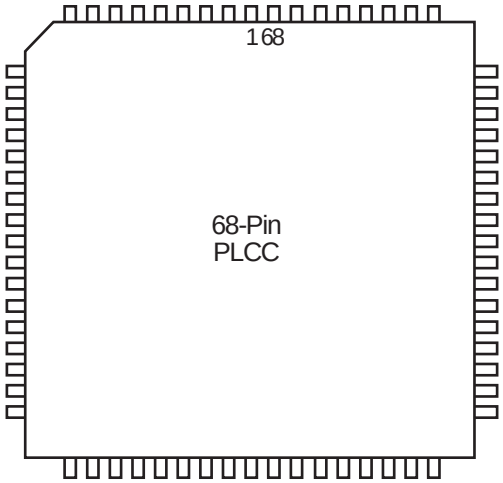


Table 48 • **PL68**

PL68		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
1	I/O	I/O
2	I/O	I/O
3	I/O	I/O
4	VCC	VCC
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	GND	GND
15	GND	GND
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	VCC	VCC
22	I/O	I/O
23	I/O	I/O

Table 48 • **PL68**

PL68		
Pin Number	**A40MX02 Function**	**A40MX04 Function**
24	I/O	I/O
25	VCC	VCC
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	GND	GND
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	VCC	VCC
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	GND	GND
50	I/O	I/O
51	I/O	I/O
52	CLK, I/O	CLK, I/O
53	I/O	I/O
54	MODE	MODE
55	VCC	VCC
56	SDI, I/O	SDI, I/O
57	DCLK, I/O	DCLK, I/O
58	PRA, I/O	PRA, I/O
59	PRB, I/O	PRB, I/O
60	I/O	I/O

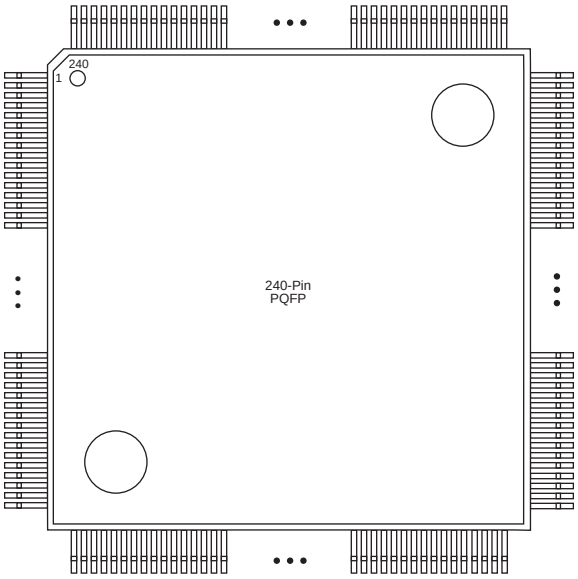
Table 52 • **PQ160**

PQ160			
Pin Number	**A42MX09 Function**	**A42MX16 Function**	**A42MX24 Function**
58	VCCI	VCCI	VCCI
59	GND	GND	GND
60	VCCA	VCCA	VCCA
61	LP	LP	LP
62	I/O	I/O	TCK, I/O
63	I/O	I/O	I/O
64	GND	GND	GND
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	I/O	I/O	I/O
69	GND	GND	GND
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	I/O	I/O	I/O
77	NC	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	GND	GND	GND
81	I/O	I/O	I/O
82	SDO, I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	WD, I/O
84	I/O	I/O	WD, I/O
85	I/O	I/O	I/O
86	NC	VCCI	VCCI
87	I/O	I/O	I/O
88	I/O	I/O	WD, I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O

Table 53 • **PQ208**

PQ208			
Pin Number	**A42MX16 Function**	**A42MX24 Function**	**A42MX36 Function**
206	I/O	I/O	I/O
207	DCLK, I/O	DCLK, I/O	DCLK, I/O
208	I/O	I/O	I/O

Figure 45 • **PQ240**



Note: This figure shows the 240-Pin PQFP Package top view.

Table 54 • **PQ240**

PQ240	
Pin Number	**A42MX36 Function**
1	I/O
2	DCLK, I/O
3	I/O
4	I/O
5	I/O
6	WD, I/O
7	WD, I/O
8	VCCI
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O

Table 58 • **CQ208**

CQ208	
Pin Number	**A42MX36 Function**
185	I/O
186	CLKB, I/O
187	I/O
188	PRB, I/O
189	I/O
190	WD, I/O
191	WD, I/O
192	I/O
193	I/O
194	WD, I/O
195	WD, I/O
196	QCLKC, I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	I/O
202	VCCI
203	WD, I/O
204	WD, I/O
205	I/O
206	I/O
207	DCLK, I/O
208	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
A6	I/O
A7	WD, I/O
A8	WD, I/O
A9	I/O
A10	I/O
A11	CLKA
A12	I/O
A13	I/O
A14	I/O
A15	I/O
A16	WD, I/O
A17	I/O
A18	I/O
A19	GND
A20	GND
B1	GND
B2	GND
B3	DCLK, I/O
B4	I/O
B5	I/O
B6	I/O
B7	WD, I/O
B8	I/O
B9	PRB, I/O
B10	I/O
B11	I/O
B12	WD, I/O
B13	I/O
B14	I/O
B15	WD, I/O
B16	I/O
B17	WD, I/O
B18	I/O
B19	GND
B20	GND
C1	I/O
C2	MODE

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
C3	GND
C4	I/O
C5	WD, I/O
C6	I/O
C7	QCLKC, I/O
C8	I/O
C9	I/O
C10	CLKB
C11	PRA, I/O
C12	WD, I/O
C13	I/O
C14	QCLKD, I/O
C15	I/O
C16	WD, I/O
C17	SDI, I/O
C18	I/O
C19	I/O
C20	I/O
D1	I/O
D2	I/O
D3	I/O
D4	I/O
D5	VCCI
D6	I/O
D7	I/O
D8	VCCA
D9	WD, I/O
D10	VCCI
D11	I/O
D12	VCCI
D13	I/O
D14	VCCI
D15	I/O
D16	VCCA
D17	GND
D18	I/O
D19	I/O

Table 60 • **BG272**

BG272	
Pin Number	**A42MX36 Function**
D20	I/O
E1	I/O
E2	I/O
E3	I/O
E4	VCCA
E17	VCCI
E18	I/O
E19	I/O
E20	I/O
F1	I/O
F2	I/O
F3	I/O
F4	VCCI
F17	I/O
F18	I/O
F19	I/O
F20	I/O
G1	I/O
G2	I/O
G3	I/O
G4	VCCI
G17	VCCI
G18	I/O
G19	I/O
G20	I/O
H1	I/O
H2	I/O
H3	I/O
H4	VCCA
H17	I/O
H18	I/O
H19	I/O
H20	I/O
J1	I/O
J2	I/O
J3	I/O
J4	VCCI

Table 61 • **PG132**

PG132	
Pin Number	**A42MX09 Function**
F2	I/O
F1	I/O
G1	I/O
G4	VSV
H1	I/O
H2	I/O
H3	I/O
H4	I/O
J1	I/O
K1	I/O
L1	I/O
K2	I/O
M1	I/O
K3	I/O
L2	I/O
N1	I/O
L3	BININ
M2	BINOUT
N2	I/O
M3	I/O
L4	I/O
N3	I/O
M4	I/O
N4	I/O
M5	I/O
K6	I/O
N5	I/O
N6	I/O
L6	I/O
M6	I/O
M7	I/O
N7	I/O
N8	I/O
M8	I/O
L8	I/O
K8	I/O
N9	I/O