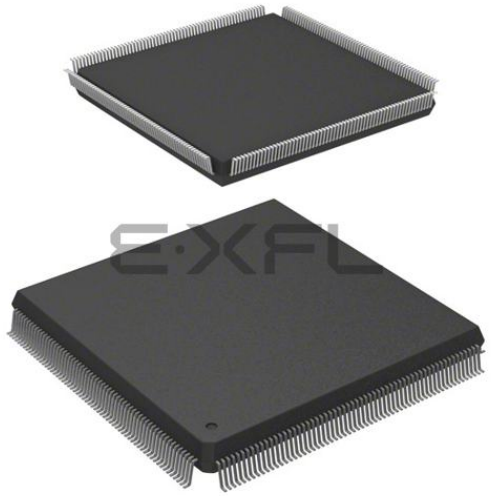


Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 2560 |
| Number of I/O | 202 |
| Number of Gates | 54000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a42mx36-2pq240 |

# Figures

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 15.0

The following is a summary of the changes in revision 15.0 of this document.

- Table 15, page 21 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 22, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V
- Table 23, page 25 is edited to add the footnote, VIH(Min) is 2.4V for A42MX36 family. This applies only to VCCI of 5V and is not applicable to VCCI of 3.3V

## 1.2 Revision 14.0

The following is a summary of the changes in revision 14.0 of this document.

- Added CQFP package information for A42MX16 device in Product Profile, page 1 and Ceramic Device Resources, page 4 (SAR 79522).
- Added Military (M) and MIL-STD-883 Class B (B) grades for CPGA 132 Package and added Commercial (C), Military (M), and MIL-STD-883 Class B (B) grades for CQFP 172 Package in Temperature Grade Offerings, page 5 (SAR 79519)
- Changed Silicon Sculptor II to Silicon Sculptor in Programming, page 12 (SAR 38754)
- Added Figure 53, page 158 CQ172 package (SAR 79522).

## 1.3 Revision 13.0

The following is a summary of the changes in revision 13.0 of this document.

- Added Figure 42, page 97 PQ144 Package for A42MX09 device (SAR 69776)
- Added Figure 52, page 153 PQ132 Package for A42MX09 device (SAR 69776)

## 1.4 Revision 12.0

The following is a summary of the changes in revision 12.0 of this document.

- Added information on power-up behavior for A42MX24 and A42MX36 devices to the Power Supply, page 13 (SAR 42096
- Corrected the inadvertent mistake in the naming of the PL68 pin assignment table (SARs 48999, 49793)

## 1.5 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- The FuseLock logo and accompanying text was removed from the User Security, page 12. This marking is no longer used on Microsemi devices (PCN 0915)
- The Development Tool Support, page 19 was updated (SAR 38512)

## 1.6 Revision 10.0

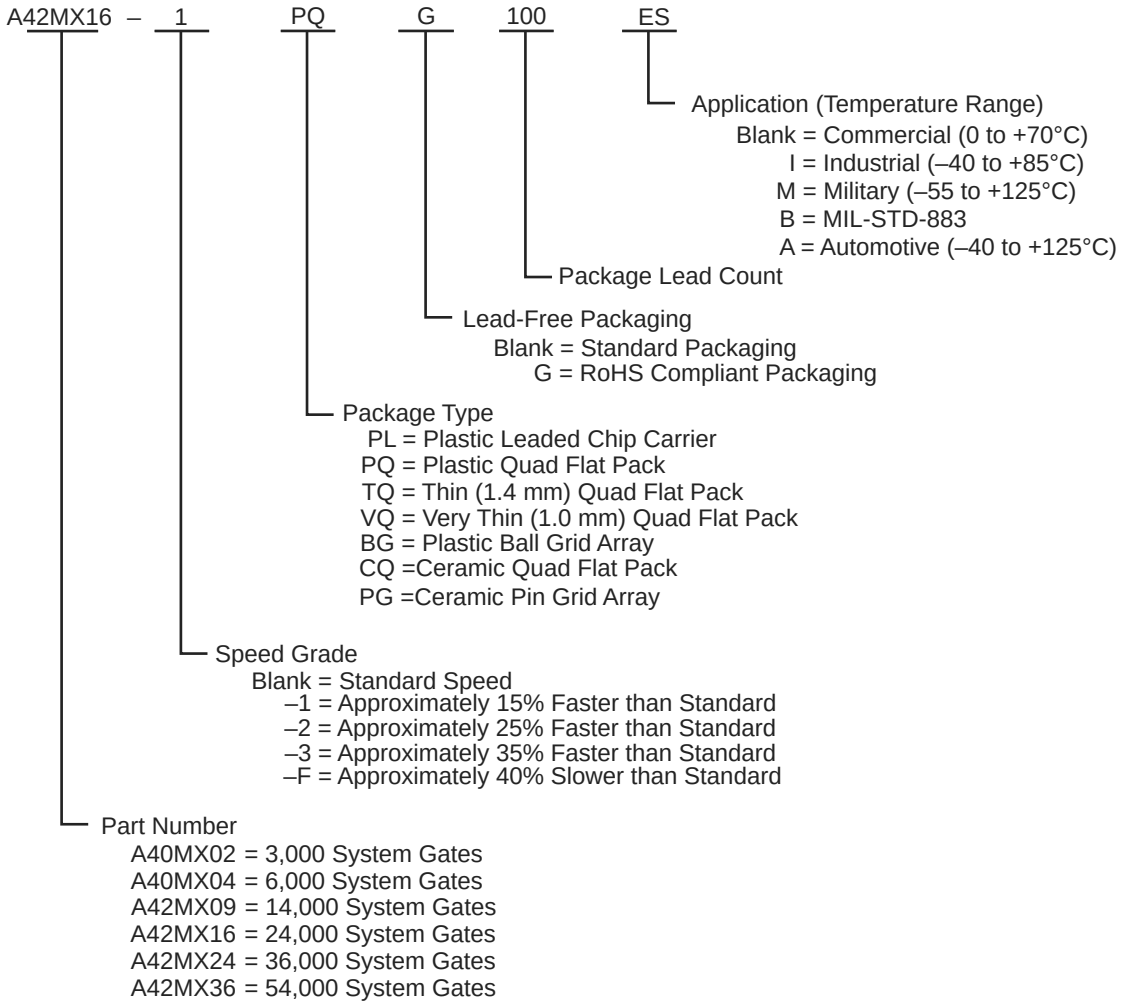
The following is a summary of the changes in revision 10.0 of this document.

- Ordering Information, page 3 was updated to include lead-free package ordering codes (SAR 21968)
- The User Security, page 12 was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34673)

## 2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

***Figure 1 •*** **Ordering Information**



## 2.4 Plastic Device Resources

***Table 2 •*** **Plastic Device Resources**

| | User I/Os | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Device** | **PLCC 44-Pin** | **PLCC 68-Pin** | **PLCC 84-Pin** | **PQFP 100-Pin** | **PQFP 144-Pin** | **PQFP 160-Pin** | **PQFP 208-Pin** | **PQFP 240-Pin** | **VQFP 80-Pin** | **VQFP 100-Pin** | **TQFP 176-Pin** | **PBGA 272-Pin** |
| A40MX02 | 34 | 57 | – | 57 | – | – | – | – | 57 | – | – | – |
| A40MX04 | 34 | 57 | 69 | 69 | – | – | – | – | 69 | – | – | – |
| A42MX09 | – | – | 72 | 83 | 95 | 101 | – | – | – | 83 | 104 | – |
| A42MX16 | – | – | 72 | 83 | – | 125 | 140 | – | – | 83 | 140 | – |
| A42MX24 | – | – | 72 | – | – | 125 | 176 | – | – | – | 150 | – |
| A42MX36 | – | – | – | – | – | – | 176 | 202 | – | – | – | 202 |

**Note: Package Definitions:** PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

## 2.5 Ceramic Device Resources

***Table 3 •*** **Ceramic Device Resources**

| | User I/Os | | | |
|---|---|---|---|---|
| **Device** | **CPGA 132-Pin** | **CQFP 172-Pin** | **CQFP 208-Pin** | **CQFP 256-Pin** |
| A42MX09 | 95 | | | |
| A42MX16 | | 131 | | |
| A42MX36 | | | 176 | 202 |

**Note: Package Definitions:** CQFP = Ceramic Quad Flat Pack

## 2.6 Temperature Grade Offerings

***Table 4 •*** **Temperature Grade Offerings**

| Package | A40MX02 | A40MX04 | A42MX09 | A42MX16 | A42MX24 | A42MX36 |
|---|---|---|---|---|---|---|
| PLCC 44 | C, I, M | C, I, M | | | | |
| PLCC 68 | C, I, A, M | C, I, M | | | | |
| PLCC 84 | | C, I, A, M | C, I, A, M | C, I, M | C, I, M | |
| PQFP 100 | C, I, A, M | C, I, A, M | C, I, A, M | C, I, M | | |
| PQFP 144 | | | C | | | |
| PQFP 160 | | | C, I, A, M | C, I, M | C, I, A, M | |
| PQFP 208 | | | | C, I, A, M | C, I, A, M | C, I, A, M |
| PQFP 240 | | | | | | C, I, A, M |
| VQFP 80 | C, I, A, M | C, I, A, M | | | | |
| VQFP 100 | | | C, I, A, M | C, I, A, M | | |
| TQFP 176 | | | C, I, A, M | C, I, A, M | C, I, A, M | |
| PBGA 272 | | | | | | C, I, M |
| CQFP 172 | | | | C, M, B | | |
| CQFP 208 | | | | | | C, M, B |
| CQFP 256 | | | | | | C, M, B |
| CPGA 132 | | | C, M, B | | | |

**Note:** C = Commercial
I = Industrial
A = Automotive
M = Military
B = MIL-STD-883 Class B

## 2.7 Speed Grade Offerings

***Table 5 •*** **Speed Grade Offerings**

| | – F | Std | –1 | –2 | –3 |
|---|---|---|---|---|---|
| C | P | P | P | P | P |
| I | | P | P | P | P |
| A | | P | | | |
| M | | P | P | | |
| B | | P | P | | |

**Note:** See the 40MX and 42MX Automotive Family FPGAs datasheet for details on automotive-grade MX offerings.

Contact your local *Microsemi Sales representative* for device availability.

# 3 40MX and 42MX FPGAs

## 3.1 General Description

Microsemi's 40MX and 42MX families offer a cost-effective design solution at 5V. The MX devices are single-chip solutions and provide high performance while shortening the system design and development cycle. MX devices can integrate and consolidate logic implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Microsemi's patented antifuse technology implemented in a 0.45µm triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the MX devices provide performance up to 250 MHz, are live on power-up and have one-fifth the standby power consumption of comparable FPGAs. MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

A42MX24 and A42MX36 devices also feature multiPlex I/Os, which support mixed-voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode. The devices are fully compliant with the PCI local bus specification (version 2.1). They deliver 200 MHz on-chip operation and 6.1 ns clock-to-output performance.

The 42MX24 and 42MX36 devices include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing and fast wide-decode modules. In addition, the A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The storage elements can efficiently address applications requiring wide data path manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All MX devices are fully tested over automotive and military temperature ranges. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin-compatible.

## 3.2 MX Architectural Overview

The MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources and clock networks, which are the building blocks for fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM modules, which are optimized for high-speed data path functions such as FIFOs, LIFOs and scratch pad memory. A42MX24 and A42MX36 also contain wide-decode modules.

### 3.2.1 Logic Modules

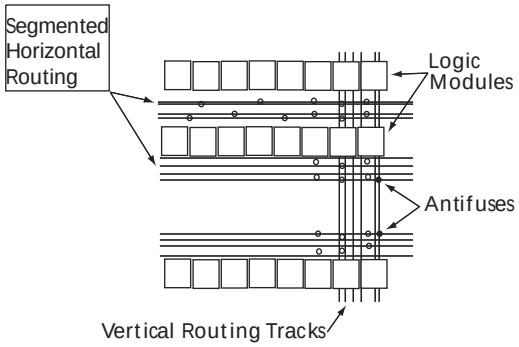
The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources.(see the following figure).

The logic module can implement the four basic logic functions (NAND, AND, OR and NOR) in gates of two, three, or four inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array; latches and flip-flops can be constructed from logic modules whenever required in the application.

#### 3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

***Figure 7 •*** **MX Routing Structure**




### 3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

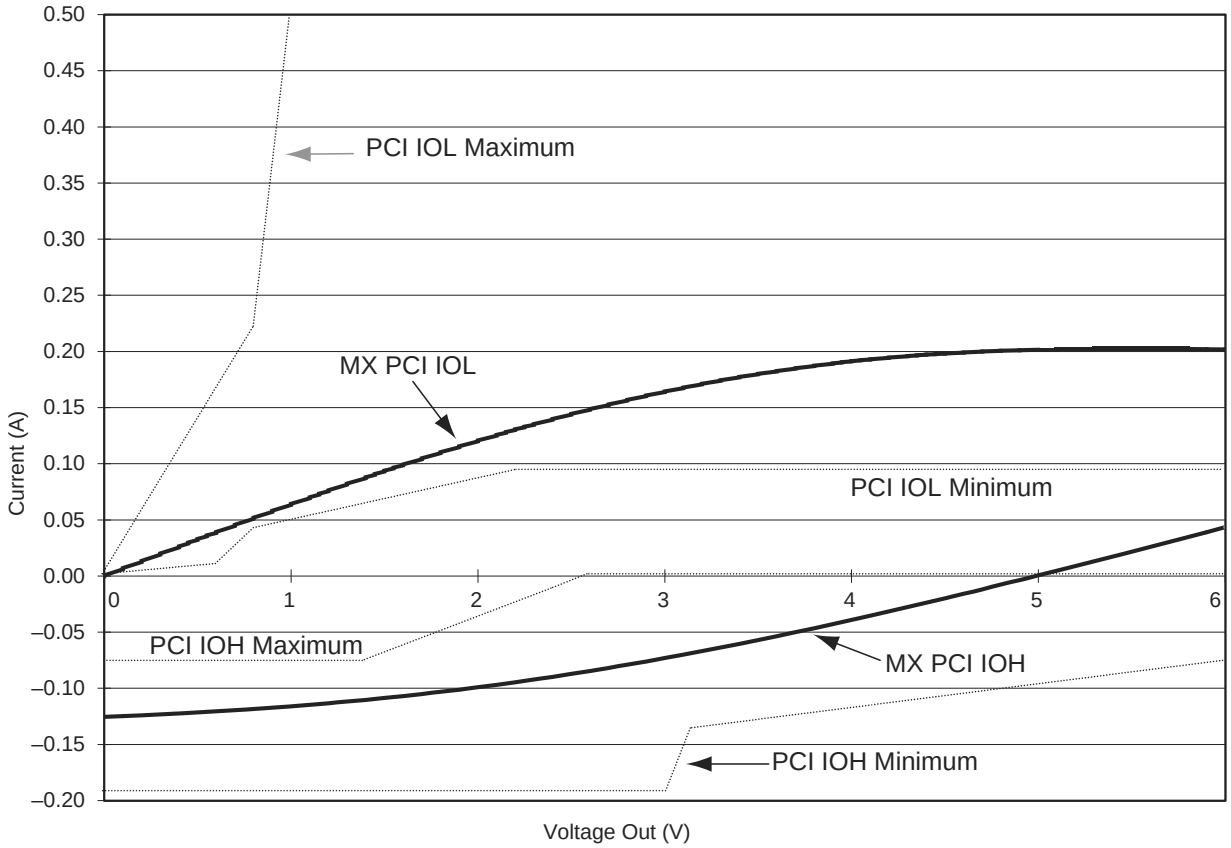
- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

***Figure 16 •*** **Typical Output Drive Characteristics (Based Upon Measured Data)**




## 3.9.4 Junction Temperature ($T_J$)

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. The following equation can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

**EQ 4**

where:

- $T_a$ = Ambient Temperature
- $\Delta T$ = Temperature gradient between junction (silicon) and ambient
- $\Delta T = \theta_{ja} * P$ (2)
- P = Power
- $\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in Table 27, page 29.

## 3.9.5 Package Thermal Characteristics

The device junction-to-case thermal characteristic is $\theta_{jc}$, and the junction-to-ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates.

The maximum junction temperature is 150°C.

Maximum power dissipation for commercial- and industrial-grade devices is a function of $\theta_{ja}$.

***Table 33 •*** **Timing Parameters for 33 MHz PCI**

| | | PCI | | A42MX24 | | A42MX36 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{SU(PTP)}$ | Input Set-Up Time to CLK—Point-to-Point | 10, 12[2] | – | 1.5 | – | 1.5 | – | ns |
| $t_H$ | Input Hold to CLK | 0 | – | 0 | – | 0 | – | ns |

1. TOFF is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.
2. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than do bussed signals. GNT# has a setup of 10; REW# has a setup of 12.

### 3.11.6.1 Timing Characteristics

The following tables list the timing characteristics.

***Table 34 •*** **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.2 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 2.7 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.2 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.2 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.2 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.8 | | 2.1 | | 2.4 | | 2.8 | | 3.9 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 2.3 | | 2.7 | | 3.0 | | 3.6 | | 5.0 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.9 | | 3.3 | | 3.7 | | 4.4 | | 6.1 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 4.9 | | 5.7 | | 6.5 | | 7.6 | | 10.6 | ns |
| **Logic Module Sequential Timing[2]** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| $t_{HD}$[3] | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 3.1 | | 3.5 | | 4.0 | | 4.7 | | 6.6 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.3 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 3.3 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 4.8 | | 5.6 | | 6.3 | | 7.5 | | 10.4 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency (FO = 128) | | 181 | | 168 | | 154 | | 134 | | 80 | MHz |

***Table 34 •*** **A40MX02 Timing Characteristics (Nominal 5.0 V Operation) *(continued)***
**(Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.3 | | 3.8 | | 4.3 | | 5.1 | | 7.2 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.0 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.3 | | 4.9 | | 5.8 | | 8.0 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.7 | | 5.4 | | 6.1 | | 7.2 | | 10.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.1 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| **CMOS Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.9 | | 4.5 | | 5.1 | | 6.05 | | 8.5 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.4 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.9 | | 5.6 | | 6.4 | | 7.5 | | 10.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 7.9 | | 9.1 | | 10.4 | | 12.2 | | 17.0 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.9 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.03 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35pF loading

***Table 35 •*** **A40MX02 Timing Characteristics (Nominal 3.3 V Operation)**
**(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{PD2}$ | Dual-Module Macros | | 3.7 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.7 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| **Logic Module Predicted Routing Delays[1]** | | | | | | | | | | | | |

***Table 44 •*** **A42MX36 Timing Characteristics (Nominal 5.0 V Operation)(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Combinatorial Functions[1]** | | | | | | | | | | | | |
| $t_{PD}$ | Internal Array Module Delay | | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{PDD}$ | Internal Decode Module Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.3 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 2.0 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{RD3}$ | FO =3 Routing Delay | | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{RD5}$ | FO = 8 Routing Delay | | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.3 | | 0.3 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.2 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.3 | | 3.7 | | 4.2 | | 4.9 | | 6.9 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.4 | | 4.8 | | 5.5 | | 6.4 | | 9.0 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{WC}$ | Write Cycle Time | 6.8 | | 7.5 | | 8.5 | | 10.0 | | 14.0 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 1.6 | | 1.8 | | 2.0 | | 2.4 | | 3.4 | | ns |
| **Synchronous SRAM Operations (continued)** | | | | | | | | | | | | |
| $t_{ADH}$ | Address/Data Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RENSU}$ | Read Enable Set-Up | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.3 | | ns |
| $t_{RENH}$ | Read Enable Hold | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |
| $t_{WENSU}$ | Write Enable Set-Up | 2.7 | | 3.0 | | 3.4 | | 4.0 | | 5.6 | | ns |
| $t_{WENH}$ | Write Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{BENS}$ | Block Enable Set-Up | 2.8 | | 3.1 | | 3.5 | | 4.1 | | 5.7 | | ns |
| $t_{BENH}$ | Block Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |

***Table 49 •*** **PL84**

| **PL84** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 47 | I/O | I/O | I/O | WD, I/O |
| 48 | I/O | I/O | I/O | I/O |
| 49 | I/O | GND | GND | GND |
| 50 | I/O | I/O | I/O | WD, I/O |
| 51 | I/O | I/O | I/O | WD, I/O |
| 52 | I/O | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 53 | I/O | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | GND | I/O | I/O | I/O |
| 61 | GND | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | TCK, I/O |
| 63 | I/O | LP | LP | LP |
| 64 | CLK, I/O | VCCA | VCCA | VCCA |
| 65 | I/O | VCCI | VCCI | VCCI |
| 66 | MODE | I/O | I/O | I/O |
| 67 | VCC | I/O | I/O | I/O |
| 68 | VCC | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O | I/O |
| 70 | I/O | GND | GND | GND |
| 71 | I/O | I/O | I/O | I/O |
| 72 | SDI, I/O | I/O | I/O | I/O |
| 73 | DCLK, I/O | I/O | I/O | I/O |
| 74 | PRA, I/O | I/O | I/O | I/O |
| 75 | PRB, I/O | I/O | I/O | I/O |
| 76 | I/O | SDI, I/O | SDI, I/O | SDI, I/O |
| 77 | I/O | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O | WD, I/O |
| 79 | I/O | I/O | I/O | WD, I/O |
| 80 | I/O | I/O | I/O | WD, I/O |
| 81 | I/O | PRA, I/O | PRA, I/O | PRA, I/O |
| 82 | GND | I/O | I/O | I/O |
| 83 | I/O | CLKA, I/O | CLKA, I/O | CLKA, I/O |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 95 | NC | I/O | I/O |
| 96 | NC | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | VCCI | VCCI | VCCI |
| 99 | I/O | I/O | I/O |
| 100 | I/O | WD, I/O | WD, I/O |
| 101 | I/O | WD, I/O | WD, I/O |
| 102 | I/O | I/O | I/O |
| 103 | SDO, I/O | SDO, TDO, I/O | SDO, TDO, I/O |
| 104 | I/O | I/O | I/O |
| 105 | GND | GND | GND |
| 106 | NC | VCCA | VCCA |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |
| 109 | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | NC | I/O | I/O |
| 113 | NC | I/O | I/O |
| 114 | NC | I/O | I/O |
| 115 | NC | I/O | I/O |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | I/O | I/O | I/O |
| 126 | GND | GND | GND |
| 127 | I/O | I/O | I/O |
| 128 | I/O | TCK, I/O | TCK, I/O |
| 129 | LP | LP | LP |
| 130 | VCCA | VCCA | VCCA |
| 131 | GND | GND | GND |

***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 57 | I/O | I/O |
| 58 | I/O | I/O |
| 59 | I/O | I/O |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | LP | LP |
| 63 | VCCA | VCCA |
| 64 | VCCI | VCCI |
| 65 | VCCA | VCCA |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | I/O | I/O |
| 69 | I/O | I/O |
| 70 | GND | GND |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | I/O | I/O |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | SDI, I/O | SDI, I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | GND | GND |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | PRA, I/O | PRA, I/O |
| 86 | I/O | I/O |
| 87 | CLKA, I/O | CLKA, I/O |
| 88 | VCCA | VCCA |
| 89 | I/O | I/O |
| 90 | CLKB, I/O | CLKB, I/O |
| 91 | I/O | I/O |
| 92 | PRB, I/O | PRB, I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | VCCA |
| 27 | I/O |
| 28 | I/O |
| 29 | VCCA |
| 30 | VCCI |
| 31 | GND |
| 32 | VCCA |
| 33 | LP |
| 34 | TCK, I/O |
| 35 | I/O |
| 36 | GND |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | GND |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 170 | VCCA |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | I/O |
| 177 | I/O |
| 178 | I/O |
| 179 | I/O |
| 180 | GND |
| 181 | I/O |
| 182 | I/O |
| 183 | I/O |
| 184 | I/O |
| 185 | I/O |
| 186 | I/O |
| 187 | I/O |
| 188 | MODE |
| 189 | VCCA |
| 190 | GND |
| 191 | NC |
| 192 | NC |
| 193 | NC |
| 194 | I/O |
| 195 | DCLK, I/O |
| 196 | I/O |
| 197 | I/O |
| 198 | I/O |
| 199 | WD, I/O |
| 200 | WD, I/O |
| 201 | VCCI |
| 202 | I/O |
| 203 | I/O |
| 204 | I/O |
| 205 | I/O |
| 206 | GND |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| C3 | GND |
| C4 | I/O |
| C5 | WD, I/O |
| C6 | I/O |
| C7 | QCLKC, I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | CLKB |
| C11 | PRA, I/O |
| C12 | WD, I/O |
| C13 | I/O |
| C14 | QCLKD, I/O |
| C15 | I/O |
| C16 | WD, I/O |
| C17 | SDI, I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| D1 | I/O |
| D2 | I/O |
| D3 | I/O |
| D4 | I/O |
| D5 | VCCI |
| D6 | I/O |
| D7 | I/O |
| D8 | VCCA |
| D9 | WD, I/O |
| D10 | VCCI |
| D11 | I/O |
| D12 | VCCI |
| D13 | I/O |
| D14 | VCCI |
| D15 | I/O |
| D16 | VCCA |
| D17 | GND |
| D18 | I/O |
| D19 | I/O |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M17 | I/O |
| M18 | I/O |
| M19 | I/O |
| M20 | I/O |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | VCCI |
| N17 | VCCI |
| N18 | I/O |
| N19 | I/O |
| N20 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | VCCA |
| P17 | I/O |
| P18 | I/O |
| P19 | I/O |
| P20 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | VCCI |
| R17 | VCCI |
| R18 | I/O |
| R19 | I/O |
| R20 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T17 | VCCA |
| T18 | I/O |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |

***Figure 53 •*** **CQ172**

***Table 62 •*** **CQ172**

| **CQ172** | |
|---|---|
| **Pin Number** | **A42MX16 Function** |
| 1 | MODE |
| 2 | I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | GND |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | VCC |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | GND |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |