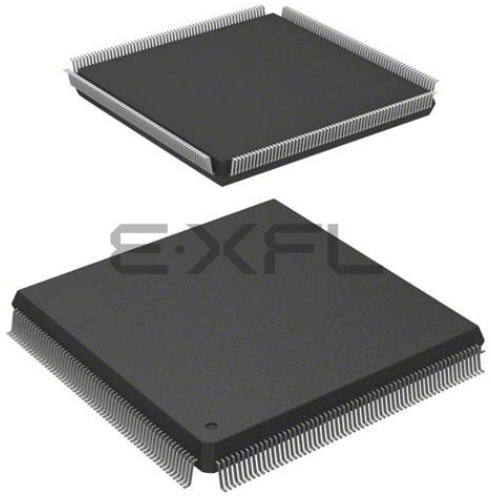

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

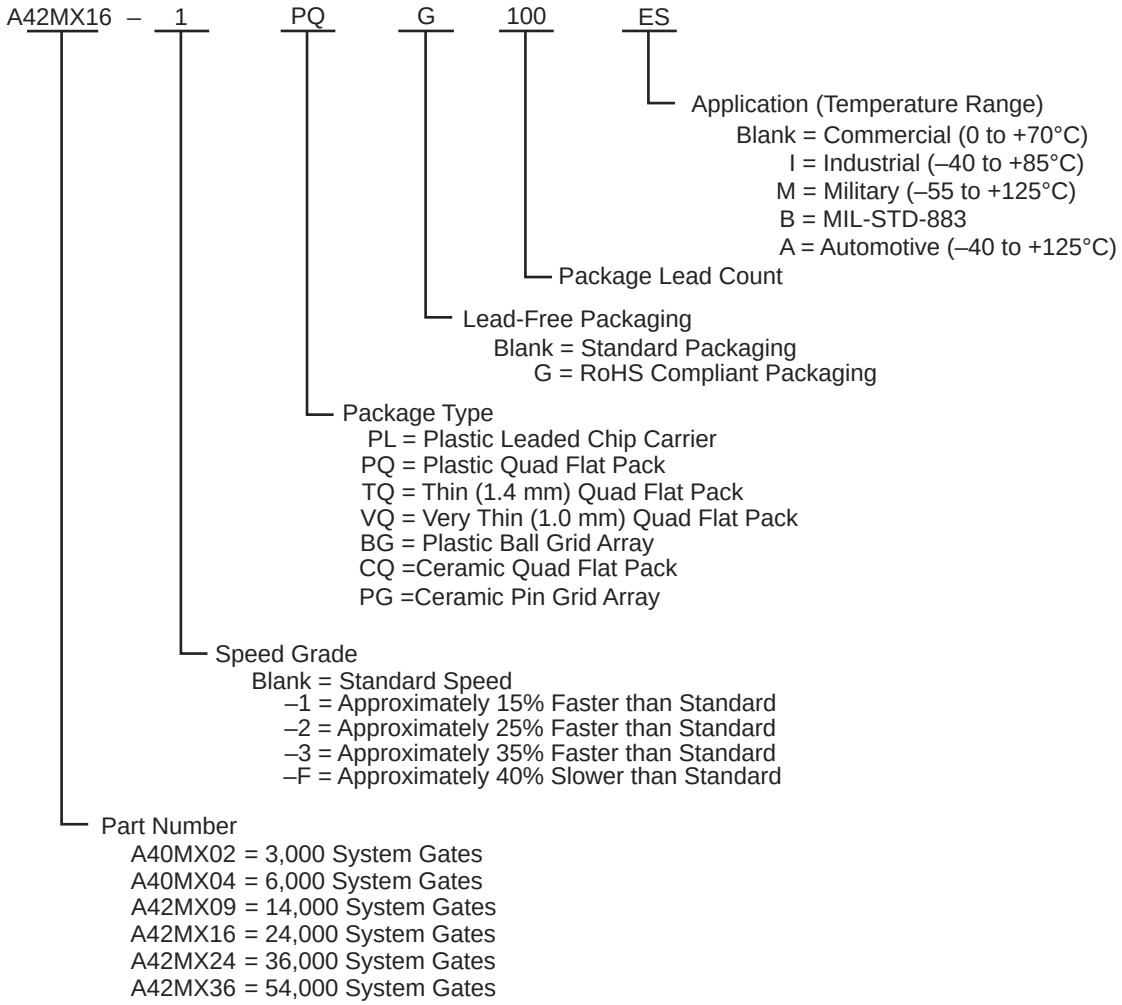
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 2560 |
| Number of I/O | 202 |
| Number of Gates | 54000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a42mx36-2pq240i |

## 2.3 Ordering Information

The following figure shows ordering information.All the following tables show plastic and ceramic device resources, temperature and speed grade offerings.

***Figure 1 •*** **Ordering Information**



- VCCA = Power supply in volts (V)
- F = Switching frequency in megahertz (MHz)

### 3.4.4 Equivalent Capacitance

Equivalent capacitance is calculated by measuring ICCactive at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

### 3.4.5 $C_{EQ}$ Values for Microsemi MX FPGAs

Modules ($C_{EQM}$)3.5

Input Buffers ($C_{EQI}$)6.9

Output Buffers ($C_{EQO}$)18.2

Routed Array Clock Buffer Loads ($C_{EQCR}$)1.4

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\text{Power} = VCCA^2 * [(m \times C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} +$$
$$0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} +$$
$$0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} (2)]$$

**EQ 3**

where:

m = Number of logic modules switching at frequency $f_m$

n = Number of input buffers switching at frequency $f_n$

p = Number of output buffers switching at frequency $f_p$

$q_1$ = Number of clock loads on the first routed array clock

$q_2$ = Number of clock loads on the second routed array clock

$r_1$ = Fixed capacitance due to first routed array clock

$r_2$ = Fixed capacitance due to second routed array clock

$C_{EQM}$ = Equivalent capacitance of logic modules in pF

$C_{EQI}$ = Equivalent capacitance of input buffers in pF

$C_{EQO}$ = Equivalent capacitance of output buffers in pF

$C_{EQCR}$ = Equivalent capacitance of routed array clock in pF

$C_L$ = Output load capacitance in pF

$f_m$ = Average logic module switching rate in MHz

$f_n$ = Average input buffer switching rate in MHz

$f_p$ = Average output buffer switching rate in MHz

$f_{q1}$ = Average first routed array clock rate in MHz

approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, shown in Table 34, page 41.

## 3.11.3 Timing Derating

MX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature and worst-case processing.

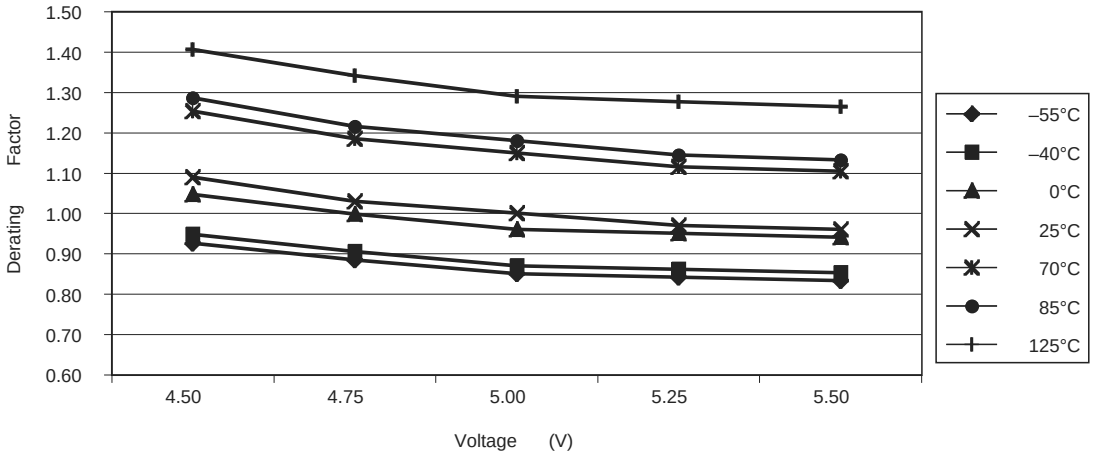
## 3.11.4 Temperature and Voltage Derating Factors

The following tables and figures show temperature and voltage derating factors for 40MX and 42MX FPGAs.

***Table 28 •*** **42MX Temperature and Voltage Derating Factors (Normalized to $T_J$ = 25°C, VCCA = 5.0 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **42MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| **4.50** | 0.93 | 0.95 | 1.05 | 1.09 | 1.25 | 1.29 | 1.41 |
| **4.75** | 0.88 | 0.90 | 1.00 | 1.03 | 1.18 | 1.22 | 1.34 |
| **5.00** | 0.85 | 0.87 | 0.96 | 1.00 | 1.15 | 1.18 | 1.29 |
| **5.25** | 0.84 | 0.86 | 0.95 | 0.97 | 1.12 | 1.14 | 1.28 |
| **5.50** | 0.83 | 0.85 | 0.94 | 0.96 | 1.10 | 1.13 | 1.26 |

***Figure 34 •*** **42MX Junction Temperature and Voltage Derating Curves (Normalized to TJ = 25°C, VCCA = 5.0 V)**




**Note:** This derating factor applies to all routing and propagation delays

***Table 29 •*** **40MX Temperature and Voltage Derating Factors(Normalized to TJ = 25°C, VCC = 5.0 V)**

| | Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **40MX Voltage** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 4.50 | 0.89 | 0.93 | 1.02 | 1.09 | 1.25 | 1.31 | 1.45 |
| 4.75 | 0.84 | 0.88 | 0.97 | 1.03 | 1.18 | 1.24 | 1.37 |
| 5.00 | 0.82 | 0.85 | 0.94 | 1.00 | 1.15 | 1.20 | 1.33 |
| 5.25 | 0.80 | 0.82 | 0.91 | 0.97 | 1.12 | 1.16 | 1.29 |
| 5.50 | 0.79 | 0.82 | 0.90 | 0.96 | 1.10 | 1.15 | 1.28 |

***Table 37 •*** **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.3 | | 5.6 | | 7.0 | | 9.8 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.6 | | 5.3 | | 5.6 | | 7.0 | | 9.8 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 6.8 | | 7.8 | | 8.9 | | 10.4 | | 14.6 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency (FO = 128) | | 109 | | 101 | | 92 | | 80 | | 48 | MHz |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INYH}$ | Pad-to-Y HIGH | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INYL}$ | Pad-to-Y LOW | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.9 | ns |

***Table 37 •*** **A40MX04 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCC = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **CMOS Output Module Timing[4]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 5.5 | | 6.4 | | 7.2 | | 8.5 | | 11.9 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.8 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 4.7 | | 5.5 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 6.8 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 11.1 | | 12.8 | | 14.5 | | 17.1 | | 23.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 8.2 | | 9.5 | | 10.7 | | 12.6 | | 17.7 | ns |
| $d_{TLH}$ | Delta LOW to HIGH | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Delta HIGH to LOW | | 0.03 | | 0.03 | | 0.04 | | 0.04 | | 0.06 | ns/pF |

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Timer tool from the Designer software to check the hold time for this macro.
4. Delays based on 35 pF loading.

***Table 38 •*** **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays[1]** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.2 | | 1.3 | | 1.5 | | 1.8 | | 2.5 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.7 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.6 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.2 | | 1.6 | | 1.8 | | 2.1 | | 2.9 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 0.9 | | 1.0 | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.2 | | 1.3 | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.4 | | 1.5 | | 1.7 | | 2.0 | | 2.9 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.3 | | 2.6 | | 2.9 | | 3.4 | | 4.8 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Set-Up | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.4 | | 0.5 | | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 3.4 | | 3.8 | | 4.3 | | 5.0 | | 7.0 | | ns |

***Table 38 •*** **A42MX09 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter / Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 2.5 | | 2.7 | | 3.1 | | 3.6 | | 5.1 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 2.9 | | 3.2 | | 3.6 | | 4.3 | | 6.0 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 2.6 | | 2.9 | | 3.3 | | 3.9 | | 5.5 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 2.9 | | 3.2 | | 3.7 | | 4.3 | | 6.1 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 4.9 | | 5.4 | | 6.2 | | 7.3 | | 10.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 5.3 | | 5.9 | | 6.7 | | 7.9 | | 11.1 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 2.6 | | 2.9 | | 3.3 | | 3.8 | | 5.3 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 2.6 | | 2.9 | | 3.3 | | 3.8 | | 5.3 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 5.2 | | 5.8 | | 6.6 | | 7.7 | | 10.8 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 7.4 | | 8.2 | | 9.3 | | 10.9 | | 15.3 | ns |
| $d_{TLH}$ | Capacity Loading, LOW to HIGH | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.06 | ns/pF |
| $d_{THL}$ | Capacity Loading, HIGH to LOW | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

***Table 39 •*** **A42MX09 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | 3.4 | | 3.8 | | 5.5 | | 6.4 | | 9.0 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | 4.1 | | 4.5 | | 4.2 | | 5.0 | | 7.0 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | 3.7 | | 4.1 | | 4.6 | | 5.5 | | 7.6 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | 4.1 | | 4.5 | | 5.1 | | 6.1 | | 8.5 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | 6.9 | | 7.6 | | 8.6 | | 10.2 | | 14.2 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | 7.5 | | 8.3 | | 9.4 | | 11.1 | | 15.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | 5.8 | | 6.5 | | 7.3 | | 8.6 | | 12.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | 5.8 | | 6.5 | | 7.3 | | 8.6 | | 12.0 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 8.7 | | 9.7 | | 10.9 | | 12.9 | | 18.0 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | 12.2 | | 13.5 | | 15.4 | | 18.1 | | 25.3 | ns |
| $d_{TLH}$ | Capacity Loading, LOW to HIGH | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{THL}$ | Capacity Loading, HIGH to LOW | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *Delays based on 35 pF loading.*

***Table 40 •*** **A42MX16 Timing Characteristics (Nominal 5.0 V Operation) (Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Propagation Delays[1]** | | | | | | | | | | | | |
| $t_{PD1}$ | Single Module | | 1.4 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{CO}$ | Sequential Clock-to-Q | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 3.0 | ns |
| $t_{GO}$ | Latch G-to-Q | | 1.4 | | 1.5 | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset-to-Q | | 1.6 | | 1.7 | | 2.0 | | 2.3 | | 3.3 | ns |
| **Logic Module Predicted Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | | 1.6 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.0 | | 1.2 | | 1.3 | | 1.5 | | 2.1 | ns |

***Table 45 •*** **A42MX36 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RD5}$ | FO = 8 Routing Delay | | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | ns |
| $t_{RDD}$ | Decode-to-Output Routing Delay | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | ns |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 1.0 | | 1.1 | | 1.2 | | 1.4 | | 2.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Synchronous SRAM Operations** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 9.5 | | 10.5 | | 11.9 | | 14.0 | | 19.6 | | ns |
| $t_{WC}$ | Write Cycle Time | 9.5 | | 10.5 | | 11.9 | | 14.0 | | 19.6 | | ns |
| $t_{RCKHL}$ | Clock HIGH/LOW Time | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | | ns |
| $t_{RCO}$ | Data Valid After Clock HIGH/LOW | | 4.8 | | 5.3 | | 6.0 | | 7.0 | | 9.8 | ns |
| $t_{ADSU}$ | Address/Data Set-Up Time | 2.3 | | 2.5 | | 2.8 | | 3.4 | | 4.8 | | ns |

***Figure 39 •*** **PL68**

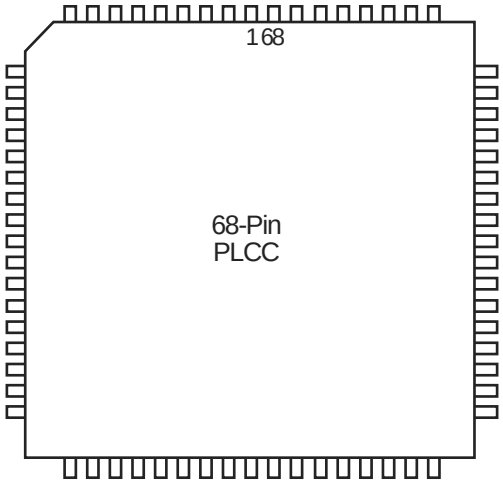



***Table 48 •*** **PL68**

| **PL68** | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 1 | I/O | I/O |
| 2 | I/O | I/O |
| 3 | I/O | I/O |
| 4 | VCC | VCC |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | I/O | I/O |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | GND | GND |
| 15 | GND | GND |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | I/O | I/O |
| 21 | VCC | VCC |
| 22 | I/O | I/O |
| 23 | I/O | I/O |

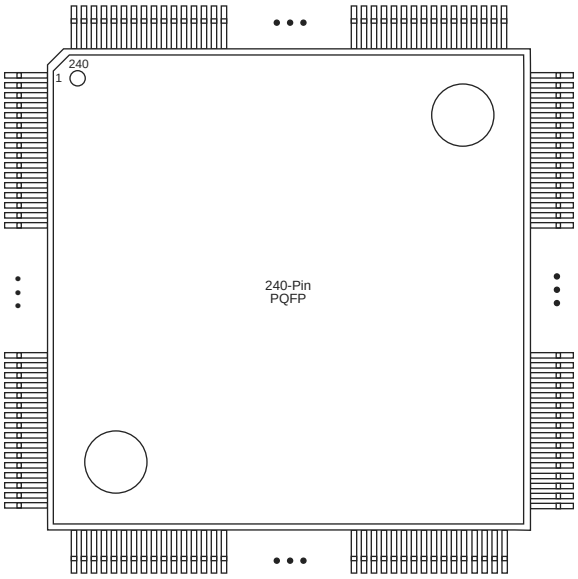
***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 58 | I/O | WD, I/O | WD, I/O |
| 59 | I/O | I/O | I/O |
| 60 | VCCI | VCCI | VCCI |
| 61 | NC | I/O | I/O |
| 62 | NC | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | QCLKA, I/O |
| 66 | I/O | WD, I/O | WD, I/O |
| 67 | NC | WD, I/O | WD, I/O |
| 68 | NC | I/O | I/O |
| 69 | I/O | I/O | I/O |
| 70 | I/O | WD, I/O | WD, I/O |
| 71 | I/O | WD, I/O | WD, I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | GND | GND | GND |
| 79 | VCCA | VCCA | VCCA |
| 80 | NC | VCCI | VCCI |
| 81 | I/O | I/O | I/O |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | WD, I/O | WD, I/O |
| 86 | I/O | WD, I/O | WD, I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | NC | I/O | I/O |
| 90 | NC | I/O | I/O |
| 91 | I/O | I/O | QCLKB, I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | WD, I/O | WD, I/O |
| 94 | I/O | WD, I/O | WD, I/O |

***Table 53 •*** **PQ208**

| PQ208 | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 206 | I/O | I/O | I/O |
| 207 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 208 | I/O | I/O | I/O |

***Figure 45 •*** **PQ240**




**Note:** This figure shows the 240-Pin PQFP Package top view.

***Table 54 •*** **PQ240**

| PQ240 | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | I/O |
| 2 | DCLK, I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | WD, I/O |
| 7 | WD, I/O |
| 8 | VCCI |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 47 | I/O | I/O | TDI, I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | WD, I/O |
| 50 | I/O | I/O | WD, I/O |
| 51 | I/O | I/O | I/O |
| 52 | NC | VCCI | VCCI |
| 53 | I/O | I/O | I/O |
| 54 | NC | I/O | I/O |
| 55 | NC | I/O | WD, I/O |
| 56 | I/O | I/O | WD, I/O |
| 57 | NC | NC | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | WD, I/O |
| 60 | I/O | I/O | WD, I/O |
| 61 | NC | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | NC | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | NC | I/O | I/O |
| 67 | GND | GND | GND |
| 68 | VCCA | VCCA | VCCA |
| 69 | I/O | I/O | WD, I/O |
| 70 | I/O | I/O | WD, I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | NC | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | NC | NC | WD, I/O |
| 78 | NC | I/O | WD, I/O |
| 79 | I/O | I/O | I/O |
| 80 | NC | I/O | I/O |
| 81 | I/O | I/O | I/O |
| 82 | NC | VCCI | VCCI |
| 83 | I/O | I/O | I/O |

***Table 57 •*** **TQ176**

| **TQ176** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** | **A42MX24 Function** |
| 84 | I/O | I/O | WD, I/O |
| 85 | I/O | I/O | WD, I/O |
| 86 | NC | I/O | I/O |
| 87 | SDO, I/O | SDO, I/O | SDO, TDO, I/O |
| 88 | I/O | I/O | I/O |
| 89 | GND | GND | GND |
| 90 | I/O | I/O | I/O |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | NC | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | I/O | I/O | I/O |
| 99 | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O |
| 101 | NC | NC | I/O |
| 102 | I/O | I/O | I/O |
| 103 | NC | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | GND | GND | GND |
| 107 | NC | I/O | I/O |
| 108 | NC | I/O | TCK, I/O |
| 109 | LP | LP | LP |
| 110 | VCCA | VCCA | VCCA |
| 111 | GND | GND | GND |
| 112 | VCCI | VCCI | VCCI |
| 113 | VCCA | VCCA | VCCA |
| 114 | NC | I/O | I/O |
| 115 | NC | I/O | I/O |
| 116 | NC | VCCA | VCCA |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |

***Table 58 •*** **CQ208**

| **CQ208** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 1 | GND |
| 2 | VCCA |
| 3 | MODE |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | I/O |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | VCCA |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | GND |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | VCCI |
| 29 | VCCA |
| 30 | I/O |
| 31 | I/O |
| 32 | VCCA |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | VCCA |
| 27 | I/O |
| 28 | I/O |
| 29 | VCCA |
| 30 | VCCI |
| 31 | GND |
| 32 | VCCA |
| 33 | LP |
| 34 | TCK, I/O |
| 35 | I/O |
| 36 | GND |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | I/O |
| 41 | I/O |
| 42 | I/O |
| 43 | I/O |
| 44 | I/O |
| 45 | I/O |
| 46 | I/O |
| 47 | I/O |
| 48 | GND |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |

***Table 59 •*** **CQ256**

| **CQ256** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 170 | VCCA |
| 171 | I/O |
| 172 | I/O |
| 173 | I/O |
| 174 | I/O |
| 175 | I/O |
| 176 | I/O |
| 177 | I/O |
| 178 | I/O |
| 179 | I/O |
| 180 | GND |
| 181 | I/O |
| 182 | I/O |
| 183 | I/O |
| 184 | I/O |
| 185 | I/O |
| 186 | I/O |
| 187 | I/O |
| 188 | MODE |
| 189 | VCCA |
| 190 | GND |
| 191 | NC |
| 192 | NC |
| 193 | NC |
| 194 | I/O |
| 195 | DCLK, I/O |
| 196 | I/O |
| 197 | I/O |
| 198 | I/O |
| 199 | WD, I/O |
| 200 | WD, I/O |
| 201 | VCCI |
| 202 | I/O |
| 203 | I/O |
| 204 | I/O |
| 205 | I/O |
| 206 | GND |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| A6 | I/O |
| A7 | WD, I/O |
| A8 | WD, I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | CLKA |
| A12 | I/O |
| A13 | I/O |
| A14 | I/O |
| A15 | I/O |
| A16 | WD, I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | GND |
| A20 | GND |
| B1 | GND |
| B2 | GND |
| B3 | DCLK, I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | WD, I/O |
| B8 | I/O |
| B9 | PRB, I/O |
| B10 | I/O |
| B11 | I/O |
| B12 | WD, I/O |
| B13 | I/O |
| B14 | I/O |
| B15 | WD, I/O |
| B16 | I/O |
| B17 | WD, I/O |
| B18 | I/O |
| B19 | GND |
| B20 | GND |
| C1 | I/O |
| C2 | MODE |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | GND |
| J17 | VCCA |
| J18 | I/O |
| J19 | I/O |
| J20 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | VCCI |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K17 | I/O |
| K18 | VCCA |
| K19 | VCCA |
| K20 | LP |
| L1 | I/O |
| L2 | I/O |
| L3 | VCCA |
| L4 | VCCA |
| L9 | GND |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L17 | VCCI |
| L18 | I/O |
| L19 | I/O |
| L20 | TCK, I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | VCCI |
| M9 | GND |

***Table 60 •*** **BG272**

| **BG272** | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| Y13 | I/O |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | WD, I/O |
| Y19 | GND |
| Y20 | GND |

***Figure 52 •*** **PG132**

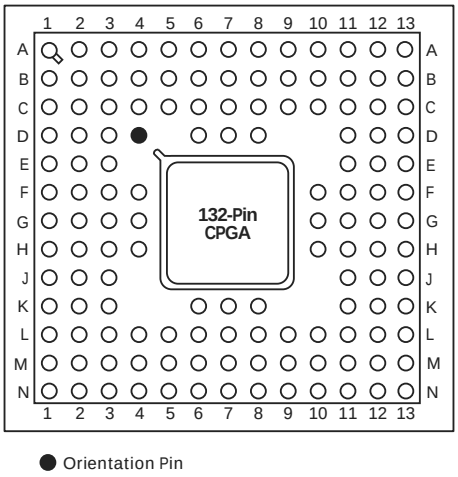



***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| – | PMPOUT |
| B2 | I/O |
| A1 | MODE |
| B1 | I/O |
| D3 | I/O |
| C2 | I/O |
| C1 | I/O |
| D2 | I/O |
| D1 | I/O |
| E2 | I/O |
| E1 | I/O |
| F3 | I/O |

***Figure 53 •*** **CQ172**

***Table 62 •*** **CQ172**

| **CQ172** | |
|---|---|
| **Pin Number** | **A42MX16 Function** |
| 1 | MODE |
| 2 | I/O |
| 3 | I/O |
| 4 | I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | GND |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | I/O |
| 12 | VCC |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | I/O |
| 17 | GND |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |