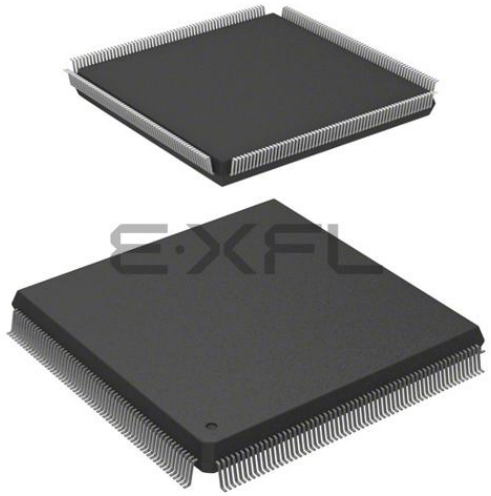

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 2560 |
| Number of I/O | 202 |
| Number of Gates | 54000 |
| Voltage - Supply | 3V ~ 3.6V, 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a42mx36-2pqg240i |

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## About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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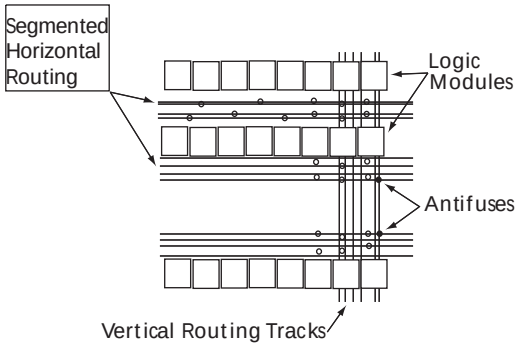
### 3.2.3.3 Antifuse Structures

An antifuse is a “normally open” structure. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. There are no pre-existing connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For instance, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

***Figure 7 •*** **MX Routing Structure**




## 3.2.4 Clock Networks

The 40MX devices have one global clock distribution network (CLK). A signal can be put on the CLK network by being routed through the CLKBUF buffer.

In 42MX devices, there are two low-skew, high-fanout clock distribution networks, referred to as CLKA and CLKB. Each network has a clock module (CLKMOD) that can select the source of the clock signal from any of the following (Figure 8, page 11):

- Externally from the CLKA pad, using CLKBUF buffer
- Externally from the CLKB pad, using CLKBUF buffer
- Internally from the CLKINTA input, using CLKINT buffer
- Internally from the CLKINTB input, using CLKINT buffer

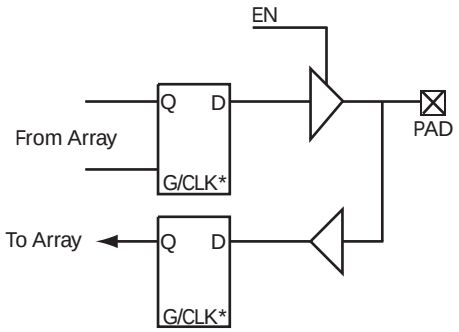
The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Clock input pads in both 40MX and 42MX devices can also be used as normal I/Os, bypassing the clock networks.

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 9, page 11). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

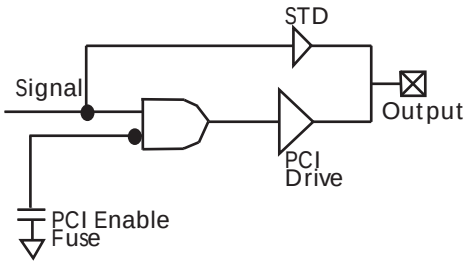
Designer software development tools provide a design library of I/O macro functions that can implement all I/O configurations supported by the MX FPGAs.

***Figure 10 •*** **42MX I/O Module**




***Note:*** **Can be configured as a Latch or D Flip-Flop (Using C-Module)*

***Figure 11 •*** **PCI Output Structure of A42MX24 and A42MX36 Devices**




# 3.3 Other Architectural Features

The following sections cover other architectural features of 40MX and 42MX FPGAs.

## 3.3.1 Performance

MX devices can operate with internal clock frequencies of 250 MHz, enabling fast execution of complex logic functions. MX devices are live on power-up and do not require auxiliary configuration devices and thus are an optimal platform to integrate the functionality contained in multiple programmable logic devices. In addition, designs that previously would have required a gate array to meet performance can be integrated into an MX device with improvements in cost and time-to-market. Using timing-driven place-and-route (TDPR) tools, designers can achieve highly deterministic device performance.

## 3.3.2 User Security

Microsemi FuseLock provides robust security against design theft. Special security fuses are hidden in the fabric of the device and protect against unauthorized users attempting to access the programming and/or probe interfaces. It is virtually impossible to identify or bypass these fuses without damaging the device, making Microsemi antifuse FPGAs protected with the highest level of security available from both invasive and noninvasive attacks.

Special security fuses in 40MX devices include the Probe Fuse and Program Fuse. The former disables the probing circuitry while the latter prohibits further programming of all fuses, including the Probe Fuse. In 42MX devices, there is the Security Fuse which, when programmed, both disables the probing circuitry and prohibits further programming of the device.

## 3.3.3 Programming

Device programming is supported through the Silicon Sculptor series of programmers. Silicon Sculptor is a compact, robust, single-site and multi-site device programmer for the PC. With standalone software, Silicon Sculptor is designed to allow concurrent programming of multiple units from the same PC.

reliability. Devices should not be operated outside the recommended operating conditions.

***Table 21 •*** **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| VCCA | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5 | V |
| VCCI | 3.14 to 3.47 | 3.0 to 3.6 | 3.0 to 3.6 | V |

**Note:** *Ambient temperature ($T_A$) is used for commercial and industrial grades; case temperature ($T_C$) is used for military grades.

A sample calculation of the absolute maximum power dissipation allowed for a TQ176 package at commercial temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{ja}(°(\text{C/W}))} = \frac{150°\text{C} - 70°\text{C}}{(28°\text{C})/\text{W}} = 2.86\text{W}$$

**EQ 5**

The maximum power dissipation for military-grade devices is a function of $\theta_{jc}$. A sample calculation of the absolute maximum power dissipation allowed for CQFP 208-pin package at military temperature and still air is given in the following equation

$$\text{MaximumPowerAllowed} = \frac{\text{Max} \cdot \text{junction temp} \cdot (°\text{C}) - \text{Max} \cdot \text{ambient temp} \cdot (°\text{C})}{\theta_{jc}(°(\text{C/W}))} = \frac{150°\text{C} - 125°\text{C}}{(6.3°\text{C})/\text{W}} = 3.97\text{W}$$

**EQ 6**

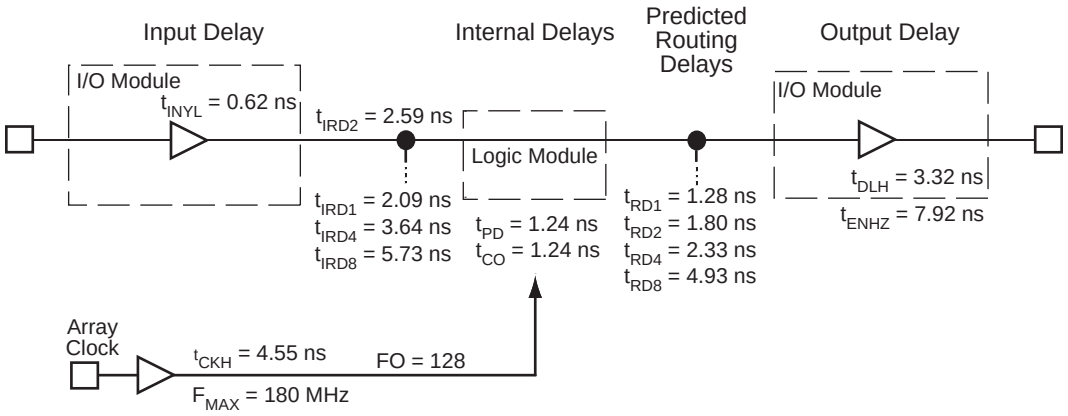
***Table 27 •*** **Package Thermal Characteristics**

| | | | $\theta_{ja}$ | | | |
|---|---|---|---|---|---|---|
| **Plastic Packages** | **Pin Count** | $\theta_{jc}$ | **Still Air** | **1.0 m/s 200 ft/min.** | **2.5 m/s 500 ft/min.** | **Units** |
| Plastic Quad Flat Pack | 100 | 12.0 | 27.8 | 23.4 | 21.2 | °C/W |
| Plastic Quad Flat Pack | 144 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 160 | 10.0 | 26.2 | 22.8 | 21.1 | °C/W |
| Plastic Quad Flat Pack | 208 | 8.0 | 26.1 | 22.5 | 20.8 | °C/W |
| Plastic Quad Flat Pack | 240 | 8.5 | 25.6 | 22.3 | 20.8 | °C/W |
| Plastic Leaded Chip Carrier | 44 | 16.0 | 20.0 | 24.5 | 22.0 | °C/W |
| Plastic Leaded Chip Carrier | 68 | 13.0 | 25.0 | 21.0 | 19.4 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12.0 | 22.5 | 18.9 | 17.6 | °C/W |
| Thin Plastic Quad Flat Pack | 176 | 11.0 | 24.7 | 19.9 | 18.0 | °C/W |
| Very Thin Plastic Quad Flat Pack | 80 | 12.0 | 38.2 | 31.9 | 29.4 | °C/W |
| Very Thin Plastic Quad Flat Pack | 100 | 10.0 | 35.3 | 29.4 | 27.1 | °C/W |
| Plastic Ball Grid Array | 272 | 3.0 | 18.3 | 14.9 | 13.9 | °C/W |
| **Ceramic Packages** | | | | | | |
| Ceramic Pin Grid Array | 132 | 4.8 | 25.0 | 20.6 | 18.7 | °C/W |
| Ceramic Quad Flat Pack | 208 | 2.0 | 22.0 | 19.8 | 18.0 | °C/W |
| Ceramic Quad Flat Pack | 256 | 2.0 | 20.0 | 16.5 | 15.0 | °C/W |

## 3.10 Timing Models

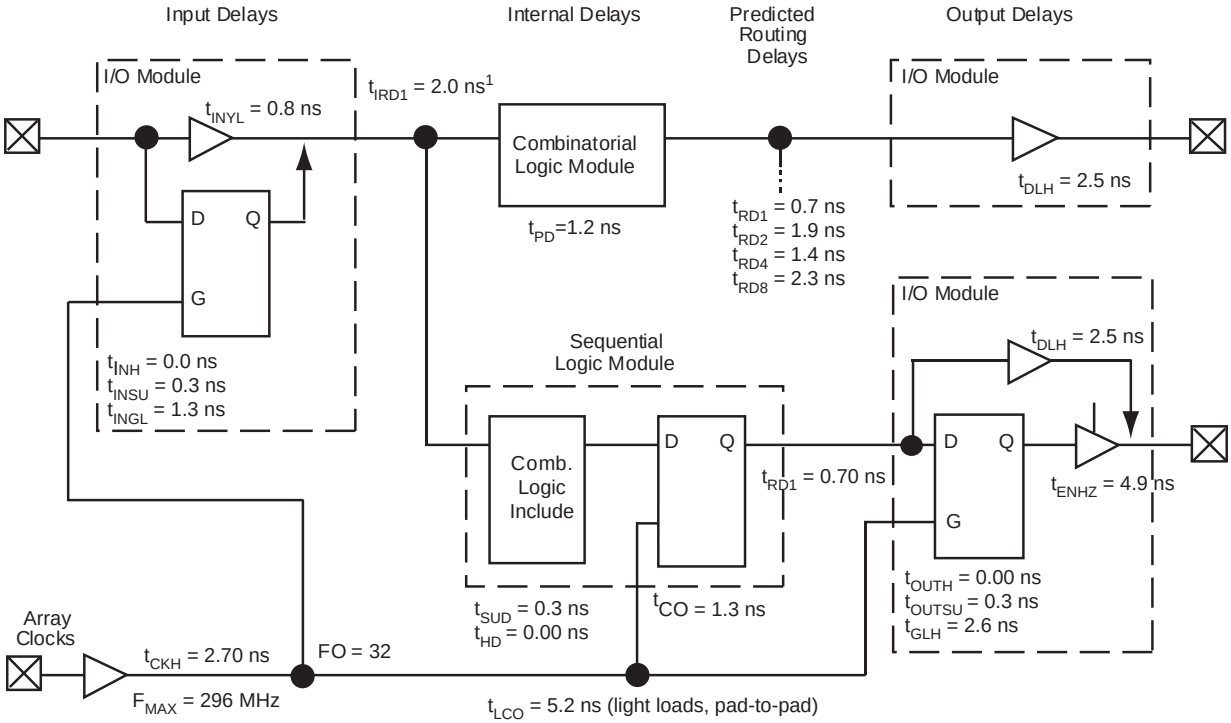
The following figures show various timing models.

***Figure 17 •*** **40MX Timing Model***




**Note:** Values are shown for 40MX –3 speed devices at 5.0 V worst-case commercial conditions.

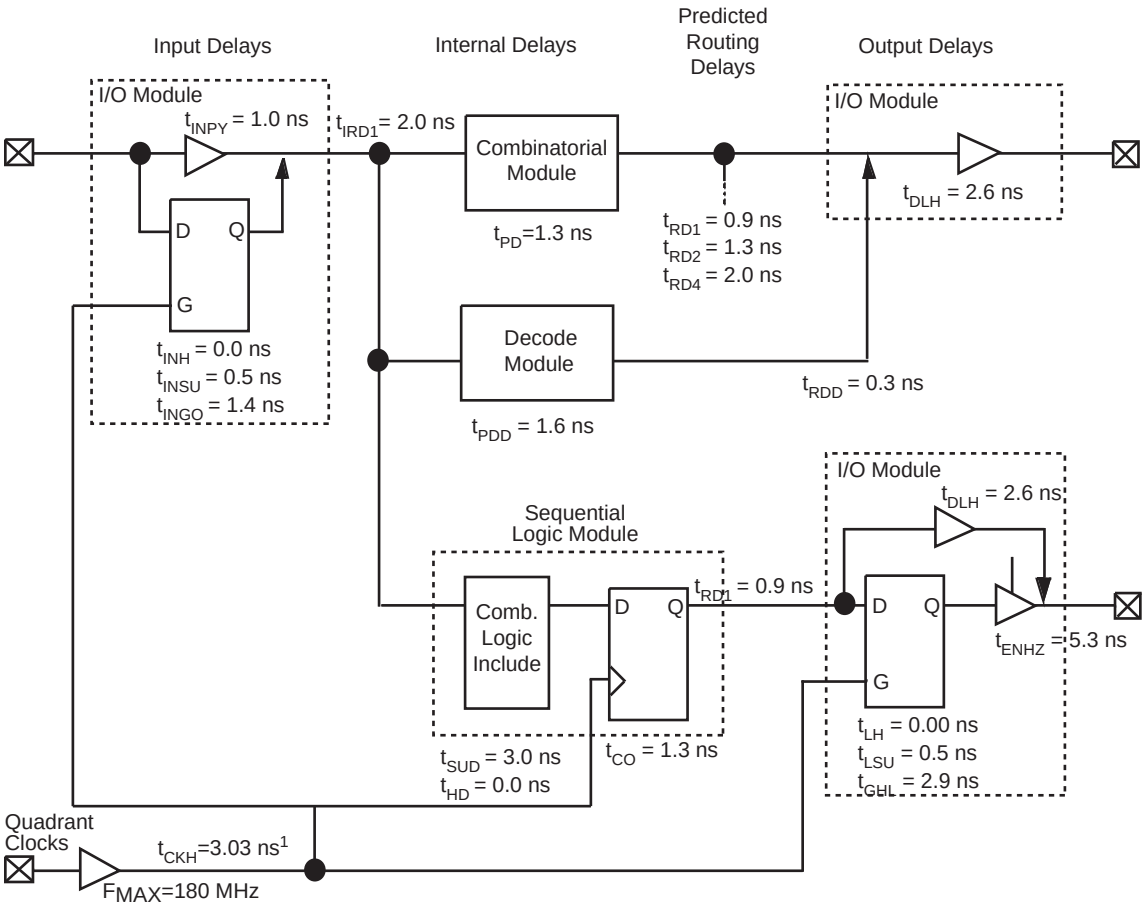
***Figure 18 •*** **42MX Timing Model**




**Note:** 1. Input module predicted routing delay

**Note:** 2. Values are shown for A42MX09 –3 at 5.0 V worst-case commercial conditions.

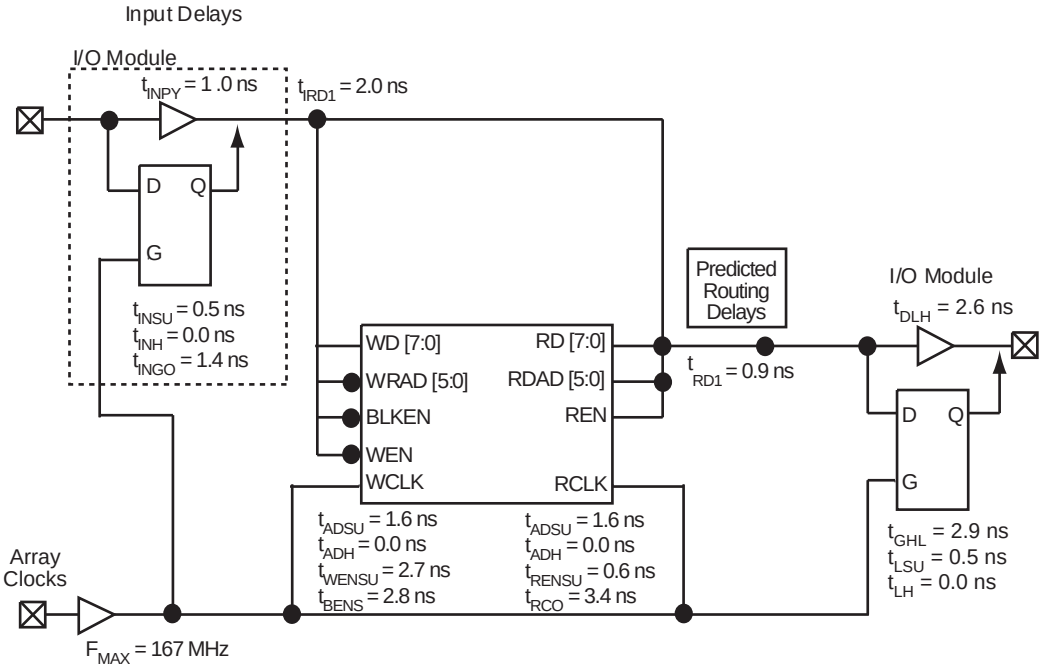
***Figure 19 •*** **42MX Timing Model (Logic Functions Using Quadrant Clocks)**




**Note:** 1. Load-dependent

**Note:** 2. Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions

***Figure 20 •*** **42MX Timing Model (SRAM Functions)**




**Note:** Values are shown for A42MX36 –3 at 5.0 V worst-case commercial conditions.

## 3.10.1 Parameter Measurement

The following figures show parameter measurement details.

***Figure 21 •*** **Output Buffer Delays**

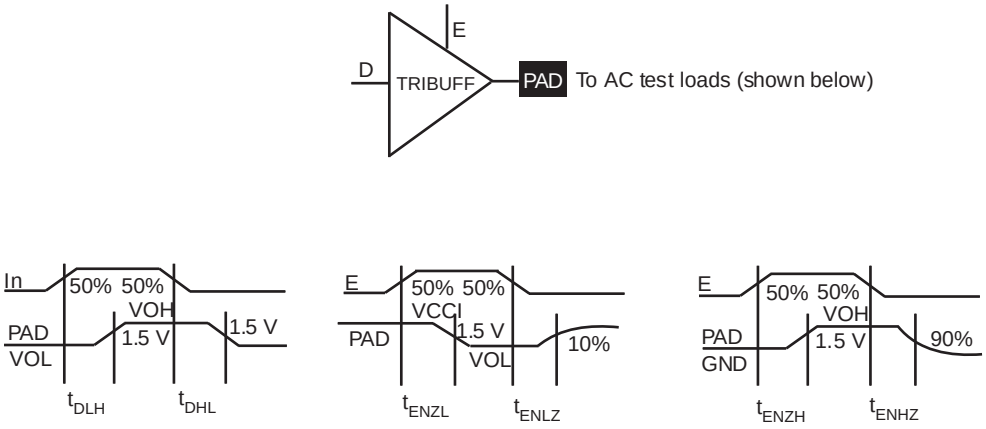


***Figure 22 •*** **AC Test Loads**

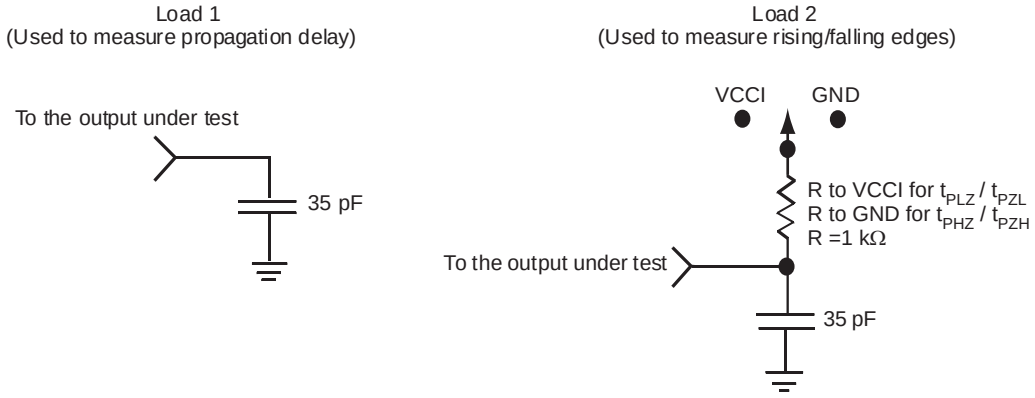



***Figure 23 •*** **Input Buffer Delays**

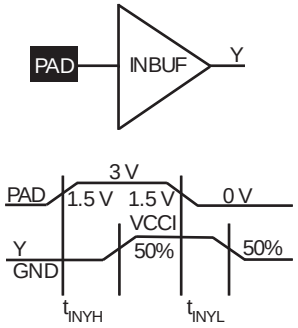



***Figure 24 •*** **Module Delays**

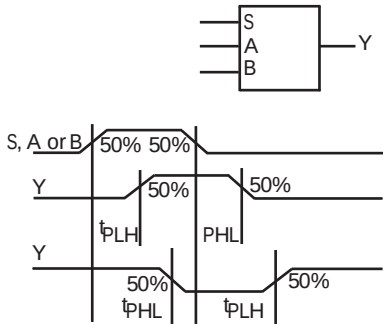
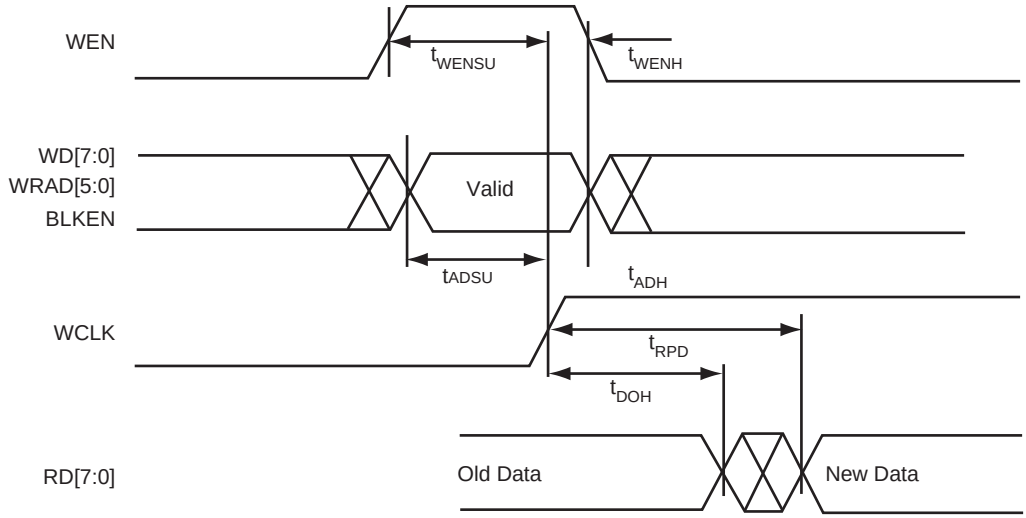


***Figure 33 •*** **42MX SRAM Asynchronous Read Operation—Type 2 (Write Address Controlled)**




## 3.10.7 Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 µm lithography, offer nominal levels of 100 Ω resistance and 7.0 fF capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

# 3.11 Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. Internal routing delays are device-dependent; actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer software utility or by performing simulation with post-layout delays.

## 3.11.1 Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment in Microsemi's Designer software prior to placement and routing. Up to 6% of the nets in a design may be designated as critical.

## 3.11.2 Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add

***Table 41 •*** **A42MX16 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PWL}$ | Minimum Pulse Width LOW | FO = 32 | 5.3 | | 5.9 | | 6.7 | | 7.8 | | 11.0 | | ns |
| | | FO = 384 | 6.2 | | 6.9 | | 7.9 | | 9.2 | | 12.9 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32 | | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | ns |
| | | FO = 384 | | 2.2 | | 2.4 | | 2.7 | | 3.2 | | 4.5 | ns |
| $t_{SUEXT}$ | Input Latch External Set-Up | FO = 32 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| | | FO = 384 | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.0 | | ns |
| | | FO = 384 | 4.5 | | 4.9 | | 5.6 | | 6.6 | | 9.2 | | ns |
| $t_P$ | Minimum Period | FO = 32 | 7.0 | | 7.8 | | 8.4 | | 9.7 | | 16.2 | | ns |
| | | FO = 384 | 7.7 | | 8.6 | | 9.3 | | 10.7 | | 17.8 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32 | | 142 | | 129 | | 119 | | 103 | | 62 | MHz |
| | | FO = 384 | | 129 | | 117 | | 108 | | 94 | | 56 | MHz |
| **TTL Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 3.5 | | 3.9 | | 4.4 | | 5.2 | | 7.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 4.1 | | 4.6 | | 5.2 | | 6.1 | | 8.6 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 4.8 | | 5.3 | | 6.0 | | 7.2 | | 10.0 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |
| $t_{ACO}$ | Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 11.3 | | 12.5 | | 14.2 | | 16.7 | | 23.3 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 4.5 | | 5.0 | | 5.6 | | 6.6 | | 9.3 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.4 | | 3.8 | | 4.3 | | 5.1 | | 7.1 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.8 | | 4.2 | | 4.8 | | 5.6 | | 7.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 4.2 | | 4.6 | | 5.3 | | 6.2 | | 8.7 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.6 | | 8.4 | | 9.5 | | 11.2 | | 15.7 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 7.0 | | 7.8 | | 8.8 | | 10.4 | | 14.5 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 7.1 | | 7.9 | | 8.9 | | 10.5 | | 14.7 | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading | | | 8.0 | | 8.9 | | 10.1 | | 11.9 | | 16.7 | ns |

**Table 42 • A42MX24 Timing Characteristics (Nominal 5.0 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 4.75 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.0 | | 1.1 | | 1.3 | | 1.5 | | 2.1 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.3 | | 1.4 | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.5 | | 0.5 | | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 4.7 | | 5.2 | | 5.9 | | 6.9 | | 9.7 | | ns |

***Table 43 •*** **A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Logic Module Sequential Timing[3, 4]** | | | | | | | | | | | | |
| $t_{CO}$ | Flip-Flop Clock-to-Output | | 2.1 | | 2.0 | | 2.3 | | 2.7 | | 3.7 | ns |
| $t_{GO}$ | Latch Gate-to-Output | | 3.4 | | 1.9 | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SUD}$ | Flip-Flop (Latch) Set-Up Time | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Hold Time | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{RO}$ | Flip-Flop (Latch) Reset-to-Output | | 2.0 | | 2.2 | | 2.5 | | 2.9 | | 4.1 | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Set-Up | 0.6 | | 0.6 | | 0.7 | | 0.8 | | 1.2 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1 | | 6.8 | | 7.7 | | 9.0 | | 12.6 | | ns |
| **Input Module Propagation Delays** | | | | | | | | | | | | |
| $t_{INPY}$ | Input Data Pad-to-Y | | 1.4 | | 1.6 | | 1.8 | | 2.2 | | 3.0 | ns |
| $t_{INGO}$ | Input Latch Gate-to-Output | | 1.8 | | 1.9 | | 2.2 | | 2.6 | | 3.6 | ns |
| $t_{INH}$ | Input Latch Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Latch Set-Up | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{ILA}$ | Latch Active Pulse Width | 6.5 | | 7.3 | | 8.2 | | 9.7 | | 13.5 | | ns |

**Table 43 • A42MX24 Timing Characteristics (Nominal 3.3 V Operation) *(continued)*(Worst-Case Commercial Conditions, VCCA = 3.0 V, $T_J$ = 70°C)**

| Parameter / Description | | | –3 Speed | | –2 Speed | | –1 Speed | | Std Speed | | –F Speed | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **TTL Output Module Timing[5] (continued)** | | | | | | | | | | | | | |
| $t_{LH}$ | I/O Latch Output Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| **CMOS Output Module Timing[5]** | | | | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad HIGH | | | 4.8 | | 5.3 | | 5.5 | | 6.4 | | 9.0 | ns |
| $t_{DHL}$ | Data-to-Pad LOW | | | 3.5 | | 3.9 | | 4.1 | | 4.9 | | 6.8 | ns |
| $t_{ENZH}$ | Enable Pad Z to HIGH | | | 3.6 | | 4.0 | | 4.5 | | 5.3 | | 7.4 | ns |
| $t_{ENZL}$ | Enable Pad Z to LOW | | | 3.4 | | 4.0 | | 5.0 | | 5.8 | | 8.2 | ns |
| $t_{ENHZ}$ | Enable Pad HIGH to Z | | | 7.2 | | 8.0 | | 9.0 | | 10.7 | | 14.9 | ns |
| $t_{ENLZ}$ | Enable Pad LOW to Z | | | 6.7 | | 7.5 | | 8.5 | | 9.9 | | 13.9 | ns |
| $t_{GLH}$ | G-to-Pad HIGH | | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{GHL}$ | G-to-Pad LOW | | | 6.8 | | 7.6 | | 8.6 | | 10.1 | | 14.2 | ns |
| $t_{LSU}$ | I/O Latch Set-Up | | 0.7 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{LH}$ | I/O Latch Hold | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{LCO}$ | I/O Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 7.7 | | 8.5 | | 9.6 | | 11.3 | | 15.9 | ns |
| $t_{ACO}$ | Array Latch Clock-to-Out (Pad-to-Pad) 32 I/O | | | 14.8 | | 16.5 | | 18.7 | | 22.0 | | 30.8 | ns |
| $d_{TLH}$ | Capacitive Loading, LOW to HIGH | | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.10 | ns/pF |
| $d_{THL}$ | Capacitive Loading, HIGH to LOW | | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32 | 3.9 | | 4.3 | | 4.9 | | 5.7 | | 8.1 | | ns |
| | | FO = 486 | 4.6 | | 5.2 | | 5.8 | | 6.9 | | 9.6 | | ns |
| $t_P$ | Minimum Period ($1/f_{MAX}$) | FO = 32 | 7.8 | | 8.7 | | 9.5 | | 10.8 | | 18.2 | | ns |
| | | FO = 486 | 8.6 | | 9.5 | | 10.4 | | 11.9 | | 19.9 | | ns |

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.
5. Delays based on 35 pF loading.

***Table 50 •*** **PQ 100**

| **PQ100** | | | | |
|---|---|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** | **A42MX09 Function** | **A42MX16 Function** |
| 56 | VCC | VCC | I/O | I/O |
| 57 | I/O | I/O | GND | GND |
| 58 | I/O | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O | I/O |
| 63 | GND | GND | I/O | I/O |
| 64 | I/O | I/O | LP | LP |
| 65 | I/O | I/O | VCCA | VCCA |
| 66 | I/O | I/O | VCCI | VCCI |
| 67 | I/O | I/O | VCCA | VCCA |
| 68 | I/O | I/O | I/O | I/O |
| 69 | VCC | VCC | I/O | I/O |
| 70 | I/O | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O | I/O |
| 72 | I/O | I/O | GND | GND |
| 73 | I/O | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O | I/O |
| 77 | NC | NC | I/O | I/O |
| 78 | NC | NC | I/O | I/O |
| 79 | NC | NC | SDI, I/O | SDI, I/O |
| 80 | NC | I/O | I/O | I/O |
| 81 | NC | I/O | I/O | I/O |
| 82 | NC | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O | I/O |
| 84 | I/O | I/O | GND | GND |
| 85 | I/O | I/O | I/O | I/O |
| 86 | GND | GND | I/O | I/O |
| 87 | GND | GND | PRA, I/O | PRA, I/O |
| 88 | I/O | I/O | I/O | I/O |
| 89 | I/O | I/O | CLKA, I/O | CLKA, I/O |
| 90 | CLK, I/O | CLK, I/O | VCCA | VCCA |
| 91 | I/O | I/O | I/O | I/O |
| 92 | MODE | MODE | CLKB, I/O | CLKB, I/O |

***Table 53 •*** **PQ208**

| **PQ208** | | | |
|---|---|---|---|
| **Pin Number** | **A42MX16 Function** | **A42MX24 Function** | **A42MX36 Function** |
| 132 | VCCI | VCCI | VCCI |
| 133 | VCCA | VCCA | VCCA |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | VCCA | VCCA | VCCA |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O |
| 145 | I/O | I/O | I/O |
| 146 | NC | I/O | I/O |
| 147 | NC | I/O | I/O |
| 148 | NC | I/O | I/O |
| 149 | NC | I/O | I/O |
| 150 | GND | GND | GND |
| 151 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O |
| 155 | I/O | I/O | I/O |
| 156 | I/O | I/O | I/O |
| 157 | GND | GND | GND |
| 158 | I/O | I/O | I/O |
| 159 | SDI, I/O | SDI, I/O | SDI, I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | WD, I/O | WD, I/O |
| 162 | I/O | WD, I/O | WD, I/O |
| 163 | I/O | I/O | I/O |
| 164 | VCCI | VCCI | VCCI |
| 165 | NC | I/O | I/O |
| 166 | NC | I/O | I/O |
| 167 | I/O | I/O | I/O |
| 168 | I/O | WD, I/O | WD, I/O |

***Table 54 •*** **PQ240**

| PQ240 | |
|---|---|
| **Pin Number** | **A42MX36 Function** |
| 237 | GND |
| 238 | MODE |
| 239 | VCCA |
| 240 | GND |

***Figure 46 •*** **VQ80**

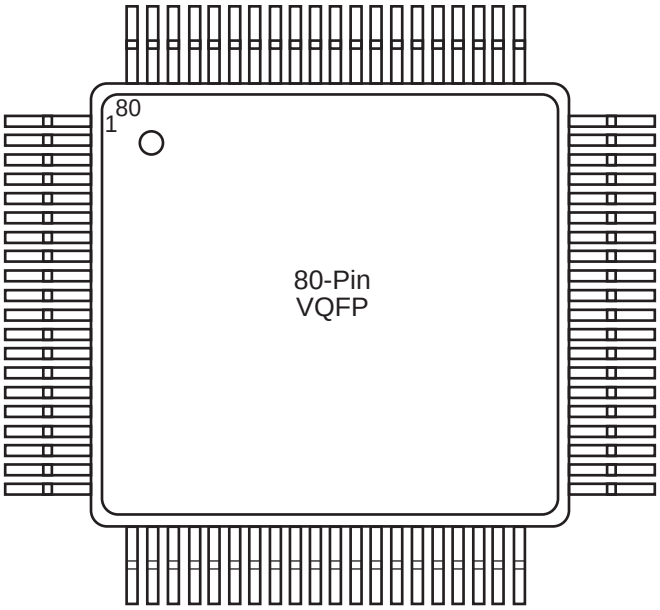



***Table 55 •*** **VQ80**

| VQ80 | | |
|---|---|---|
| **Pin Number** | **A40MX02 Function** | **A40MX04 Function** |
| 1 | I/O | I/O |
| 2 | NC | I/O |
| 3 | NC | I/O |
| 4 | NC | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |

***Figure 47 •*** **VQ100**

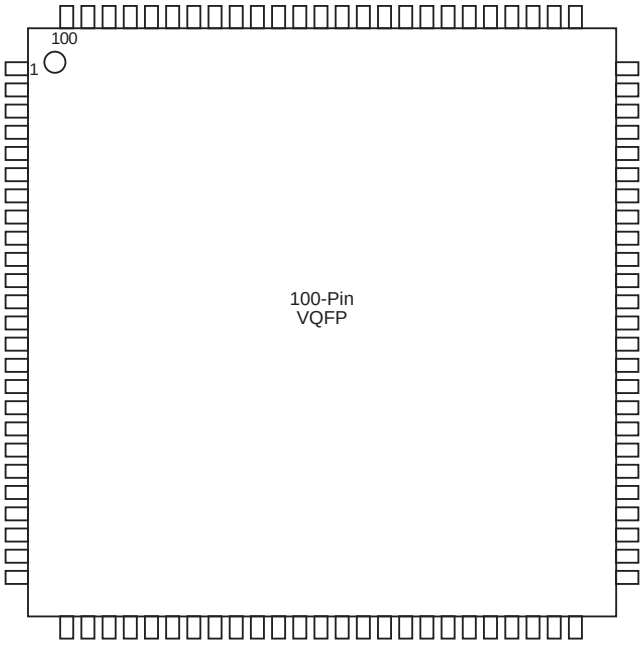



***Table 56 •*** **VQ100**

| **VQ100** | | |
|---|---|---|
| **Pin Number** | **A42MX09 Function** | **A42MX16 Function** |
| 1 | I/O | I/O |
| 2 | MODE | MODE |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | GND | GND |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | VCCA | NC |
| 15 | VCCI | VCCI |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | GND | GND |

***Table 61 •*** **PG132**

| **PG132** | |
|---|---|
| **Pin Number** | **A42MX09 Function** |
| N10 | I/O |
| M10 | I/O |
| N11 | I/O |
| L10 | I/O |
| M11 | I/O |
| N12 | SDO |
| M12 | I/O |
| L11 | I/O |
| N13 | I/O |
| M13 | I/O |
| K11 | I/O |
| L12 | I/O |
| L13 | I/O |
| K13 | I/O |
| H10 | I/O |
| J12 | I/O |
| J13 | I/O |
| H11 | I/O |
| H12 | I/O |
| H13 | VKS |
| G13 | VPP |

***Table 62 •*** **CQ172**

| | |
|---|---|
| 138 | I/O |
| 139 | I/O |
| 140 | I/O |
| 141 | GND |
| 142 | I/O |
| 143 | I/O |
| 144 | I/O |
| 145 | I/O |
| 146 | I/O |
| 147 | I/O |
| 148 | PROBA |
| 149 | I/O |
| 150 | CLKA |
| 151 | VCC |
| 152 | GND |
| 153 | I/O |
| 154 | CLKB |
| 155 | I/O |
| 156 | PROBB |
| 157 | I/O |
| 158 | I/O |
| 159 | I/O |
| 160 | I/O |
| 161 | GND |
| 162 | I/O |
| 163 | I/O |
| 164 | I/O |
| 165 | I/O |
| 166 | VCCI |
| 167 | I/O |
| 168 | I/O |
| 169 | I/O |
| 170 | I/O |
| 171 | DCLK |