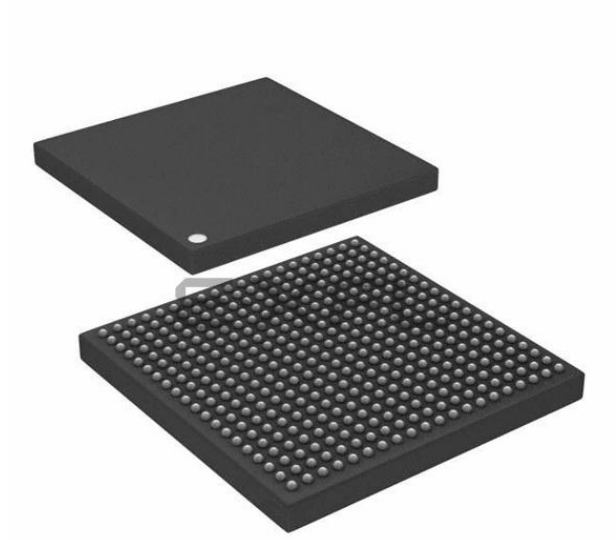

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx353cjq5c

1.3 Block Diagram

Figure 1 is the i.MX35 simplified interface block diagram.

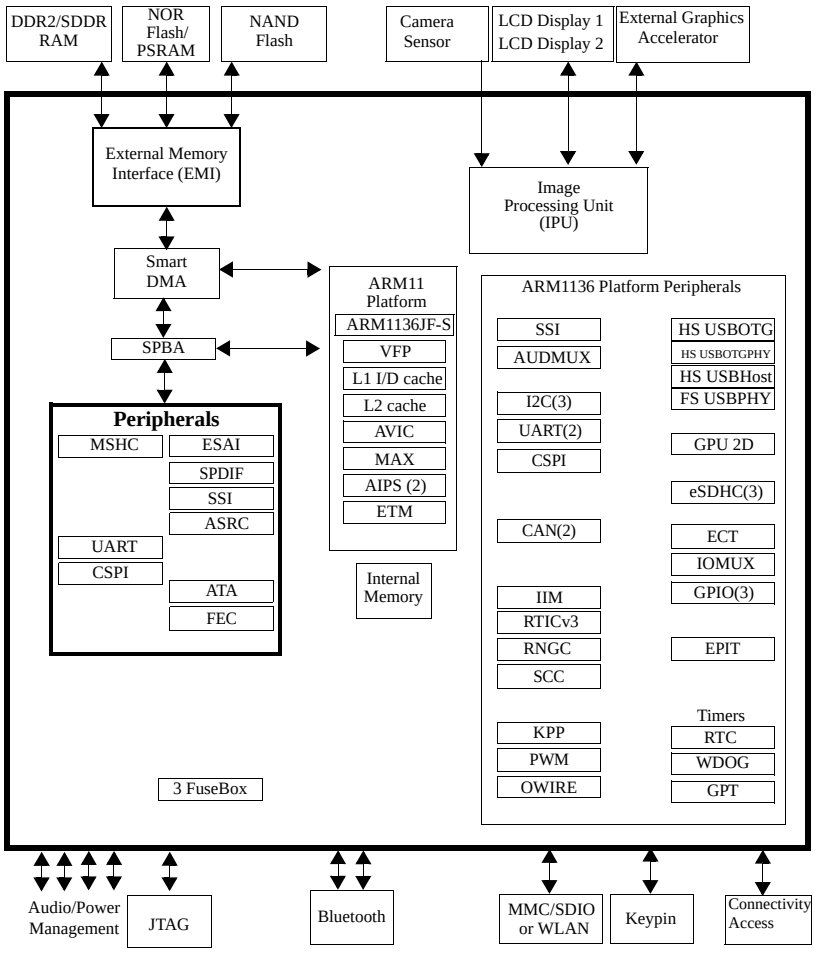

Figure 1. i.MX35 Simplified Interface Block Diagram

2 Functional Description and Application Information

The i.MX35 consists of the following major subsystems:

- ARM1136 Platform—AP domain
- SDMA Platform and EMI—Shared domain

2.1 Application Processor Domain Overview

The applications processor (AP) and its domain are responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The AP domain is built around an ARM1136JF-S core with 16-Kbyte instruction and data L1 caches, an MMU, a 128-Kbyte L2 cache, a multiported crossbar switch, and advanced debug and trace interfaces.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ATA	ATA module	SDMA	Connectivity peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disk drives and ATAPI optical disk drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	ARM	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CAN(2)	CAN module	ARM	Connectivity peripherals	The CAN protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
CCM	Clock control module	ARM	Clocks	This block generates all clocks for the peripherals in the SDMA platform. The CCM also manages ARM1136 platform low-power modes (WAIT, STOP), disabling peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.
CSPI(2)	Configurable serial peripheral interface	SDMA, ARM	Connectivity peripherals	This module is a serial interface equipped with data FIFOs; each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
ECT	Embedded cross trigger	SDMA, ARM	Debug	ECT (embedded cross trigger) is an IP for real-time debug purposes. It is a programmable matrix allowing several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources available within the SoC.
EMI	External memory interface	SDMA	External memory interface	The EMI module provides access to external memory for the ARM and other masters. It is composed of the following main submodules: M3IF—provides arbitration between multiple masters requesting access to the external memory. SDRAM CTRL—interfaces to mDDR, DDR2 (4-bank architecture type), and SDR interfaces. NANDFC—provides an interface to NAND Flash memories. WEIM—interfaces to NOR Flash and PSRAM.
EPIT(2)	Enhanced periodic interrupt timer	ARM	Timer peripherals	Each EPIT is a 32-bit “set-and-forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

Table 26. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Clock frequency	f	—	125	—	—	MHz
Output pin slew rate (max. drive)[1]	tps	25 pF 50 pF	2.83/2.68 1.59/1.49	1.84/1.85 1.03/1.05	1.21/1.40 0.70/0.75	V/ns
Output pin di/dt (max. drive)[2]	didt	25 pF 50 pF	89 95	202 213	435 456	mA/ns
Input pin transition times[3]	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pin propagation delay, 50%–50%	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pin propagation delay, 40%–60%	tpi	1.0 pF	1.18/1.99	1.45/2.35	1.97/2.85	ns

1 Min. condition for tps: wcs model, 1.1 V, IO 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Max. condition for tdit: bcs model, 1.3 V, IO 1.95 V, and –40 °C.

3 Max. condition for tpi and trfi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Min. condition for tpi and trfi: bcs model, 1.3 V, IO 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

4.9 Module-Level AC Electrical Specifications

This section contains the AC electrical information (including timing specifications) for the modules of the i.MX35. The modules are listed in alphabetical order.

4.9.1 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. See the electrical specification for SSI.

4.9.2 CSPI AC Electrical Specifications

The i.MX35 provides two CSPI modules. CSPI ports are multiplexed in the i.MX35 with other pins. See the “External Signals and Multiplexing” chapter of the reference manual for more details.

Table 32. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle[2]		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{\text{NF\_WP}}$ pulse width	tWP	T – 1.0 ns		29		ns
NF6	NFALE setup time	tALS	T – 4.0 ns	—	26	—	ns
NF7	NFALE hold time	tALH	T – 4.5 ns	—	25.5	—	ns
NF8	Data setup time	tDS	T – 2.0 ns	—	28	—	ns
NF9	Data hold time	tDH	T – 5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T – 3.0 ns		57		ns
NF11	$\overline{\text{NFWE}}$ hold time	tWH	T – 5.0 ns		25		ns
NF12	Ready to $\overline{\text{NFRE}}$ low	tRR	6T	—	180	—	ns
NF13	$\overline{\text{NFRE}}$ pulse width	tRP	1.5T – 1.0 ns	—	44	—	ns
NF14	READ cycle time	tRC	2T – 5.5 ns	—	54.5	—	ns
NF15	$\overline{\text{NFRE}}$ high hold time	tREH	0.5T – 4.0 ns		11	—	ns
NF16	Data setup on READ	tDSR	N/A		9	—	ns
NF17	Data hold on READ	tDHR	N/A		0	—	ns

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification listed in Table 28, "DPLL Specifications," on page 31.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.9.5.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clocks related to the BCLK rising edge or falling edge according to the corresponding assertion or negation control fields. The address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration.

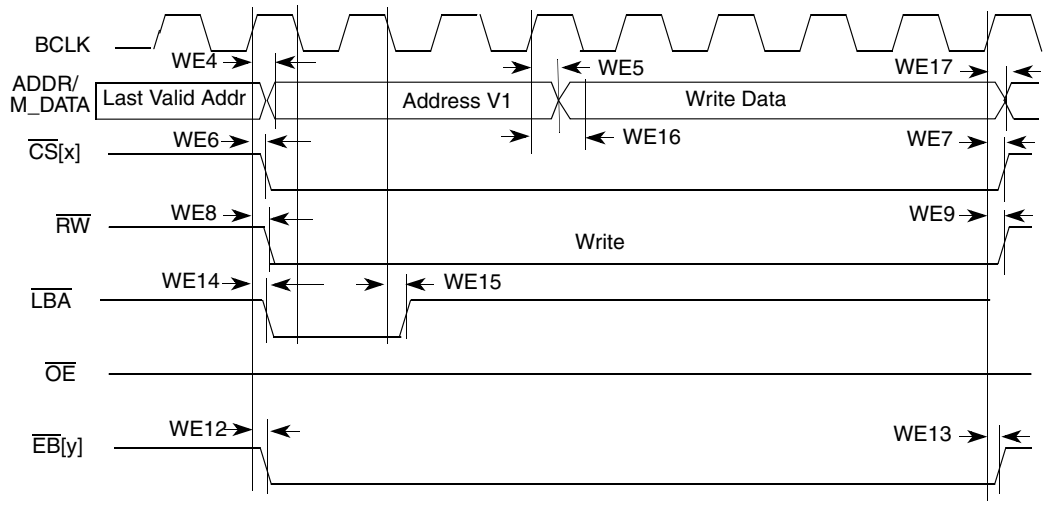

Figure 20. Muxed A/D Mode Timing Diagram for Synchronous Write Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1

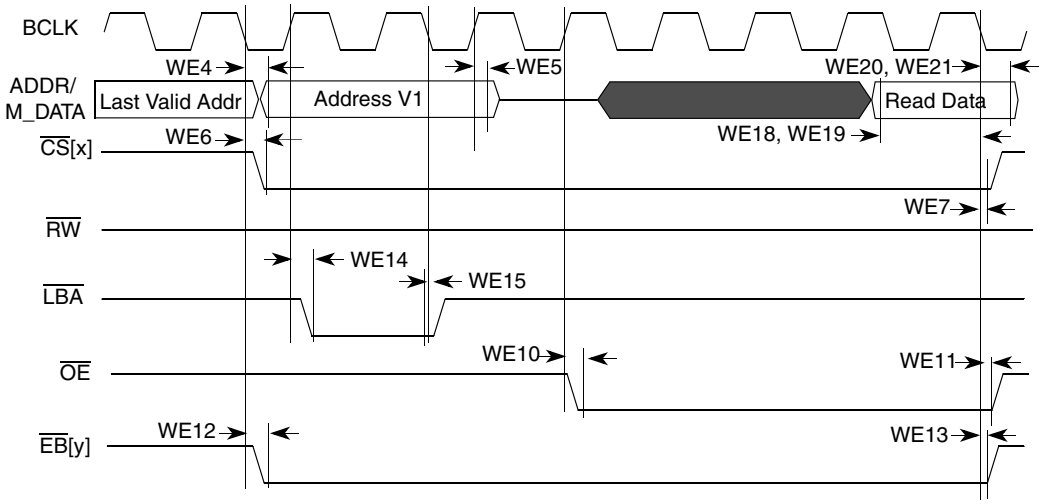

Figure 21. Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7

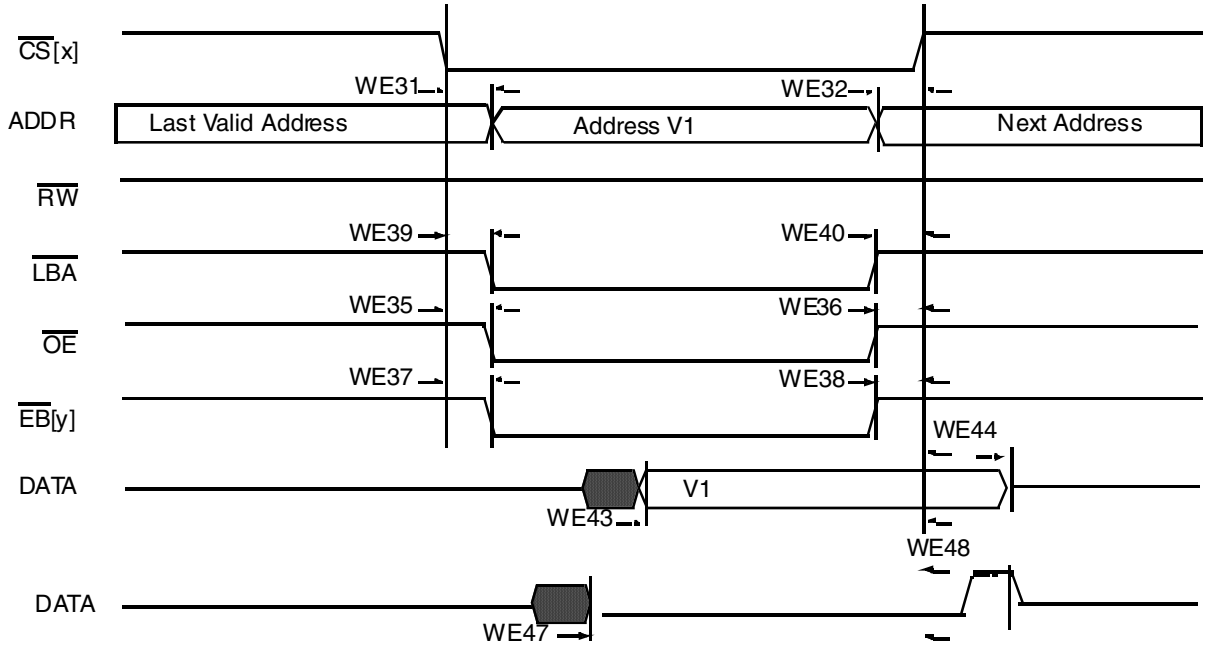

Figure 26. DTACK Read Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE32A(muxed A/D	$\overline{CS}$[x] valid to address invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] valid to $\overline{WE}$ valid	WE8 – WE6 + (WEA – CSA)	—	3 + (WEA – CSA)	ns
WE34	$\overline{WE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE9 + (WEN – CSN)	—	3 – (WEN_CSN)	ns
WE35	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{OE}$ valid	WE10 – WE6 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	–3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	3 + (OEA + RLBN + RLBA + ADH + 1 – CSA)	ns
WE36	$\overline{OE}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (read access)	WE12 – WE6 + (RBEA – CSA)	—	3 + (RBEA[4] – CSA)	ns
WE38	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (read access)	WE7 – WE13 + (RBEN – CSN)	—	3 – (RBEN[5] – CSN)	ns
WE39	$\overline{CS}$[x] valid to $\overline{LBA}$ valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ invalid to $\overline{CS}$[x] invalid	WE7 – WE15 – CSN	—	3 – CSN	ns

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE40A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{LBA}$ invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 + (WLBN + WLBA + ADH + 1 – WCSA)	—	3 + (WLBN + WLBA + ADH + 1 – WCSA)	ns
WE42	Output Data invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	$\overline{DTACK}$ valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

1 For the value of parameters WE4–WE21, see column BCD = 0 in Table 33.

2 $\overline{CS}$ Assertion. This bit field determines when the $\overline{CS}$ signal is asserted during read/write cycles.

3 $\overline{CS}$ Negation. This bit field determines when the $\overline{CS}$ signal is negated during read/write cycles.

4 $\overline{BE}$ Assertion. This bit field determines when the $\overline{BE}$ signal is asserted during read cycles.

5 $\overline{BE}$ Negation. This bit field determines when the $\overline{BE}$ signal is negated during read cycles.

6 Output maximum delay from internal driving ADDR/control FFs to chip outputs.

7 Output maximum delay from $\overline{CS}$[x] internal driving FFs to $\overline{CS}$[x] out.

8 DATA maximum delay from chip input data to its internal FF.

9 DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA, CSN, WBEA, WBEN, LBA, LBN, OEN, OEA, RBEA, and RBEN) are in cycle units.

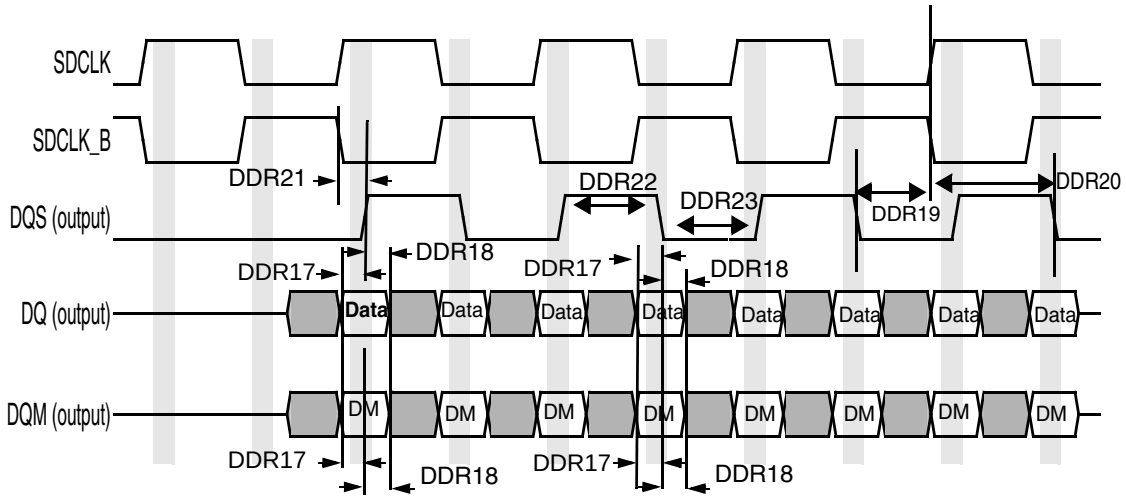

Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 41. DDR2 SDRAM Write Cycle Parameters

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (single-ended strobe)	$t_{DS1(base)}$	0.5	—	ns
DDR18	DQ and DQM hold time to DQS (single-ended strobe)	$t_{DH1(base)}$	0.5	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time.	t_{DSS}	0.2	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time.	t_{DSH}	0.2	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	–0.25	0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low level width	t_{DQSL}	0.35	—	tCK

NOTE

These values are for DQ/DM slew rate of 1 V/ns and DQS slew rate of 1 V/ns. For different values use the derating table.

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	t_{DQSQ}	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	t_{QH}	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

[1]The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

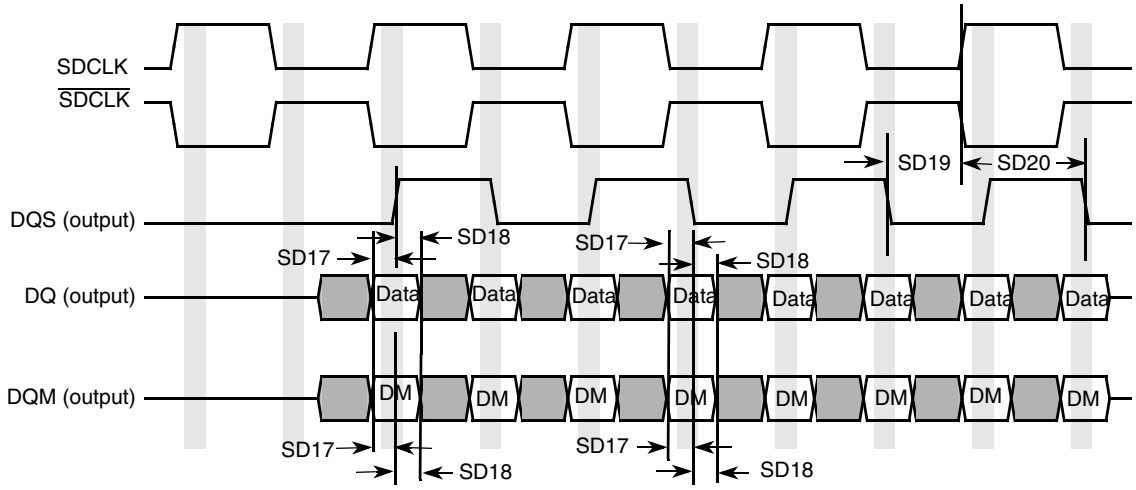

Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

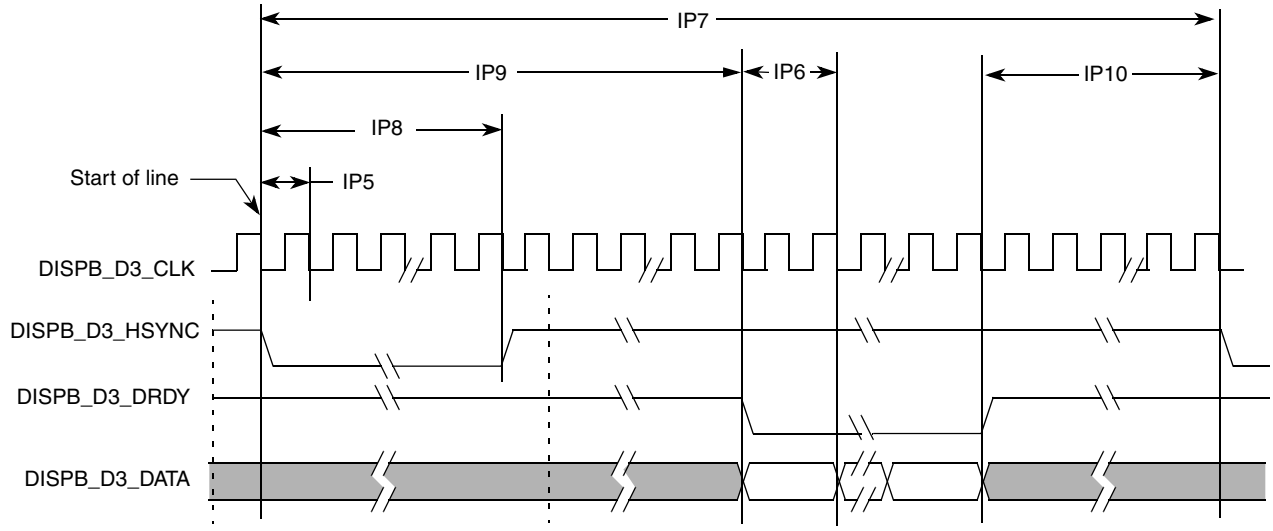

Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 49 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

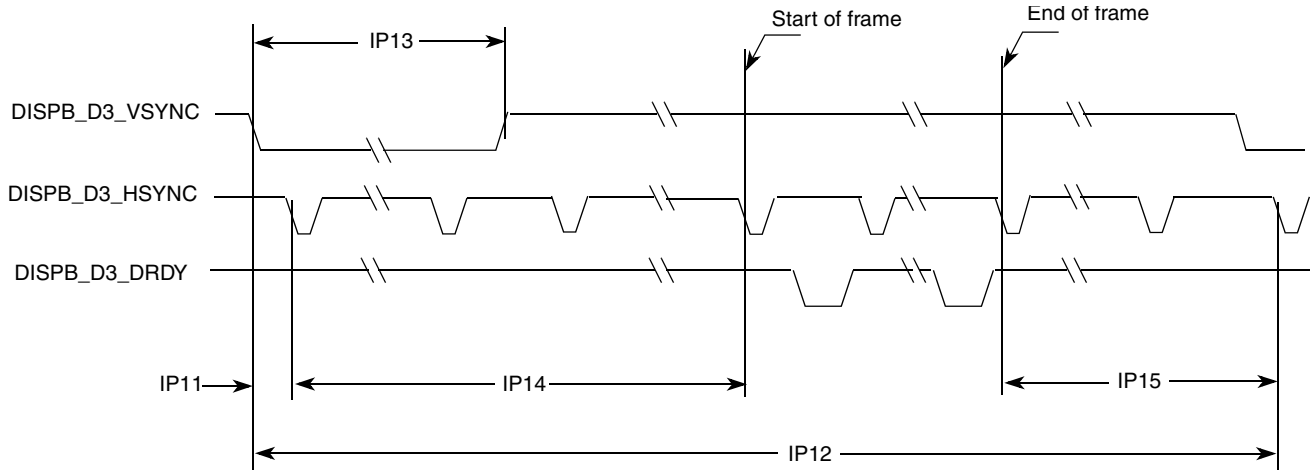

Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 55 shows timing parameters of signals presented in Figure 48 and Figure 49.

Table 55. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp[1]	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D + 1) × Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH + 1) × Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH + 1) × Tdpcp	ns

4.9.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.9.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 52 depicts the interface timing.

- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - — At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - — At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

DI_DISP*n*_TIME_CONF_3 registers (*n* = 0,1,2). Figure 57 shows the timing of the parallel interface with read wait states.

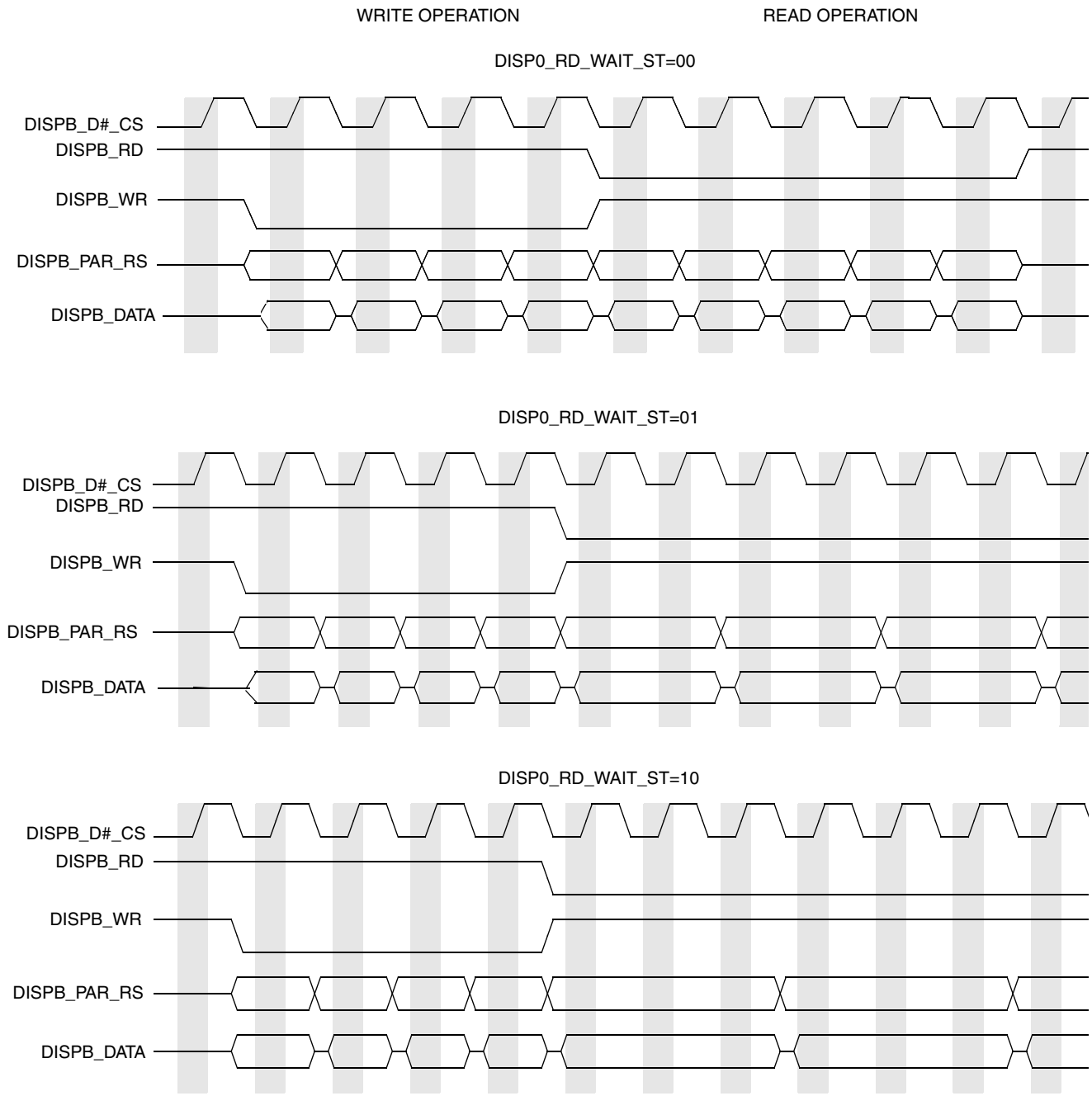

Figure 57. Parallel Interface Timing Diagram—Read Wait States

4.9.13.4.9 Parallel Interfaces, Electrical Characteristics

Figure 58, Figure 60, Figure 59, and Figure 61 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 58 lists the timing parameters at display access level. All

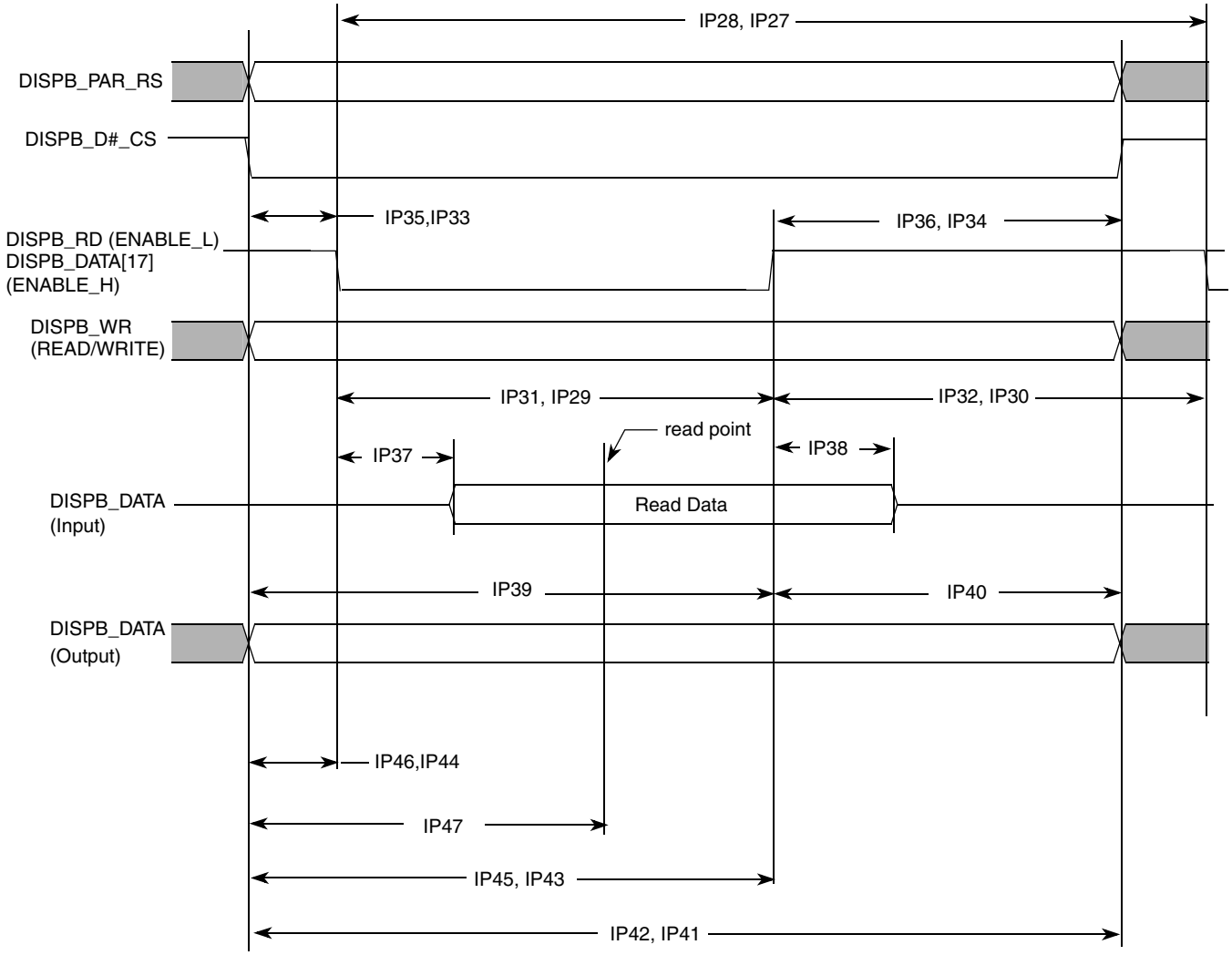

Figure 61. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 58. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP29	Read low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP30	Read high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP31	Write low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP32	Write high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns

Table 58. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP36	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP39	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device-specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

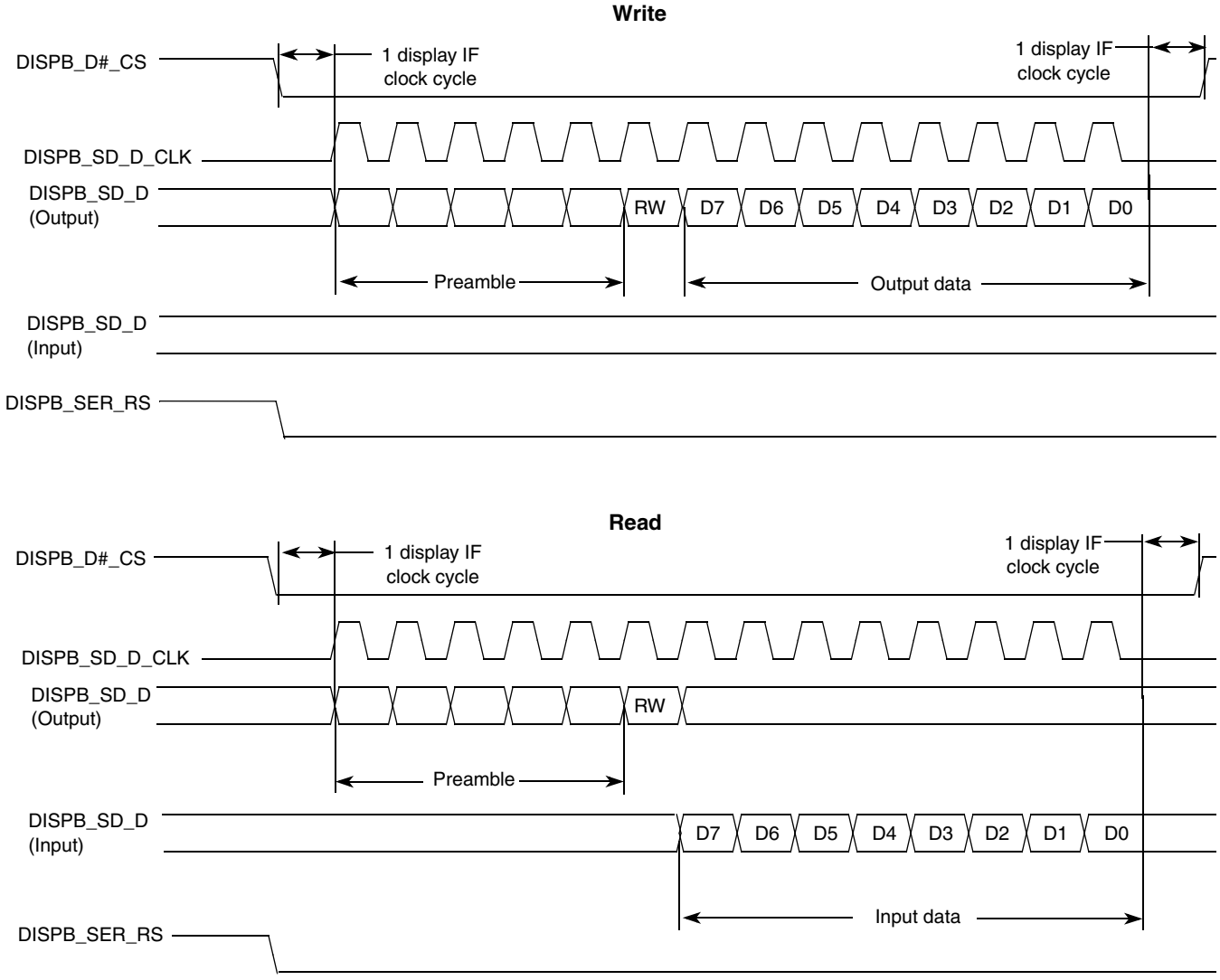

Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

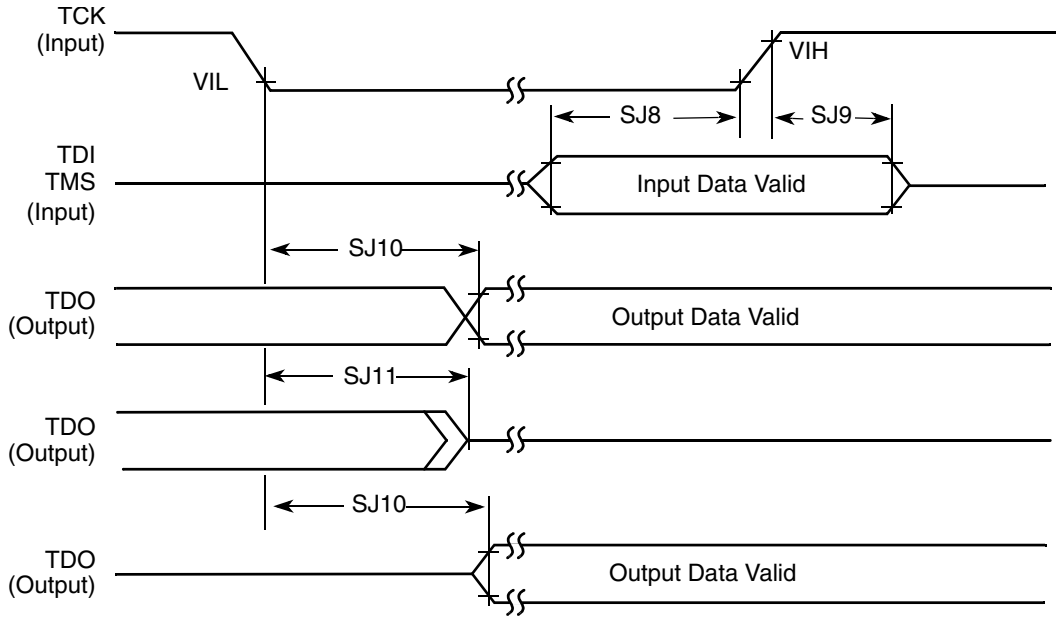

Figure 88. Test Access Port Timing Diagram

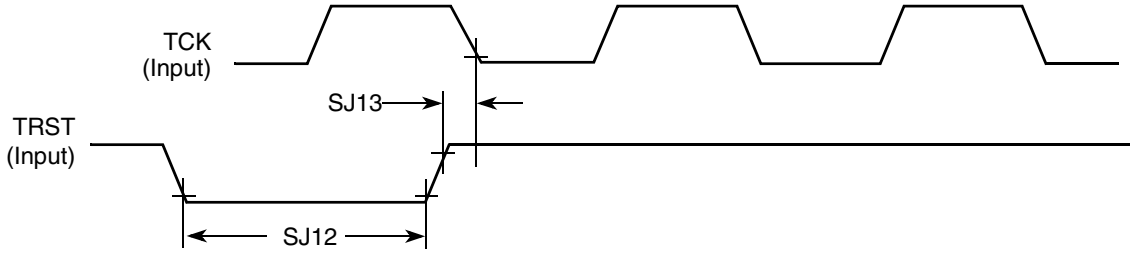

Figure 89. $\overline{\text{TRST}}$ Timing Diagram

Table 76. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

4.9.24.1 DAT_SE0 Bidirectional Mode

Table 86 defines the signals for DAT_SE0 bidirectional mode. Figure 100 and Figure 101 show the transmit and receive waveforms respectively.

Table 86. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

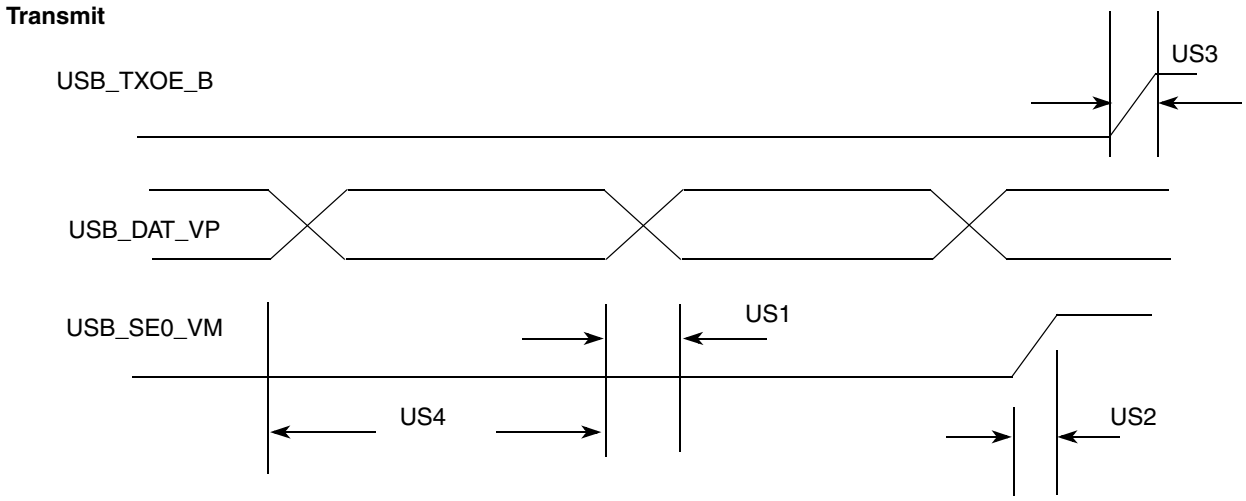

Figure 100. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

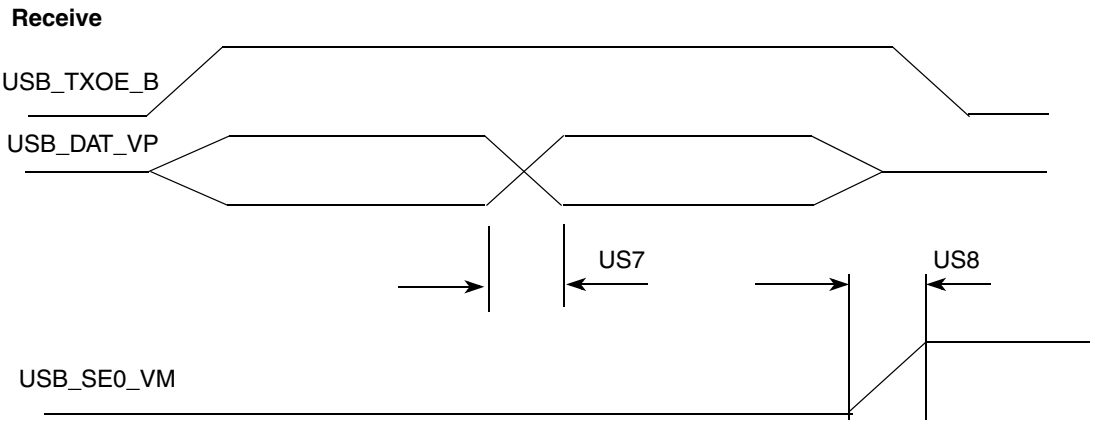

Figure 101. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_REF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.

7 Revision History

Table 98 shows the revision history of this document. Note: There were no revisions of this document between revision 1 and revision 4 or between revision 6 and revision 7.

Table 98. i.MX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
10	06/2012	• In Table 2, "Functional Differences in the i.MX35 Parts," on page 3, added two columns for part numbers MCIMX353 and MCIMX357. • Added Table 29, "Clock Input Tolerance," on page 31 in Section 4.9.3, “DPLL Electrical Specifications.” • Updated Table 39, "DDR2 SDRAM Timing Parameter Table," on page 50 for DDR2-400 values. • Updated Table 41, "DDR2 SDRAM Write Cycle Parameters," on page 52 for DDR2-400 values. • Added Table 15, "AC Requirements of I/O Pins," on page 24. • Updated WE4 parameter in Table 33, "WEIM Bus Timing Parameters," on page 37.
9	08/2010	• Updated Table 32, “NFC Timing Parameters.” • Updated Table 33, “WEIM Bus Timing Parameters.”
8	04/2010	• Updated Table 14, “I/O Pin DC Electrical Characteristics.”
7	12/18/2009	• Updated Table 1, “Ordering Information.”
6	10/21/2009	• Added information for silicon rev. 2.1 • Updated Table 1, “Ordering Information.” • Added Table 95, “Silicon Revision 2.1 Signal Ball Map Locations.” • Added Table 97, “Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch.”
5	08/06/2009	• Added a line for T_A = –40 to 85 ^oC in Table 14, “I/O Pin DC Electrical Characteristics” • Filled in TBDs in Table 14. • Revised Figure 15 and Table 33 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table. • Added Table 26, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V).”
4	04/30/2009	Note: There were no revisions of this document between revision 1 and revision 4. • In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6. • Updated values in Table 10, “i.MX35 Power Modes.” • Added Section 4.4, “Reset Timing.” • In Section 4.8.2, “AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes),” removed Slow Slew rate tables, relabeled Table 24, “AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode,” and Table 25, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode,” to exclude mention of slew rate. • In Section 4.9.5.2, “Wireless External Interface Module (WEIM),” modified Figure 16, “Synchronous Memory Timing Diagram for Read Access—WSC = 1,” through Figure 21, “Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7.” • In Section 4.9.6, “Enhanced Serial Audio Interface (ESAI) Timing Specifications,” modified Figure 36, “ESAI Transmitter Timing,” and Figure 37, “ESAI Receiver Timing,” to remove extraneous signals. Removed a note from Figure 36, “ESAI Transmitter Timing.”
3	03/2009	• In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6.
2	02/2009	• Added the following parts to Table 1, “Ordering Information”: PCIMX357CVM5B, MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B. Throughout consumer data sheet: Removed or updated information related to Media Local Bus interface.Updated Section 4.3.1, “Powering Up.” • Updated values in Table 10, “i.MX35 Power Modes.”