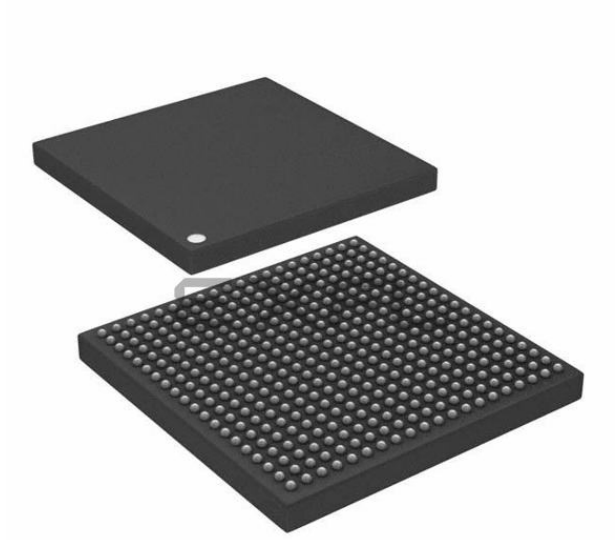

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx353djq5c

- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX353	MCIMX353CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX353	MCIMX353DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX357	MCIMX357CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX357	MCIMX357DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX353	MCIMX353CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX353	MCIMX353DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97
i.MX357	MCIMX357CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX357	MCIMX357DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

Table 2. Functional Differences in the i.MX35 Parts

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
I2C (3)	Yes	Yes	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes	Yes	Yes
ESAI	Yes	Yes	Yes	Yes	Yes
SPDIF I/O	Yes	Yes	Yes	Yes	Yes
USB HS Host	Yes	Yes	Yes	Yes	Yes
USB OTG	Yes	Yes	Yes	Yes	Yes
FlexCAN (2)	Yes	Yes	Yes	Yes	Yes
MLB	Yes	Yes	Yes	Yes	Yes

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
I^2C(3)	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

[2] The typical value of Vox(ac) is expected to be about 0.5 × NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload = 25 pF.

Table 24. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 25. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 9 depicts the TRACECLK timings of ETM, and Table 30 lists the timing parameters.

Figure 9. ETM TRACECLK Timing Diagram

Table 30. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 31 lists the timing parameters.

Figure 10. Trace Data Timing Diagram

Table 31. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.9.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same T_s and T_h parameters from Table 31 still apply with respect to the falling edge of the TRACECLK signal.

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	1.25	—	ns
DDR6	Address output setup time	t_{IS}[1]	1.5	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533

4.9.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 46 shows the interface timing values. The number field in the table refers to timing signals found in Figure 36 and Figure 37.

Table 46. Enhanced Serial Audio Interface Timing

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

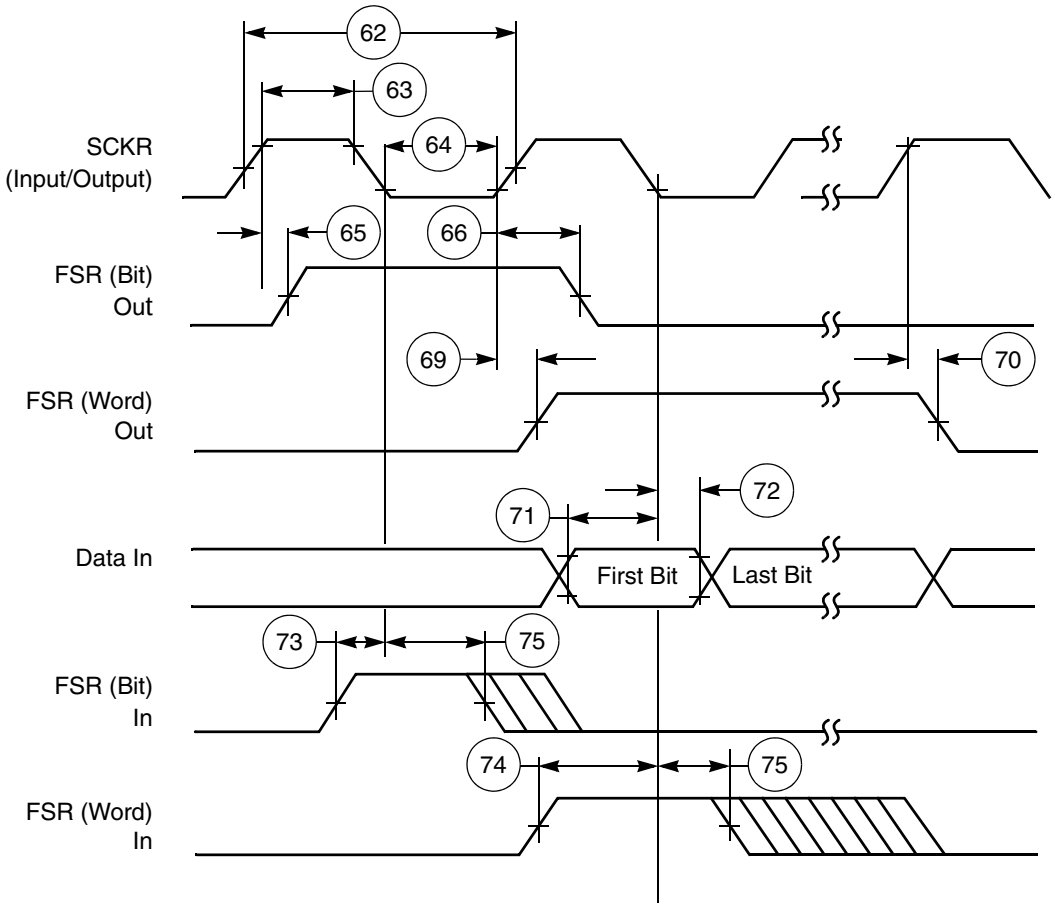

Figure 37. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 38 depicts the timing of eSDHCv2, and Table 47 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 47:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

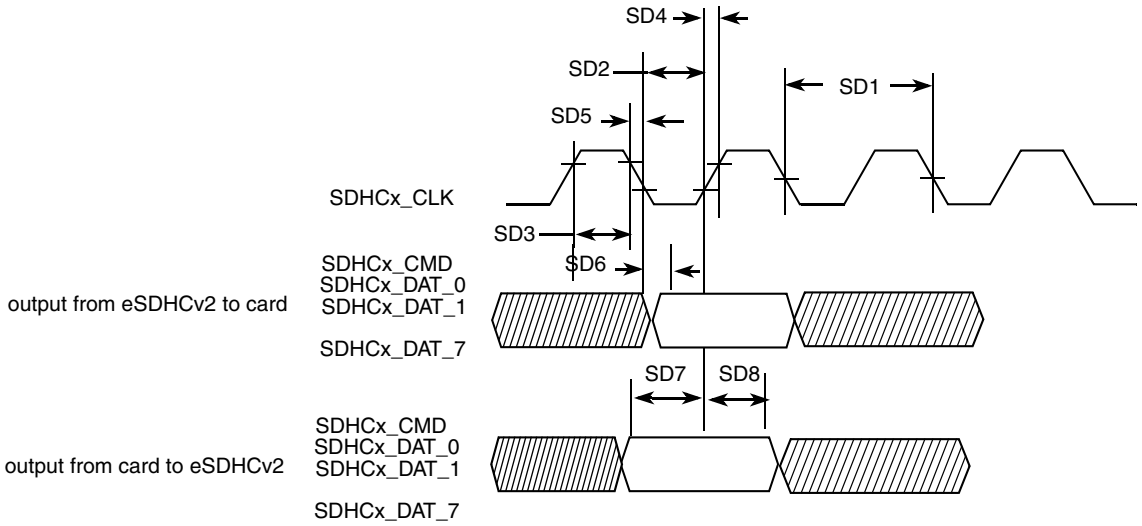

Figure 38. eSDHCv2 Timing

Table 47. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

4.9.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 52 depicts the interface timing.

- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - — At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - — At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

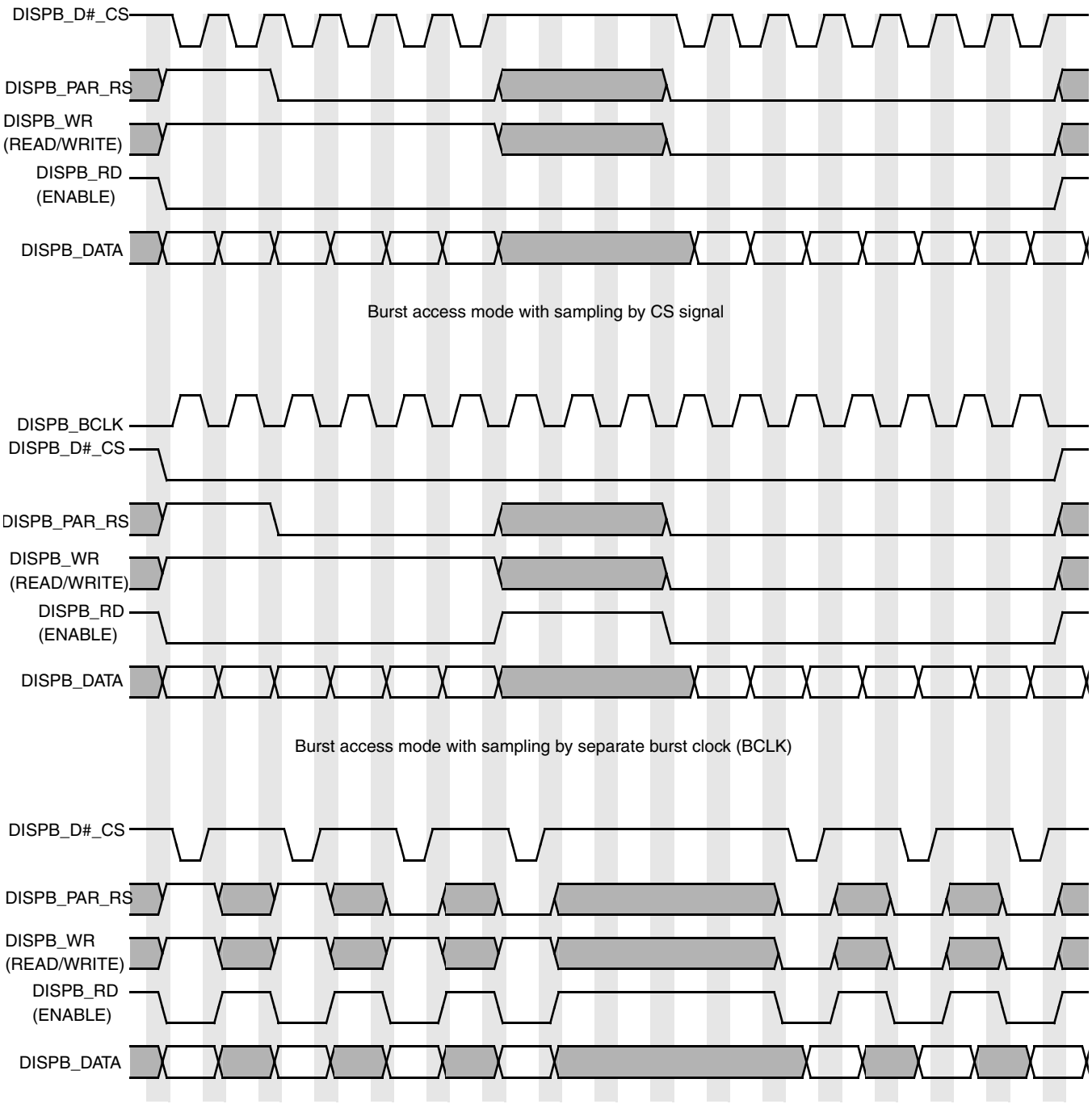

Figure 55. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

Figure 65 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

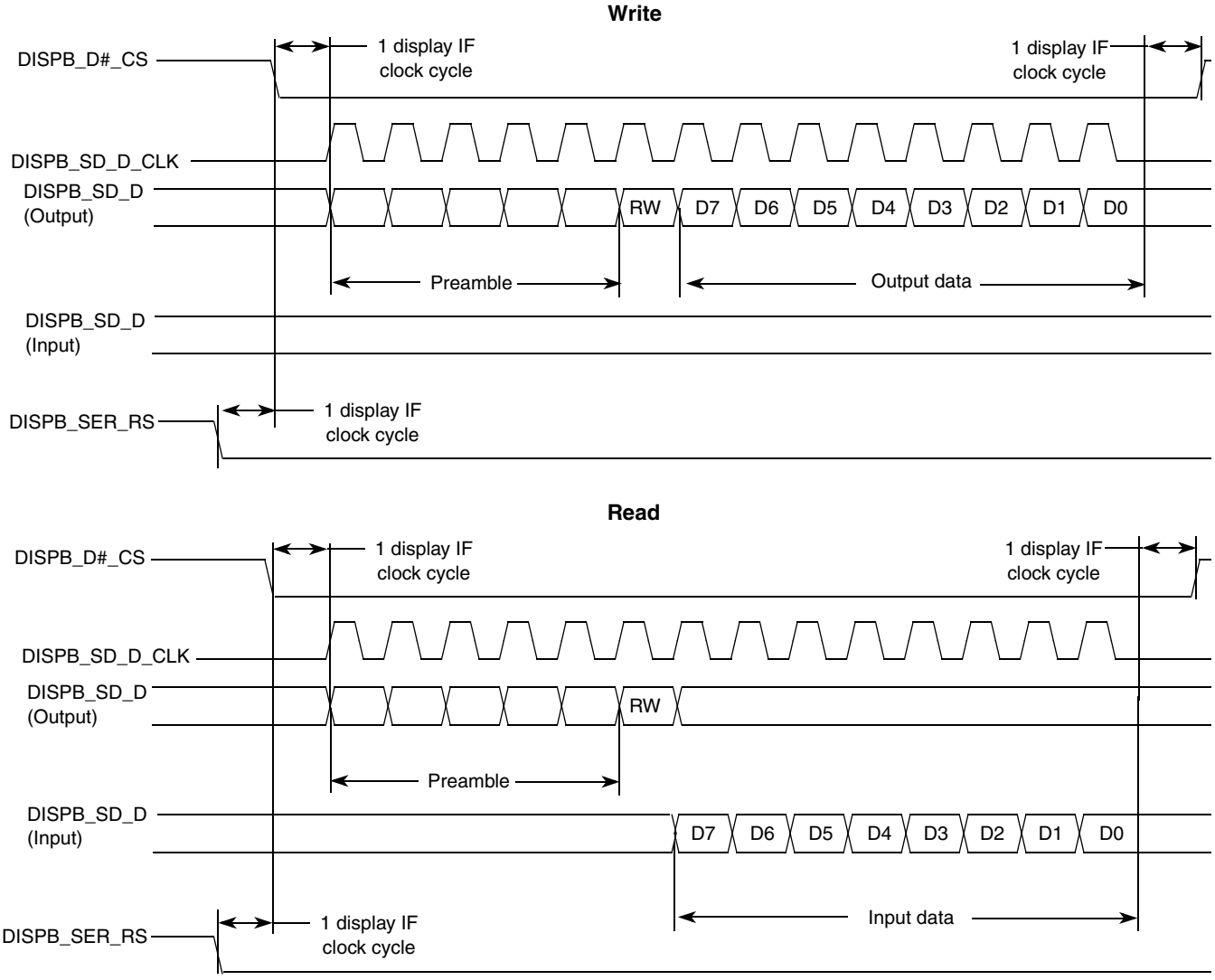

Figure 65. 5-Wire Serial Interface (Type 2) Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

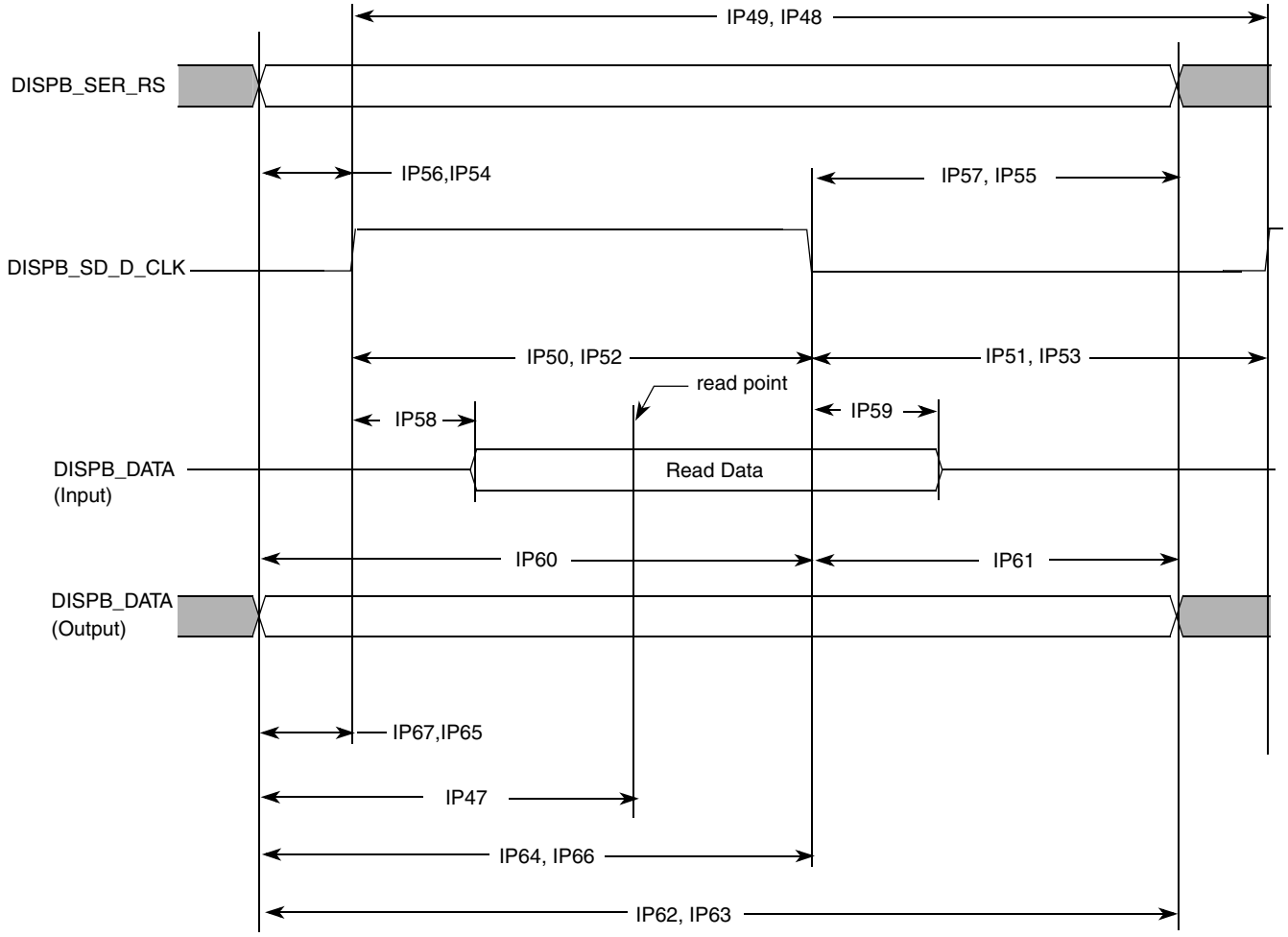

Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

Table 60. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 61.

Table 61. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in Table 8.

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 62. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}

Table 63. MLB Device 1024Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	— —	ns	PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	0.7	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	2	—	—	ns	Note[3]

1 The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.9.16 1-Wire Timing Specifications

Figure 70 depicts the RPP timing, and Table 64 lists the RPP timing parameters.

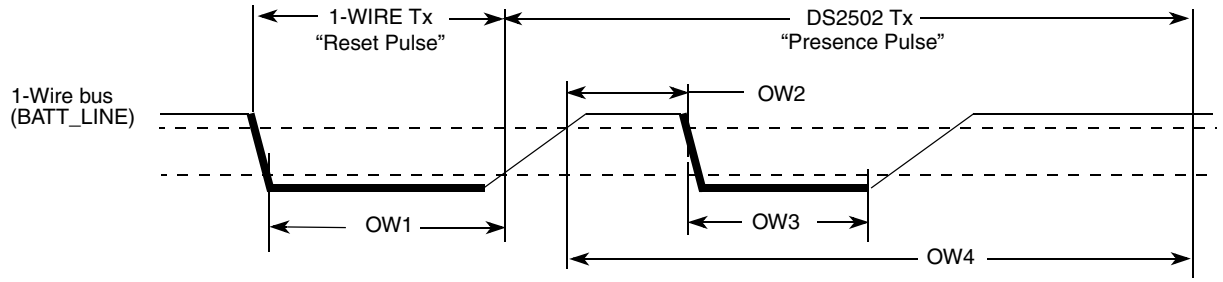

Figure 70. Reset and Presence Pulses (RPP) Timing Diagram

Table 64. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset time low	t_{RSTL}	480	511	—	µs
OW2	Presence detect high	t_{PDH}	15	—	60	µs
OW3	Presence detect low	t_{PDL}	60	—	240	µs
OW4	Reset time high	t_{RSTH}	480	512	—	µs

Figure 81. UDMA-In Device Terminates Transfer Timing Diagram

Table 72. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 79, Figure 80, Figure 81	Description	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew > T	T big enough
trp	trp	trp (min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff large enough to avoid bus contention.

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS	L17
D3_DRDY	L20
D3_FPSHIFT	L15
D3_HSYNC	L18
D3_REV	M17
D3_SPL	M18
D3_VSYNC	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
SDCKE1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3

Signal ID	Ball Location
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0	F20
LD1	G18
LD10	H20
LD11	J18
LD12	J16
LD13	J19
LD14	J17
LD15	J20
LD16	K14
LD17	K19
LD18	K18
LD19	K20
LD2	G17
LD20	K16
LD21	K17
LD22	K15
LD23	L19
LD3	G16
LD4	G19
LD5	H16
LD6	H18
LD7	G20
LD8	H17
LD9	H19

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