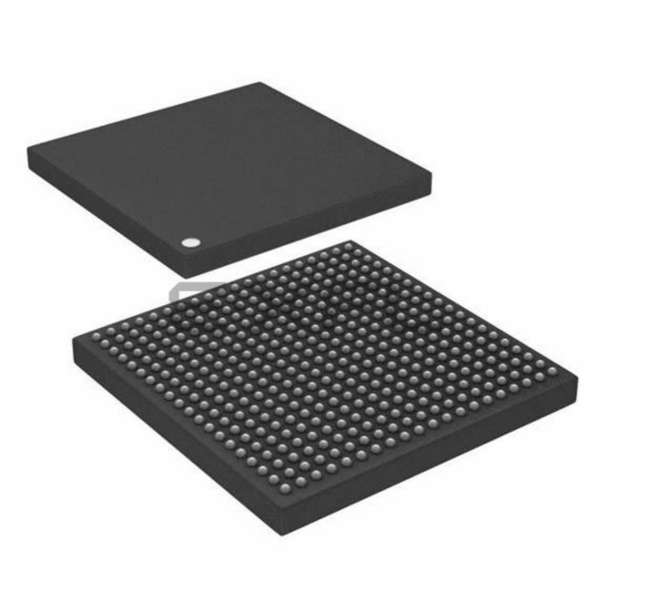

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx353djq5cr2

SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU) (not available for the MCIMX351)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface (CE-ATA is not available for the MCIMX351)
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
$I^2C(3)$	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).

Table 12. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	R_{eJA}	53	ºC/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	R_{eJA}	30	ºC/W
Junction to ambient[1] (at 200 ft/min)	Single layer board (1s)	R_{eJMA}	44	ºC/W
Junction to ambient[1] (at 200 ft/min)	Four layer board (2s2p)	R_{eJMA}	27	ºC/W
Junction to boards[2]	—	R_{eJB}	19	ºC/W
Junction to case (top)[3]	—	R_{eJCtop}	10	ºC/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	ºC/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.7 I/O Pin DC Electrical Characteristics

I/O pins are of two types: GPIO and DDR. DDR pins can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high, and max.

Table 13 shows currents for the different DDR pin drive strength modes.

Table 13. DDR Pin Drive Strength Mode Current Levels

Drive Mode	Normal	High	Max.
Mobile DDR (1.8 V)	3.6 mA	7.2 mA	10.8 mA
SDRAM (1.8 V)	—	—	6.5 mA
SDRAM (3.3 V)	4 mA	8 mA	12 mA
DDR2 (1.8 V)	—	—	13.4 mA

Table 17. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0/79 0.36/0.49	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

Table 18. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode for [NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

Table 19. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 20. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

Figure 41 shows MII asynchronous input timings listed in Table 50.

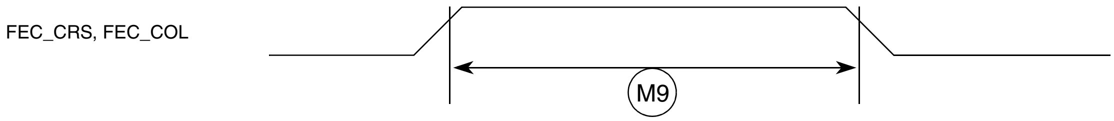

Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 42 shows MII serial management channel timings listed in Table 51.

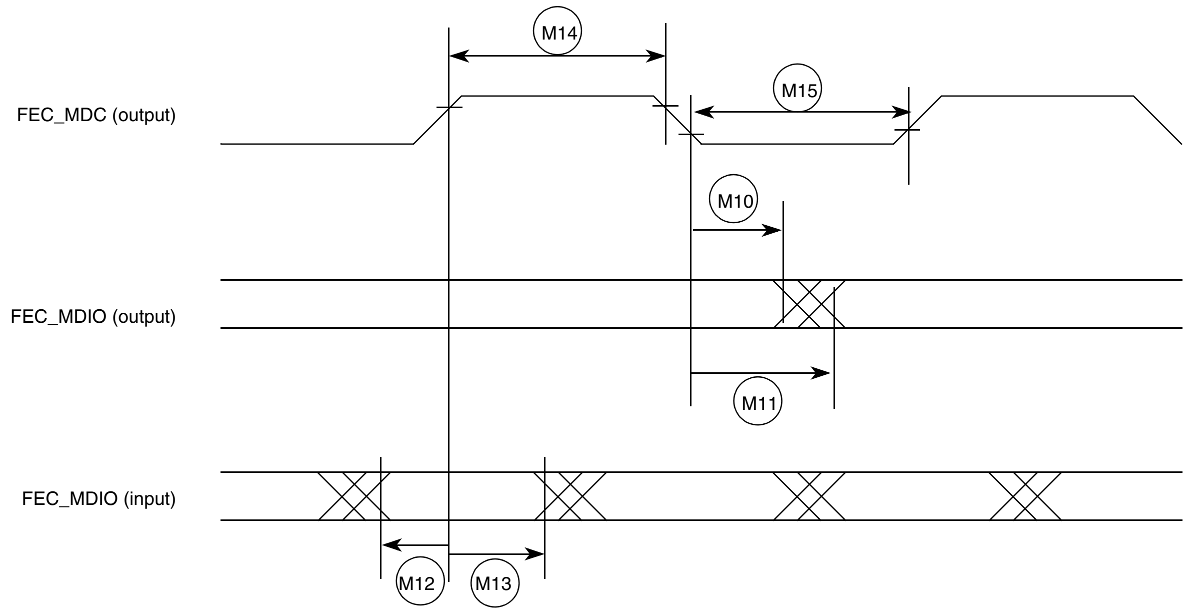

Figure 42. MII Serial Management Channel Timing Diagram

4.9.9 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) defined by IrDA® (Infrared Data Association). Refer to the IrDA® website for details on FIR and MIR protocols.

4.9.10 FlexCAN Module AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver outside the chip. The i.MX35 has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. Refer to the IOMUX chapter of the *MCIMX35 Multimedia Applications Processor Reference Manual* to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

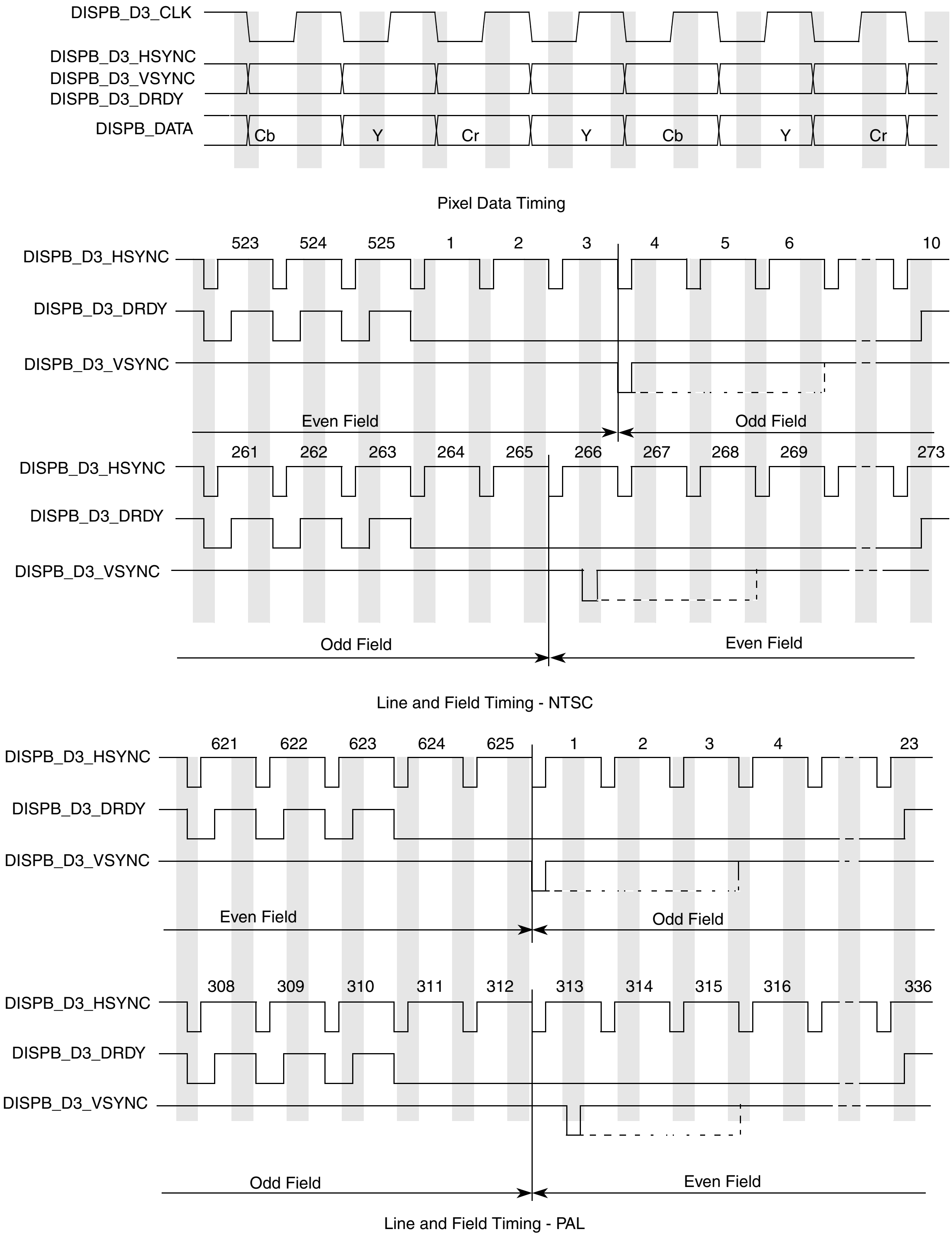

Figure 52. TV Encoder Interface Timing Diagram

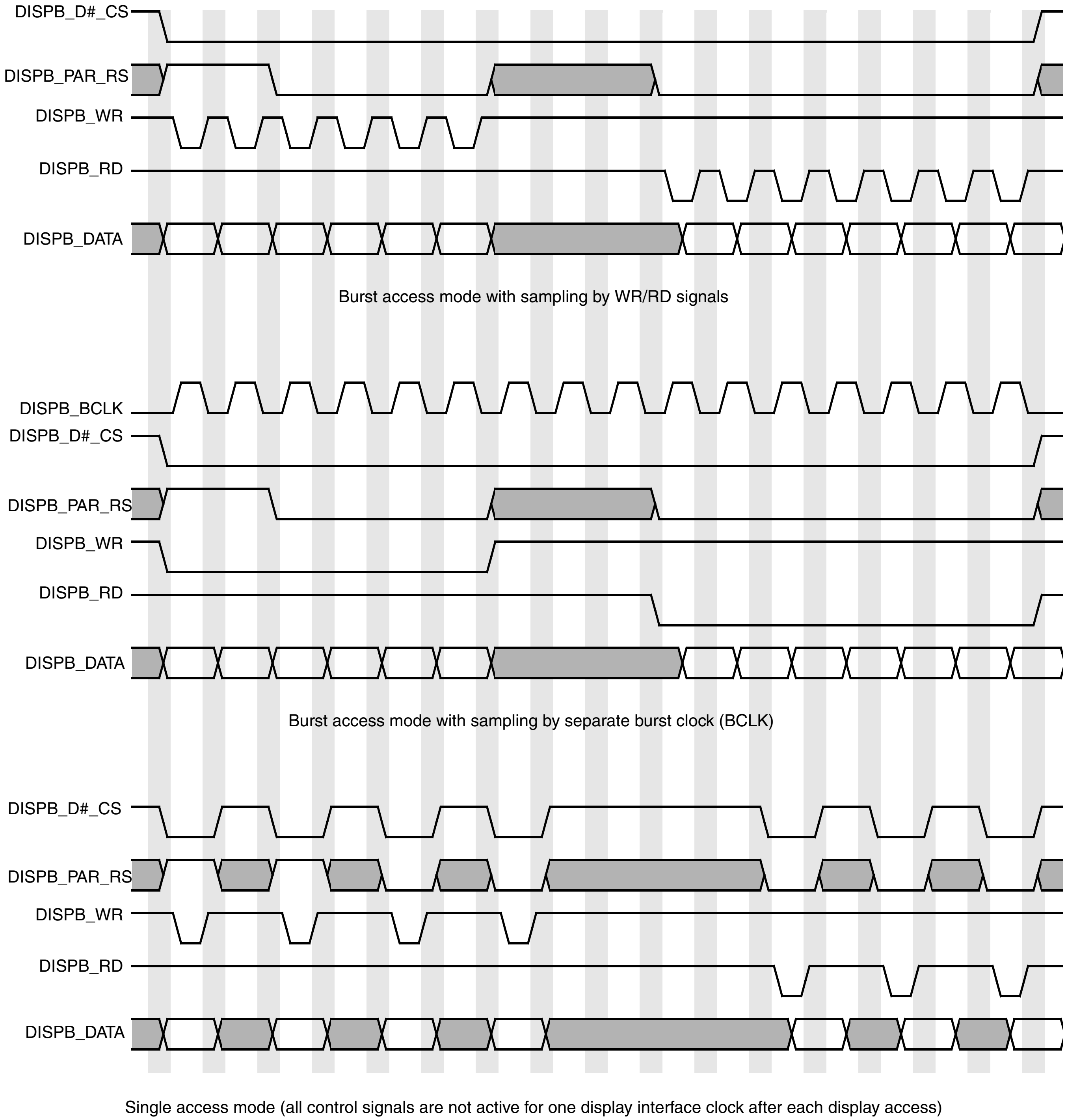

Figure 54. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

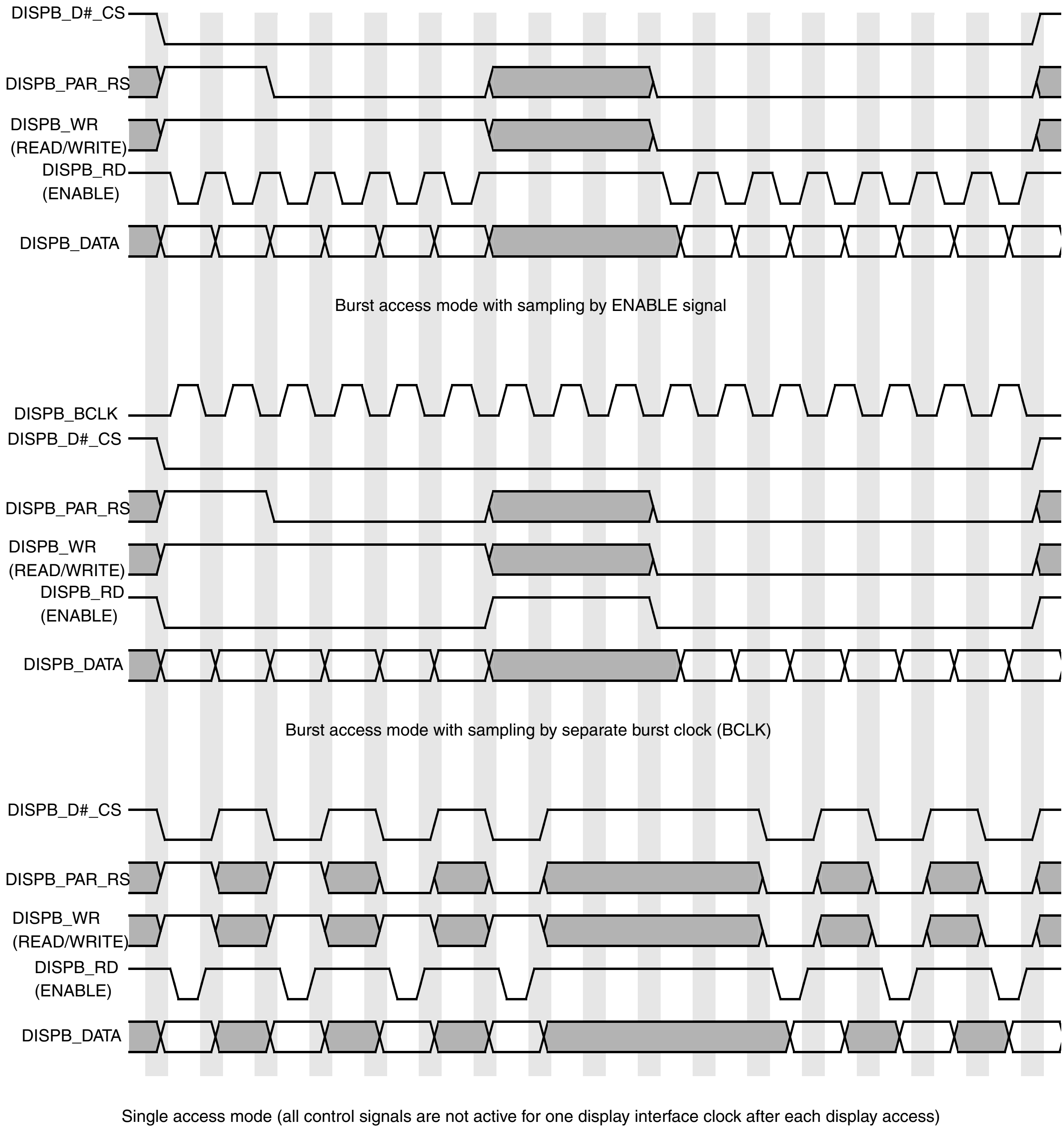

Figure 56. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the

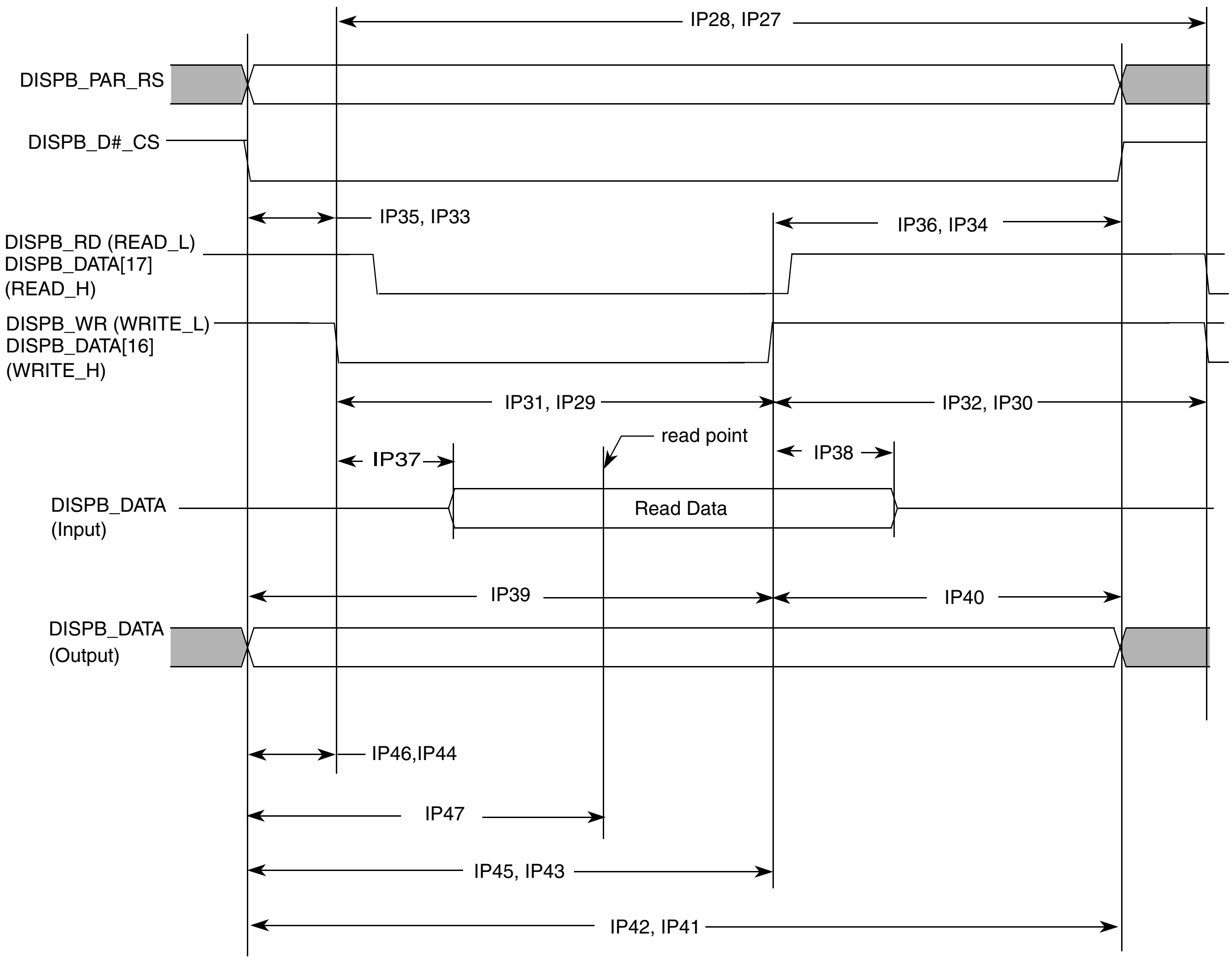

Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

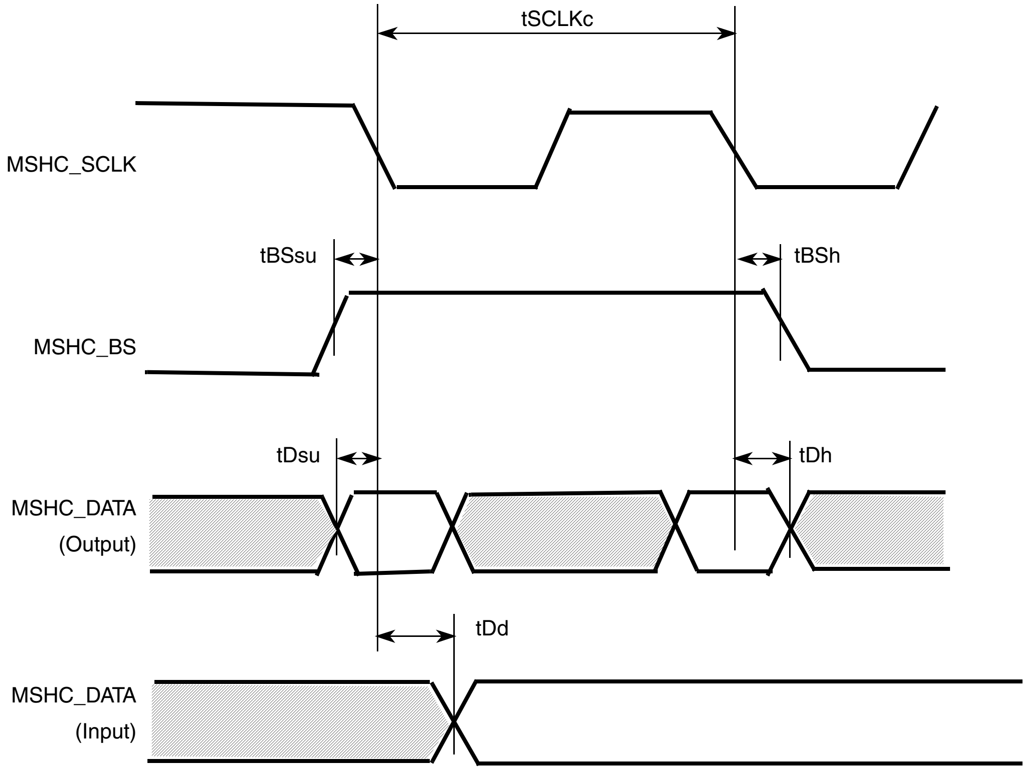

Figure 69. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 60. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 63. MLB Device 1024Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	— —	ns	PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	0.7	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	2	—	—	ns	Note[3]

1 The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.9.16 1-Wire Timing Specifications

Figure 70 depicts the RPP timing, and Table 64 lists the RPP timing parameters.

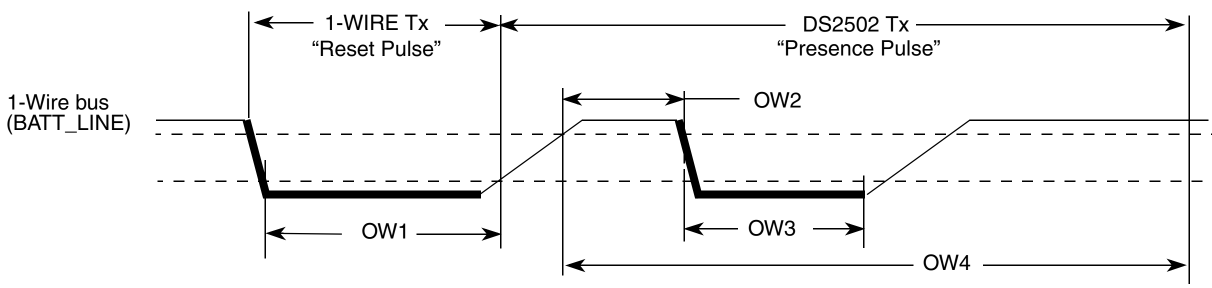

Figure 70. Reset and Presence Pulses (RPP) Timing Diagram

Table 64. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset time low	t_{RSTL}	480	511	—	µs
OW2	Presence detect high	t_{PDH}	15	—	60	µs
OW3	Presence detect low	t_{PDL}	60	—	240	µs
OW4	Reset time high	t_{RSTH}	480	512	—	µs

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes (not available for the MCIMX351). Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 67 and Figure 74 define the AC characteristics of the interface signals on all data transfer modes.

Table 67. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface[1]	S_{rise}[1]	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface[1]	S_{fall}[1]	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

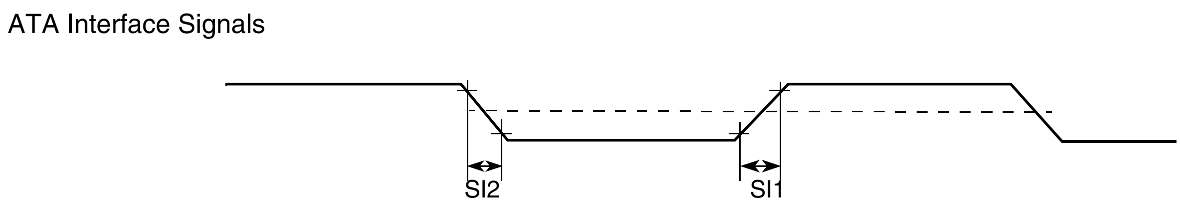

Figure 74. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When

Figure 76 shows timing for PIO write, and Table 70 lists the timing parameters for PIO write.

Figure 76. PIO Write Timing Diagram

Table 70. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 76	Value	Controlling Variable
t1	t1	t1 (min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 84. UDMA-Out Device Terminates Transfer Timing Diagram

Table 73. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 82, Figure 83, Figure 84	Value	Controlling Variable
tack	tack	tack (min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min.) = (time_env × T) – (tskew1 + tskew2) tenv (max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs ×T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli = max. (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

Table 80. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 82. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate}$ + T_{ref_clk}	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.9.23.1.12 UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 83 lists serial mode receive timing characteristics.

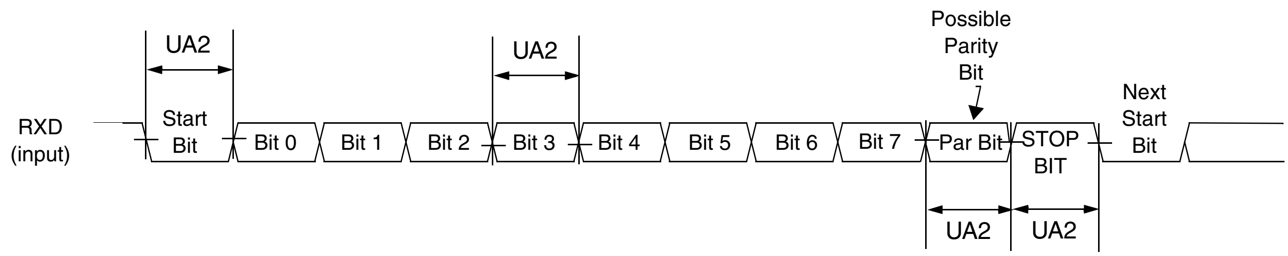

Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 83. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency) ÷ 16.

4.9.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.9.23.2.13 UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 84 lists the transmit timing characteristics.

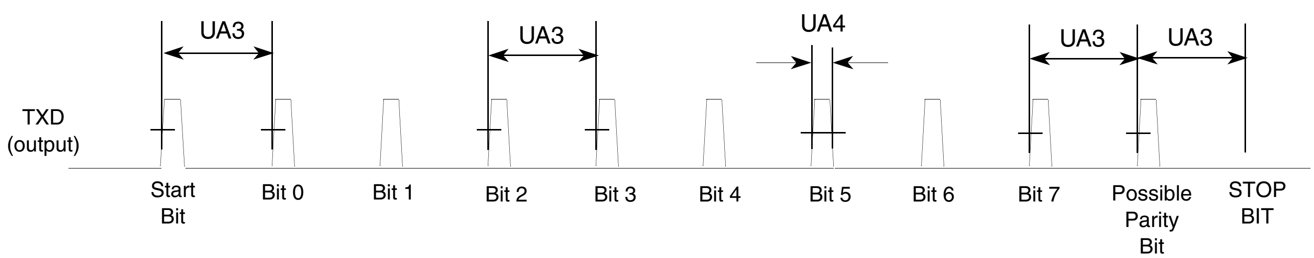

Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3
MA10	C4
MGND	N11
MLB_CLK	W13
MLB_DAT	Y13
MLB_SIG	W12
MVDD	P11
NF_CE0	G3
NFALE	F2
NFCLE	E1
NFRB	F3
NFRE_B	F1
NFWE_B	G2
NFWP_B	F4
NGND_ATA	M9
NGND_ATA	P9
NGND_ATA	L10
NGND_CRM	L11
NGND_CSI	N10
NGND_EMI1	H8
NGND_EMI1	H10
NGND_EMI1	J10
NGND_EMI2	J11
NGND_EMI3	J12
NGND_EMI3	K12
NGND_JTAG	M13
NGND_LCDC	K11
NGND_LCDC	L12
NGND_MISC	M7
NGND_MISC	K8
NGND_MLB	M10
NGND_NFC	K9
NGND_SDIO	N12
NVCC_ATA	N6
NVCC_ATA	P6
NVCC_ATA	P7
NVCC_ATA	P8
NVCC_CRM	R9
NVCC_CSI	R11

Signal ID	Ball Location
LD23[1]	L19
LD3[1]	G16
LD4[1]	G19
LD5[1]	H16
LD6[1]	H18
LD7[1]	G20
LD8[1]	H17
LD9[1]	H19
NVCC_EMI2	G12
NVCC_EMI2	F13
NVCC_EMI2	F14
NVCC_EMI3	G14
NVCC_JTAG	P16
NVCC_LCDC	H14
NVCC_LCDC	J14
NVCC_LCDC	L14
NVCC_LCDC	M14
NVCC_MISC	K6
NVCC_MISC	K7
NVCC_MISC	L8
NVCC_MLB	R10
NVCC_NFC	G6
NVCC_NFC	H6
NVCC_NFC	H7
NVCC_SDIO	P14
OE	E20
OSC_AUDIO_VDD	V20
OSC_AUDIO_VSS	U19
OSC24M_VDD	T19
OSC24M_VSS	T18
PGND	M12
PHY1_VDDA	M15
PHY1_VDDA	N20
PHY1_VSSA	N16
PHY1_VSSA	P20
PHY2_VDD	R13
PHY2_VSS	P12
POR_B	W11
POWER_FAIL	Y9
PVDD	N13
RAS	E15
RESET_IN_B	U10
RTCK	U18
RTS1	U1
RTS2	G1
RW	C20

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