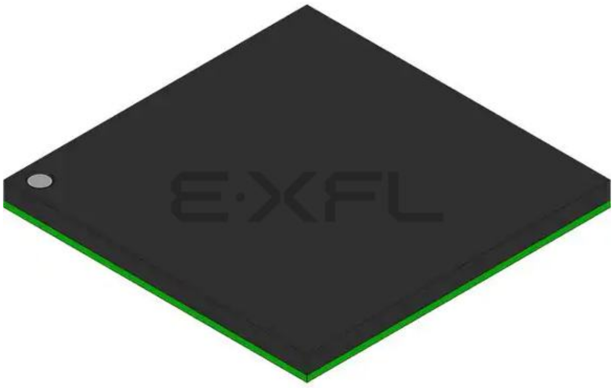

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx353dvm5b

SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU) (not available for the MCIMX351)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface (CE-ATA is not available for the MCIMX351)
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)

Stresses beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Table 8 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	VDD_{max}[1]	–0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	–0.5	3.6	V
Input voltage range	V_{Imax}	–0.5	3.6	V
Storage temperature	$T_{storage}$	–40	125	^{o}C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000[2]	
Charge Device Model (CDM)		—	500[3]	

1 VDD is also known as QVCC.

2 HBM ESD classification level according to the AEC-Q100-002 standard

3 Corner pins max. 750 V

4.1.1 i.MX35 Operating Ranges

Table 8 provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 8. i.MX35 Operating Ranges

Parameter	Symbol	Min.	Typical	Max.	Units
Core Operating Voltage 0 < f_{ARM} < 400 MHz	V_{DD}	1.22	—	1.47	V
Core Operating Voltage 0 < f_{ARM} < 532 MHz		1.33	—	1.47	V
State Retention Voltage		1	—	—	V
EMI[1]	NVCC_EMI1,2,3	1.7	—	3.6	V
WTDG, Timer, CCM, CSPI1	NVCC_CRM	1.75	—	3.6	V
NANDF	NVCC_NANDF	1.75	—	3.6	V
ATA, USB generic	NVCC_ATA	1.75	—	3.6	V
eSDHC1	NVCC_SDIO	1.75	—	3.6	V
CSI, SDIO2	NVCC_CSI	1.75	—	3.6	V
JTAG	NVCC_JTAG	1.75	—	3.6	V
LCDC, TTM, I2C1	NVCC_LCDC	1.75	—	3.6	V

Table 33. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Address valid to Clock rise/fall	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to CSx_B valid	15	19	ns
WE7	Clock rise/fall to CSx_B invalid	3.6	5	ns
WE8	Clock rise/fall to RW_B valid	8	12	ns
WE9	Clock rise/fall to RW_B invalid	3	8	ns
WE10	Clock rise/fall to OE_B valid	7	12	ns
WE11	Clock rise/fall to OE_B invalid	3.8	5.5	ns
WE12	Clock rise/fall to EBy_B valid	6	11.5	ns
WE13	Clock rise/fall to EBy_B invalid	6	10	ns
WE14	Clock rise/fall to LBA_B valid	17.5	20	ns
WE15	Clock rise/fall to LBA_B invalid	0	1	ns
WE16	Clock rise/fall to Output Data valid	5	10	ns
WE17	Clock rise to Output Data invalid	0	2.5	ns
WE18	Input Data Valid to Clock rise[3]	1	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is ECB_B asserted during access)	(BCLK/2) + 3.01	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is NO ECB_B asserted during access)	6.9	—	ns
WE20	Clock rise to Input Data invalid[3]	1	—	ns
WE22	ECB_B setup time[3]	5	—	ns
WE24	ECB_B hold time[3]	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	–3.2	—	ns

1 “High” is defined as 80% of signal value, and “low” is defined as 20% of signal value.
2 BCLK parameters are measured from the 50% point. For example, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.
3 Parameters W18, W20, W22, and W24 are tested when FCE=1. i.MX35 does not support FCE=0.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

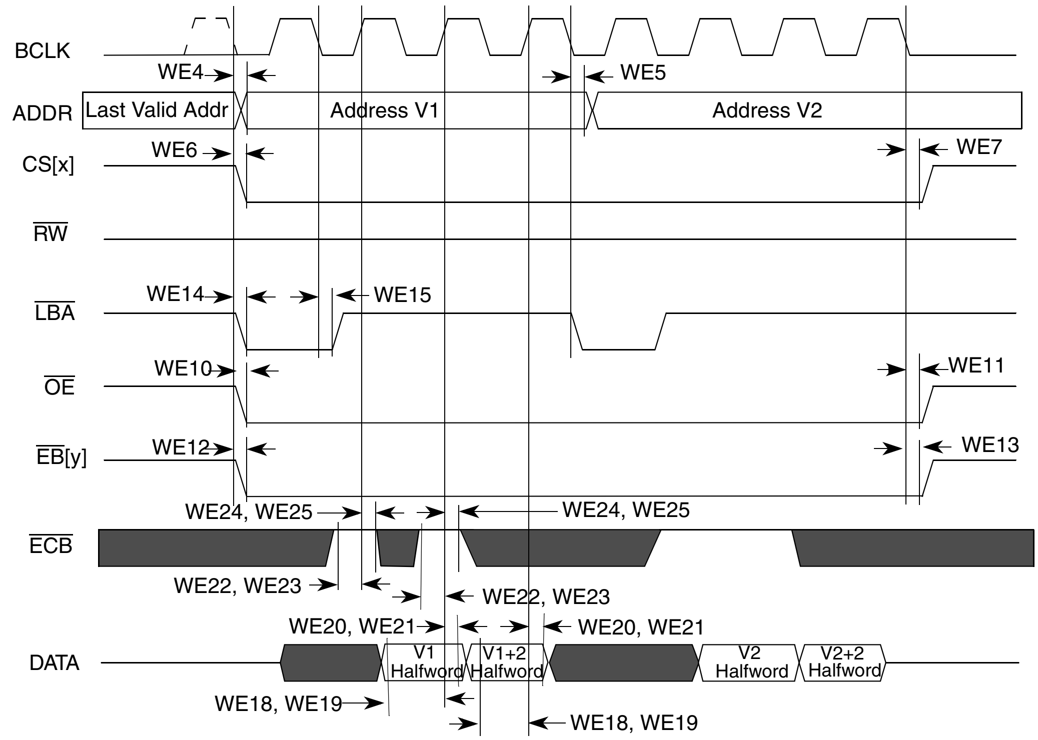

Figure 18. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses— WSC = 2, SYNC = 1, DOL = 0

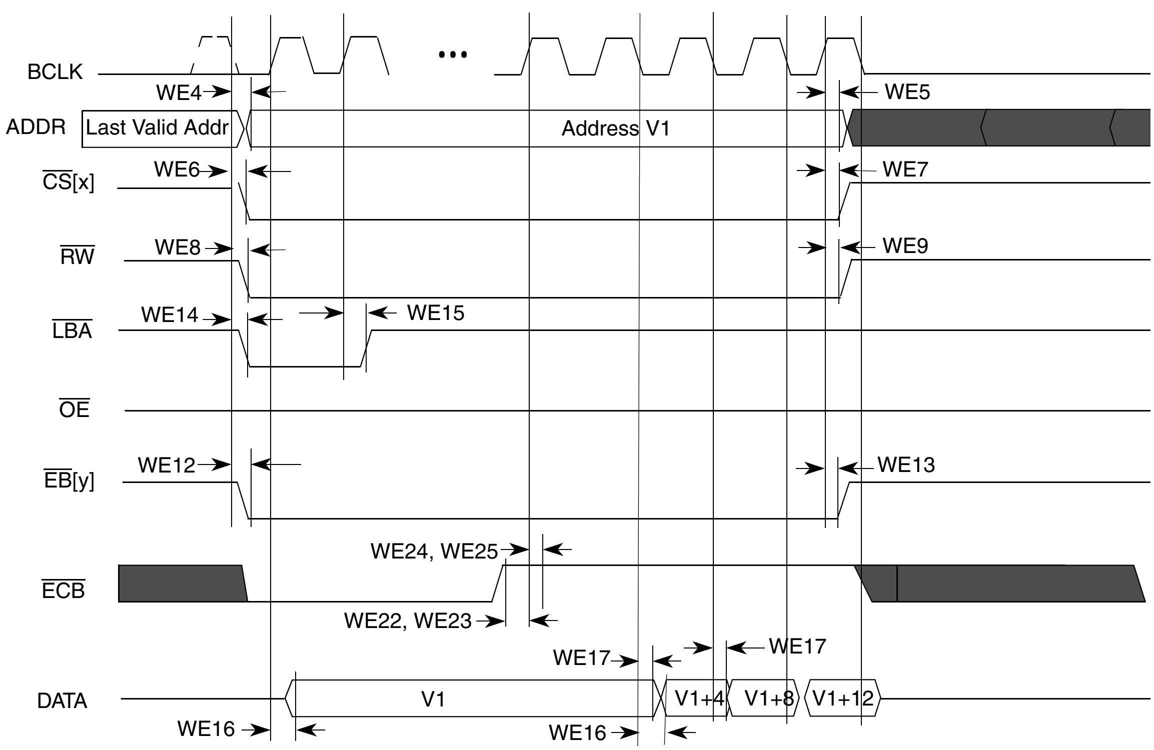

Figure 19. Synchronous Memory TIming Diagram for Burst Write Access— BCS = 1, WSC = 4, SYNC = 1, DOL = 0, PSR = 1

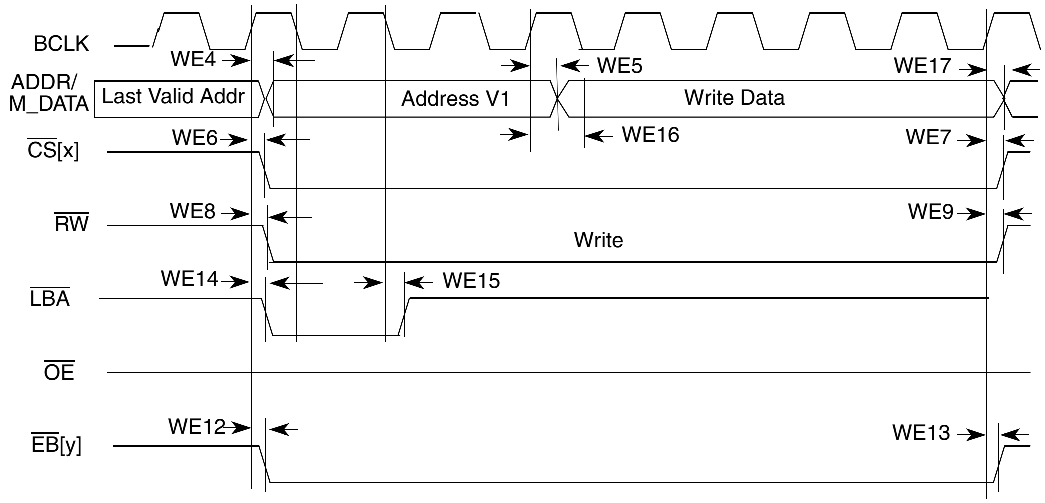

Figure 20. Muxed A/D Mode Timing Diagram for Synchronous Write Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1

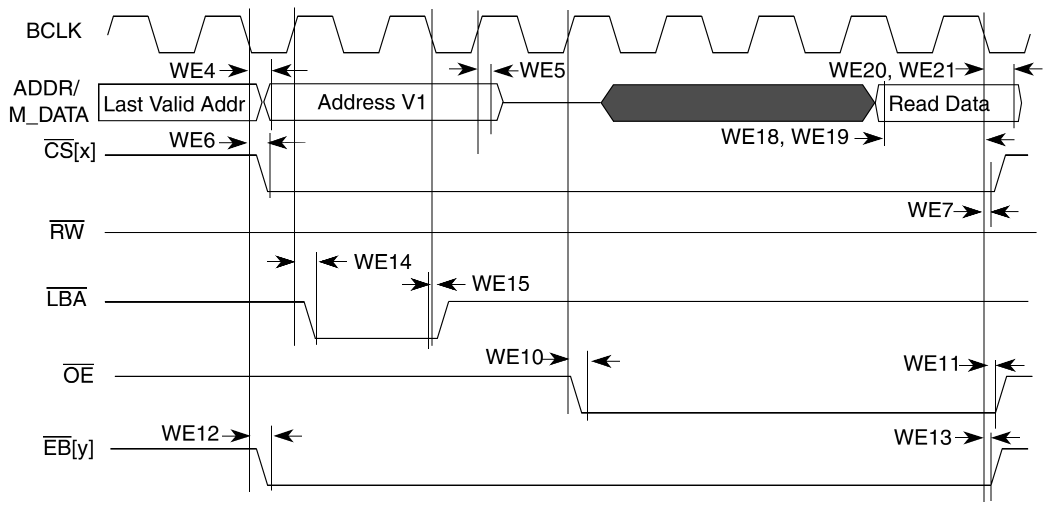

Figure 21. Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7

Figure 22 through Figure 26, and Table 34 help to determine timing parameters relative chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

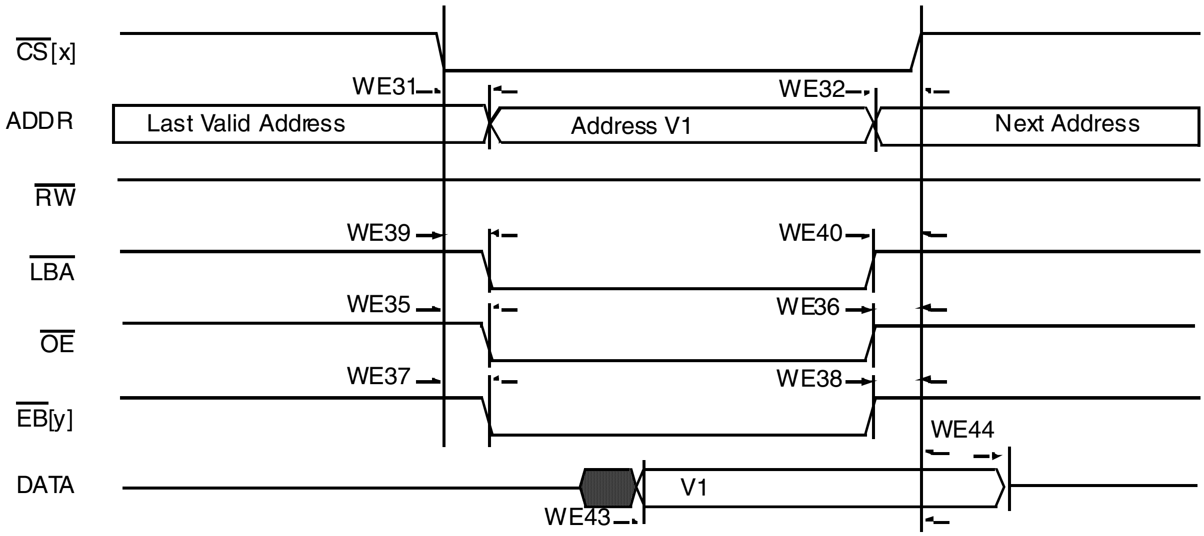

Figure 22. Asynchronous Memory Read Access

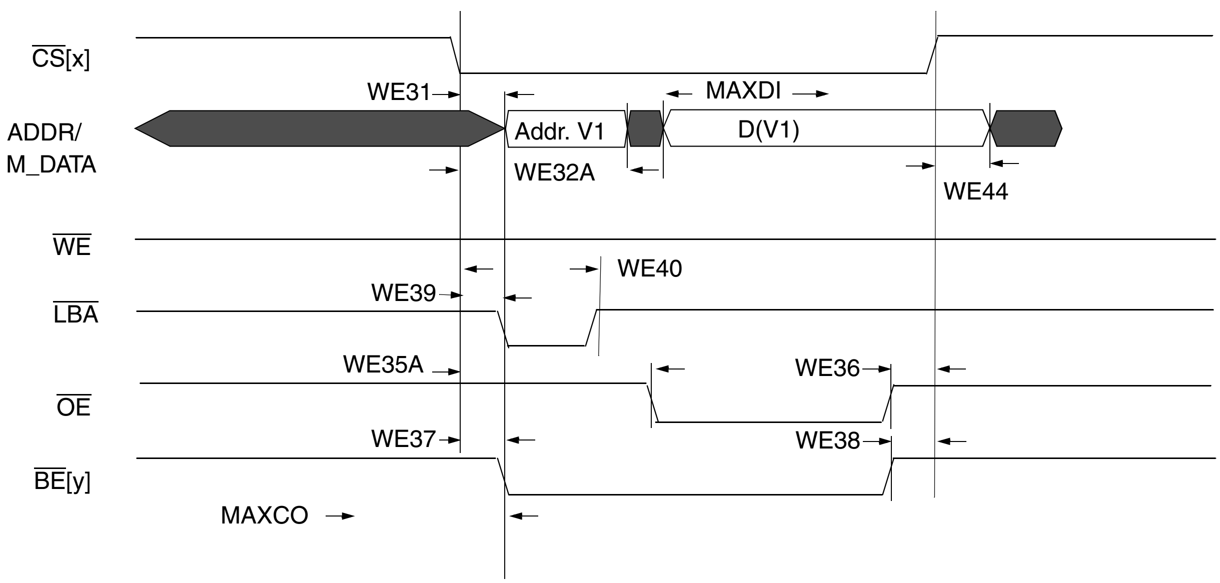

Figure 23. Asynchronous A/D muxed Read Access (RWSC = 5)

Table 43. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS[1]	tQH	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	tDQSCK	–0.5	0.5	ns

[1]The value was calculated for an SDCLK frequency of 133 MHz by the formula tQH = tHP – tQHS = min (tCL,tCH) – tQHS = 0.45 × tCK – tQHS = 0.45 × 7.5 – 0.45 = 2.925 ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

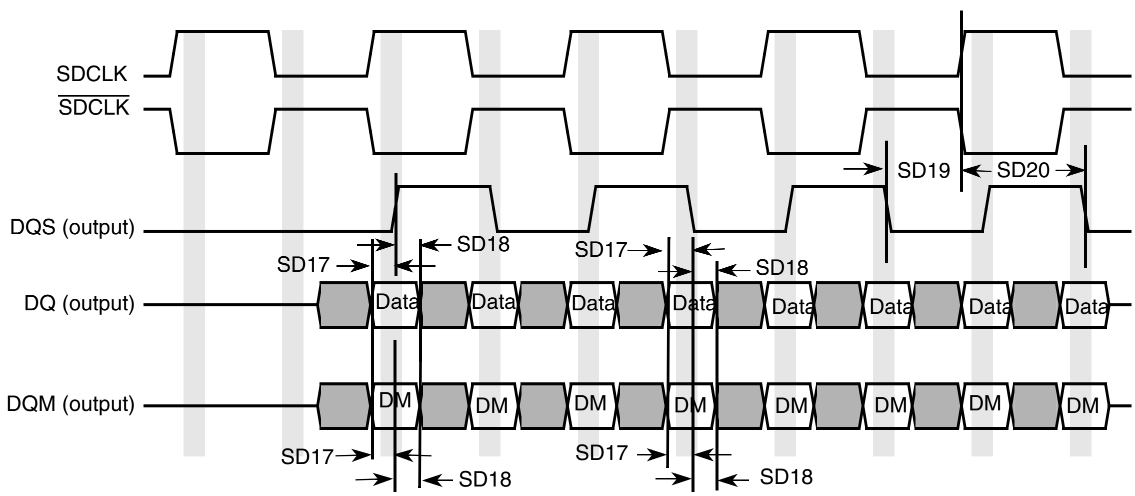

Figure 34. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 44. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

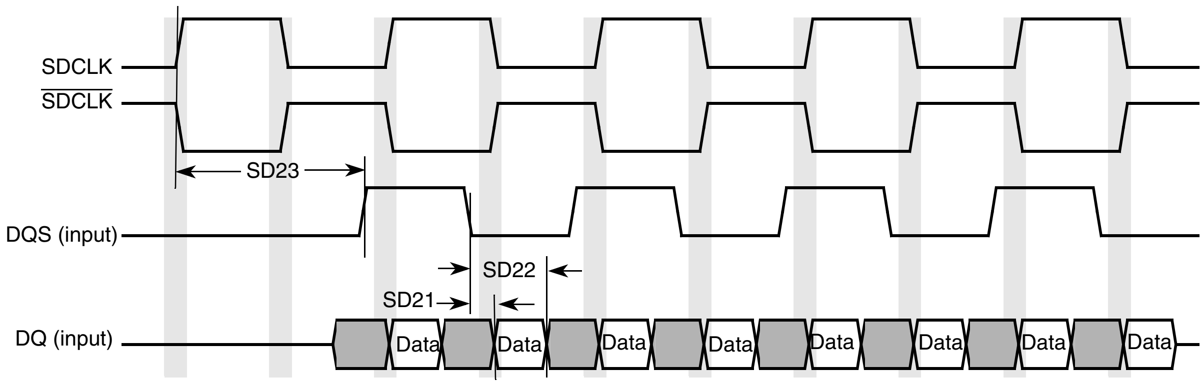

Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

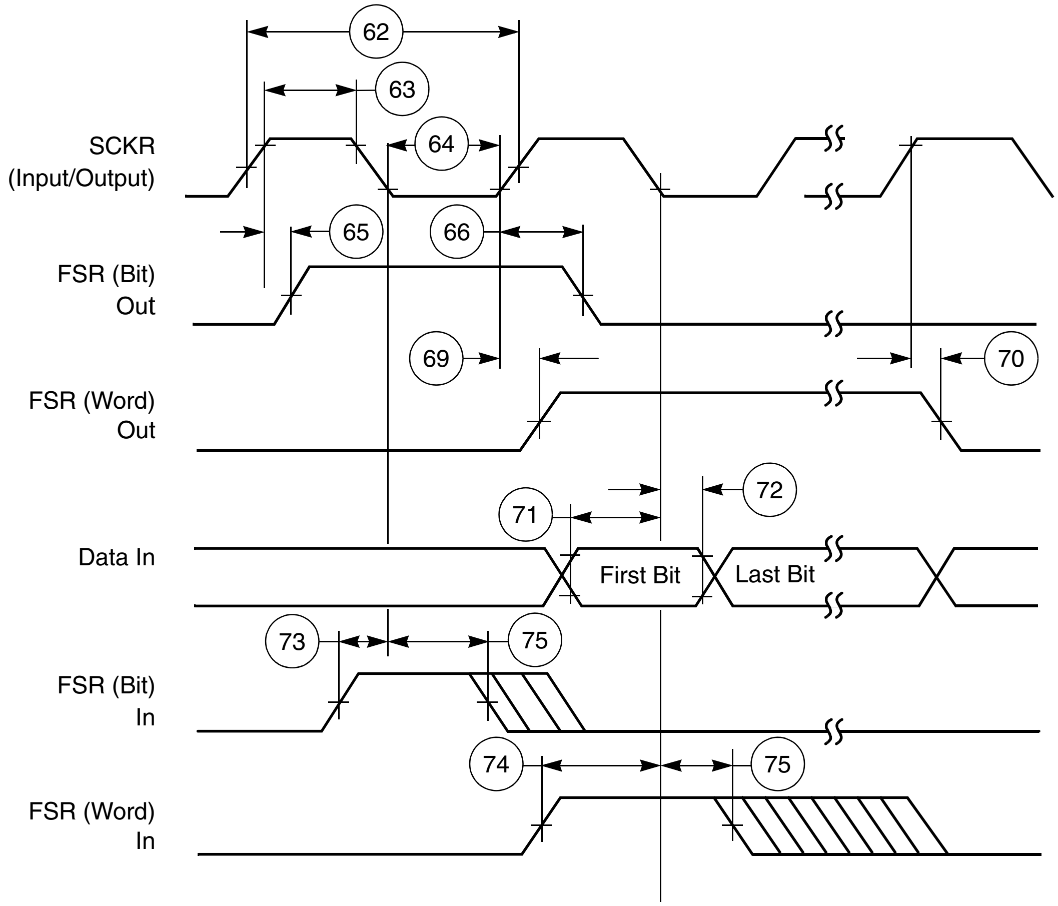

Figure 37. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 38 depicts the timing of eSDHCv2, and Table 47 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 47:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

The timing described in Figure 45 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.9.12.3 Electrical Characteristics

Figure 46 depicts the sensor interface timing, and Table 54 lists the timing parameters.

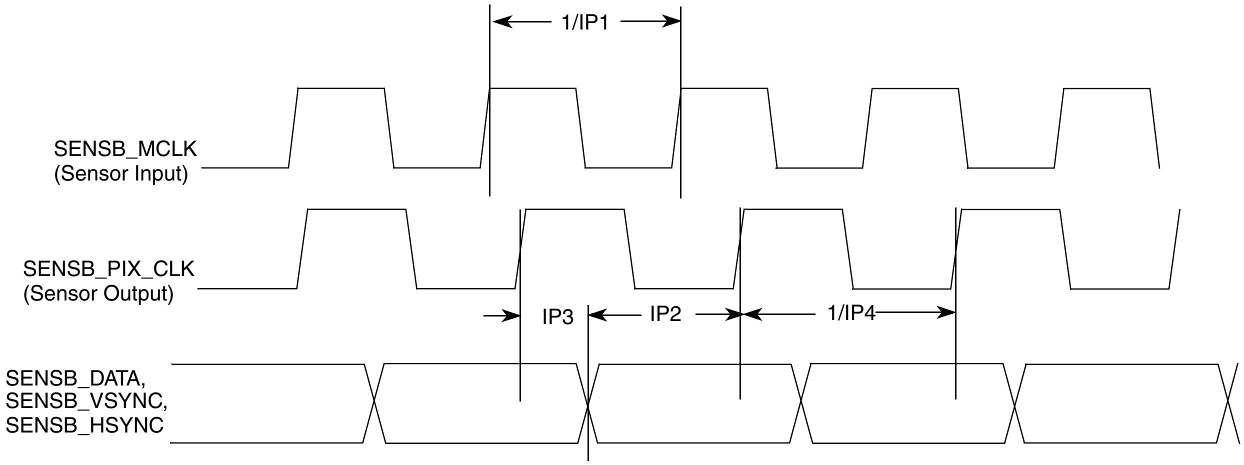

Figure 46. Sensor Interface Timing Diagram

Table 54. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.9.13 IPU—Display Interfaces

This section describes the following types of display interfaces:

- Section 4.9.13.1, “Synchronous Interfaces”
- Section 4.9.13.2, “Interface to Sharp HR-TFT Panels”
- Section 4.9.13.3, “Synchronous Interface to Dual-Port Smart Displays”
- Section 4.9.13.4, “Asynchronous Interfaces”
- Section 4.9.13.5, “Serial Interfaces, Functional Description”

of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

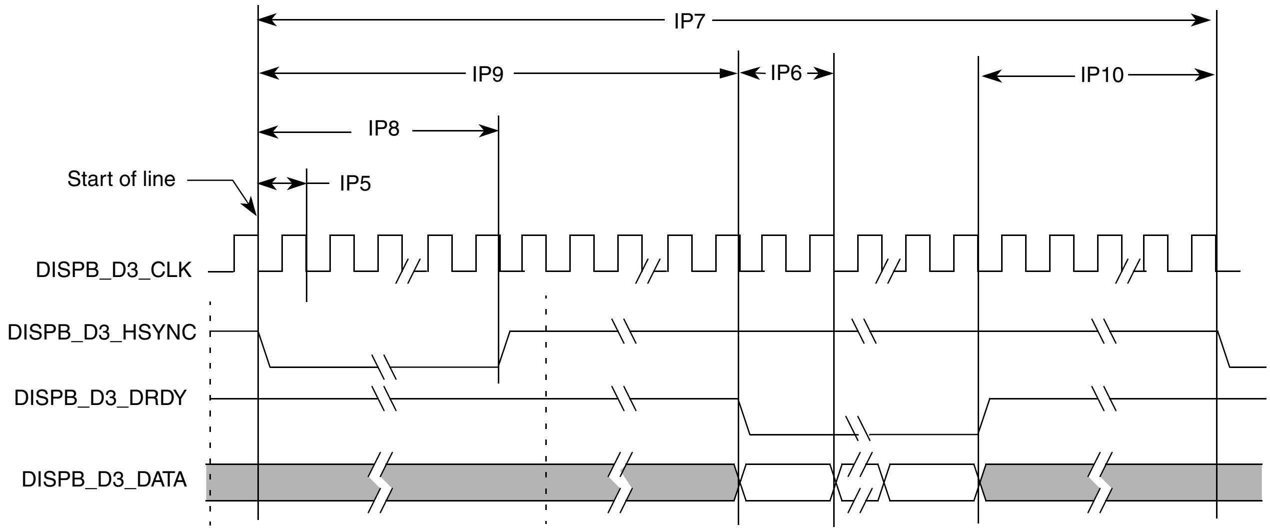

Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 49 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

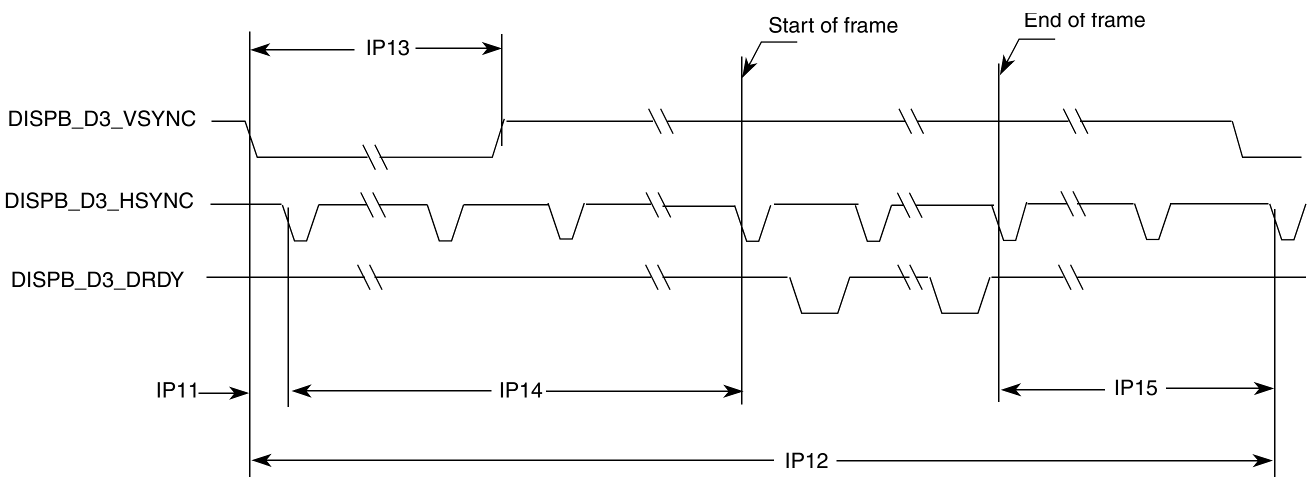

Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 55 shows timing parameters of signals presented in Figure 48 and Figure 49.

Table 55. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp[1]	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D + 1) × Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH + 1) × Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH + 1) × Tdpcp	ns

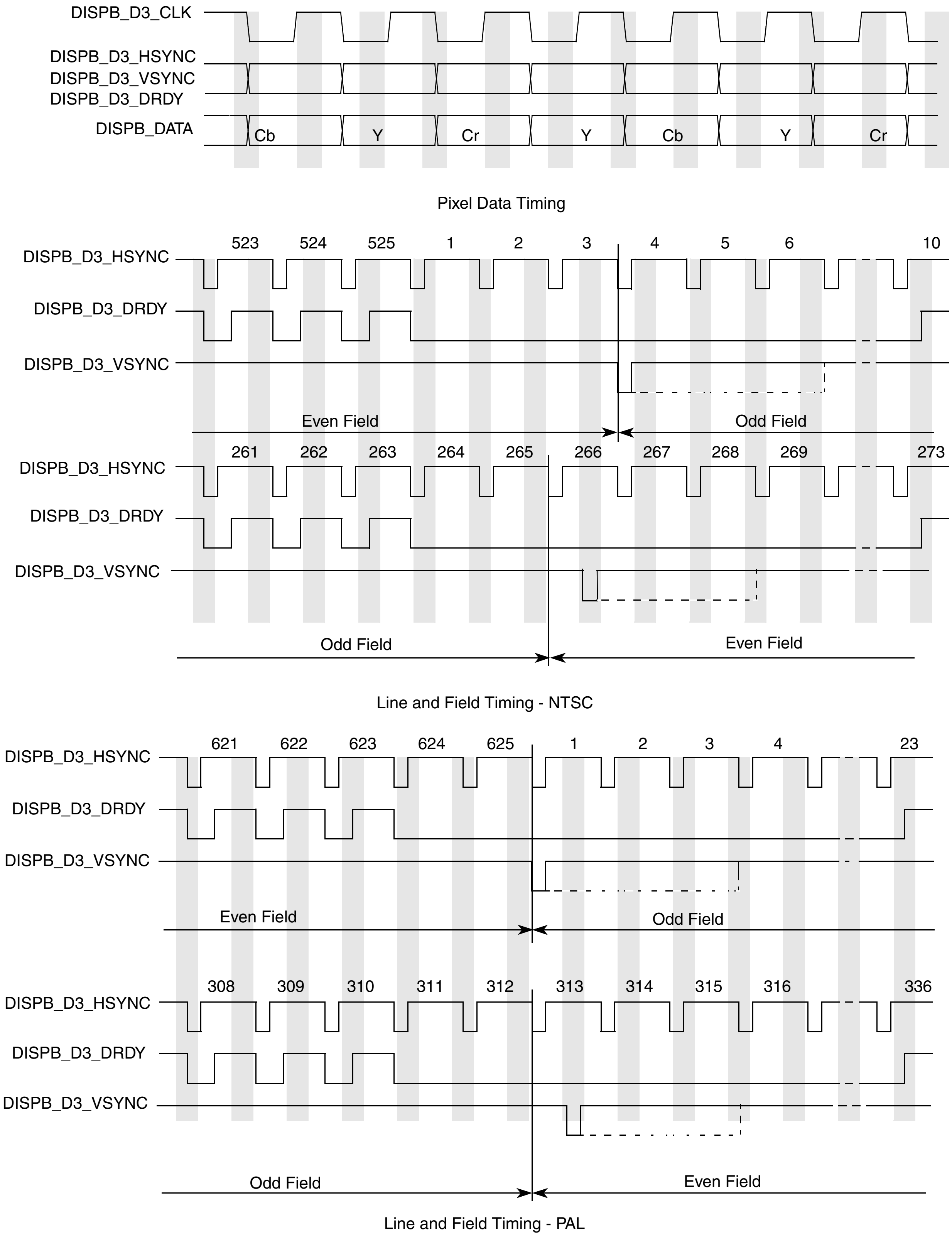

Figure 52. TV Encoder Interface Timing Diagram

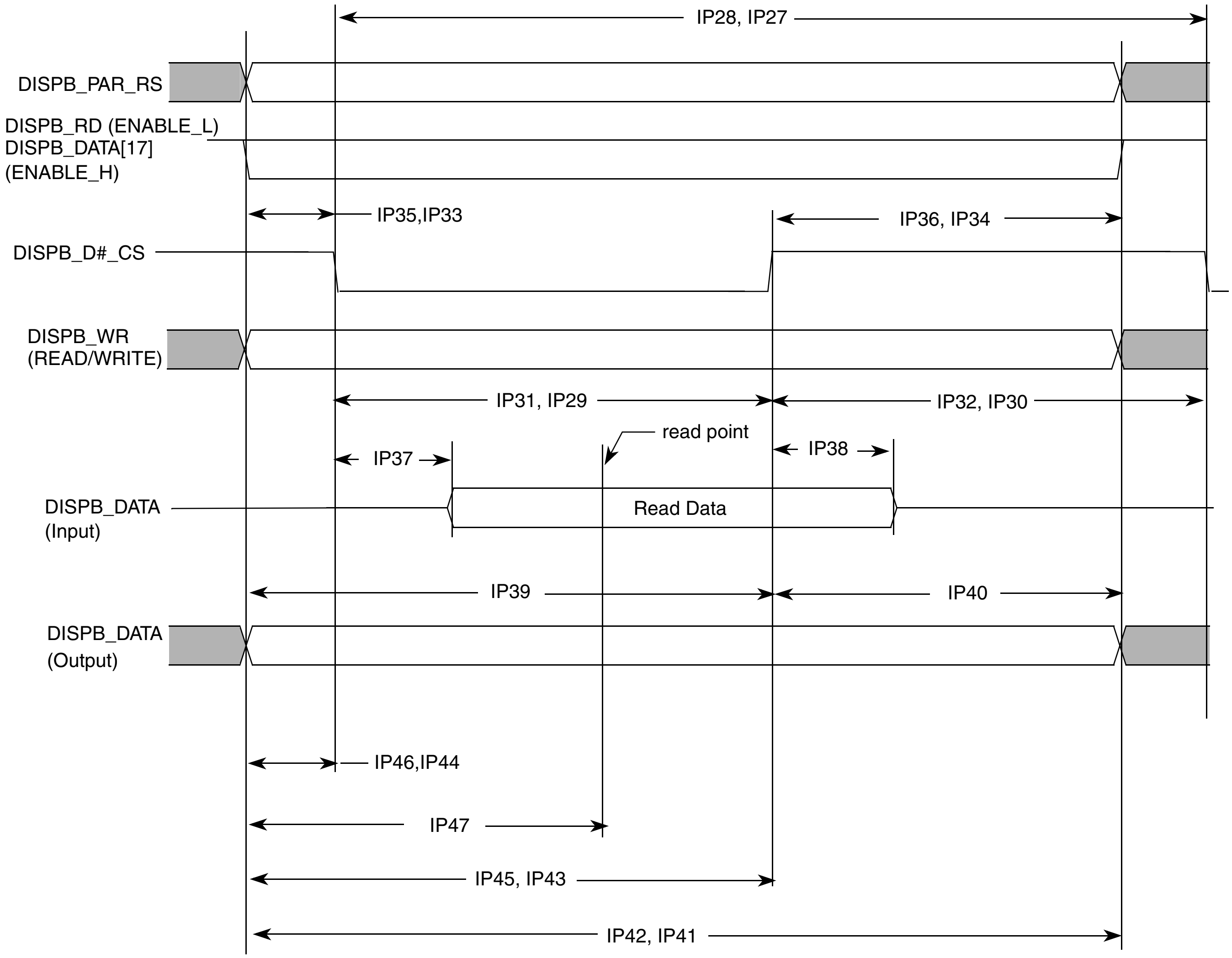

Figure 60. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

9 Data read point

$$\mathrm{Tdrp} = T_{\mathrm{HSP\_CLK}} \cdot \mathrm{ceil}\left[\frac{\mathrm{DISP\#\_READ\_EN}}{\mathrm{HSP\_CLK\_PERIOD}}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 62 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers (n = 1, 2).

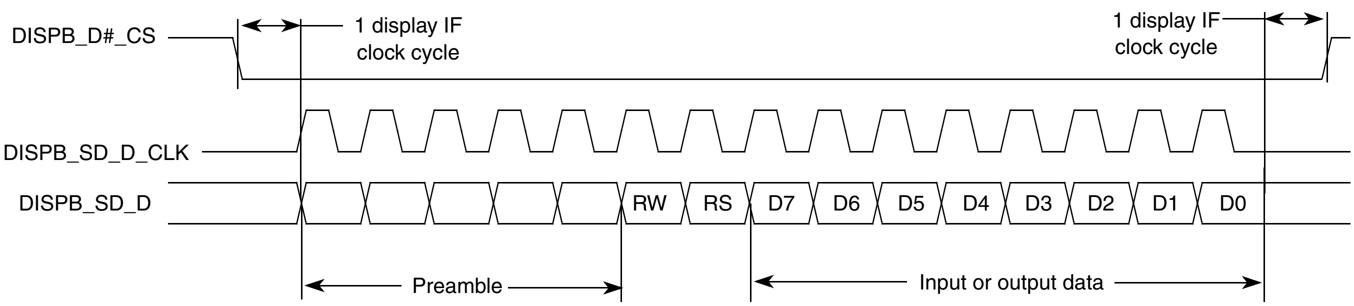

Figure 62. 3-Wire Serial Interface Timing Diagram

Figure 63 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

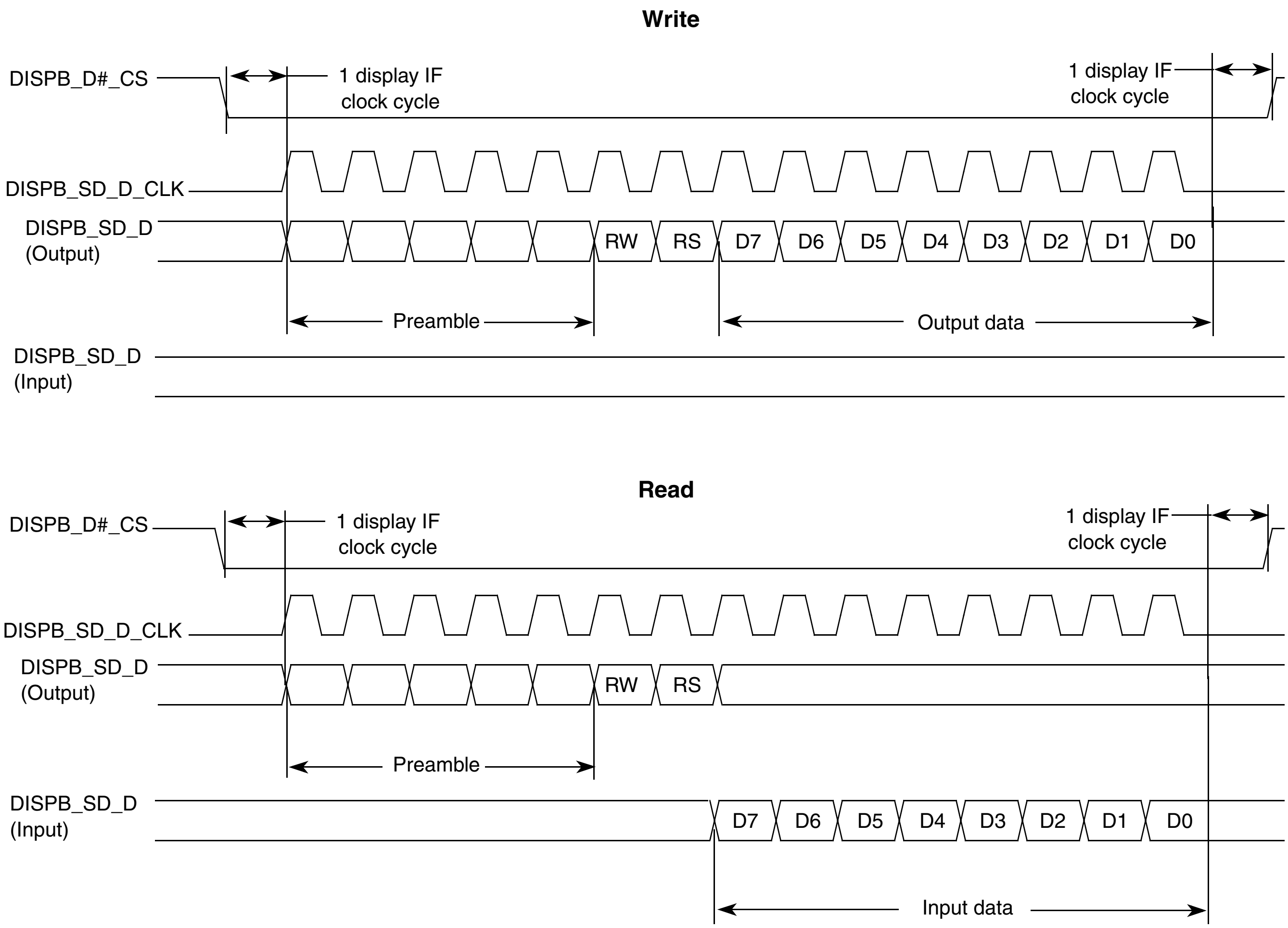

Figure 63. 4-Wire Serial Interface Timing Diagram

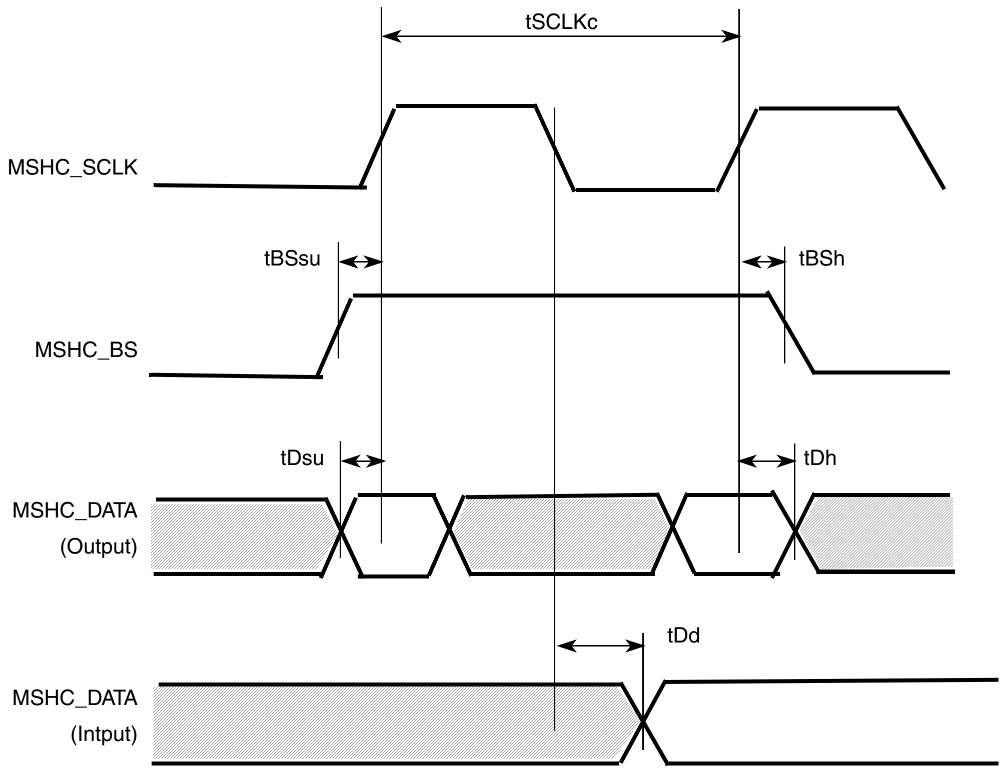

Figure 68. Transfer Operation Timing Diagram (Serial)

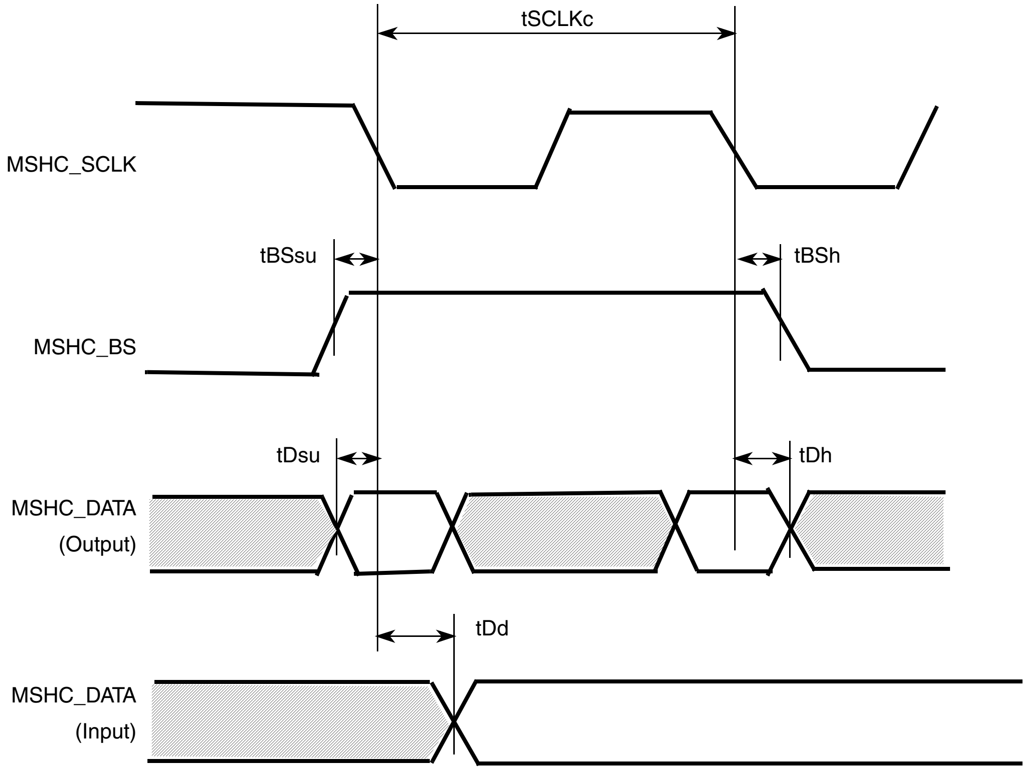

Figure 69. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 60. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 87 describes the port timing specification in DAT_SE0 bidirectional mode.

Table 87. Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.9.24.2 DAT_SE0 Unidirectional Mode

Table 88 defines the signals for DAT_SE0 unidirectional mode. Figure 102 and Figure 103 show the transmit and receive waveforms respectively.

Table 88. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

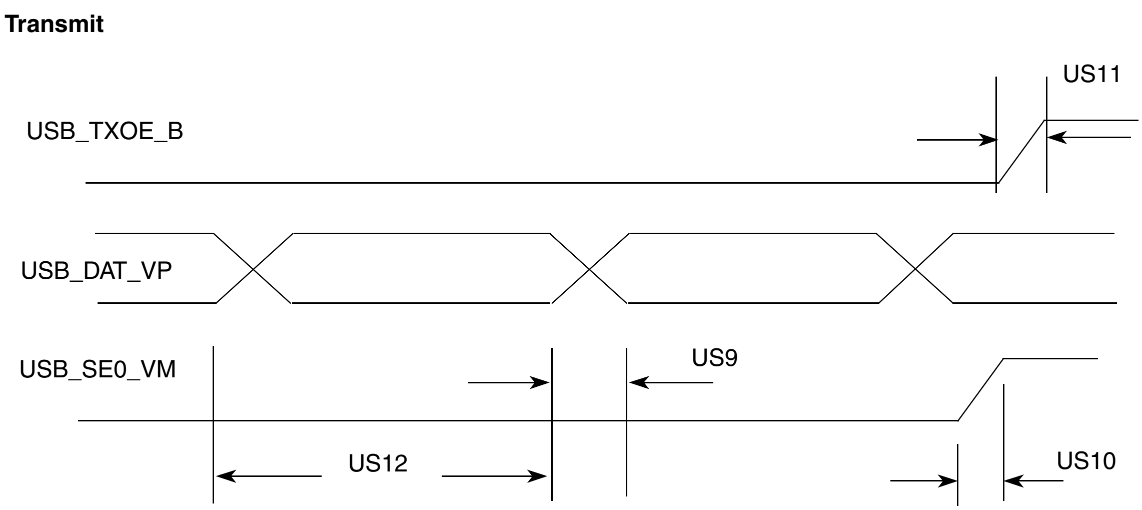

Figure 102. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_RREF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.

7 Revision History

Table 98 shows the revision history of this document. Note: There were no revisions of this document between revision 1 and revision 4 or between revision 6 and revision 7.

Table 98. i.MX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
10	06/2012	• In Table 2, "Functional Differences in the i.MX35 Parts," on page 3, added two columns for part numbers MCIMX353 and MCIMX357. • Added Table 29, "Clock Input Tolerance," on page 31 in Section 4.9.3, “DPLL Electrical Specifications.” • Updated Table 39, "DDR2 SDRAM Timing Parameter Table," on page 50 for DDR2-400 values. • Updated Table 41, "DDR2 SDRAM Write Cycle Parameters," on page 52 for DDR2-400 values. • Added Table 15, "AC Requirements of I/O Pins," on page 24. • Updated WE4 parameter in Table 33, "WEIM Bus Timing Parameters," on page 37.
9	08/2010	• Updated Table 32, “NFC Timing Parameters.” • Updated Table 33, “WEIM Bus Timing Parameters.”
8	04/2010	• Updated Table 14, “I/O Pin DC Electrical Characteristics.”
7	12/18/2009	• Updated Table 1, “Ordering Information.”
6	10/21/2009	• Added information for silicon rev. 2.1 • Updated Table 1, “Ordering Information.” • Added Table 95, “Silicon Revision 2.1 Signal Ball Map Locations.” • Added Table 97, “Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch.”
5	08/06/2009	• Added a line for T_A = –40 to 85 ^{o}C in Table 14, “I/O Pin DC Electrical Characteristics” • Filled in TBDs in Table 14. • Revised Figure 15 and Table 33 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table. • Added Table 26, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V).”
4	04/30/2009	Note: There were no revisions of this document between revision 1 and revision 4. • In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6. • Updated values in Table 10, “i.MX35 Power Modes.” • Added Section 4.4, “Reset Timing.” • In Section 4.8.2, “AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes),” removed Slow Slew rate tables, relabeled Table 24, “AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode,” and Table 25, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode,” to exclude mention of slew rate. • In Section 4.9.5.2, “Wireless External Interface Module (WEIM),” modified Figure 16, “Synchronous Memory Timing Diagram for Read Access—WSC = 1,” through Figure 21, “Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7.” • In Section 4.9.6, “Enhanced Serial Audio Interface (ESAI) Timing Specifications,” modified Figure 36, “ESAI Transmitter Timing,” and Figure 37, “ESAI Receiver Timing,” to remove extraneous signals. Removed a note from Figure 36, “ESAI Transmitter Timing.”
3	03/2009	• In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6.
2	02/2009	• Added the following parts to Table 1, “Ordering Information”: PCIMX357CVM5B, MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B. Throughout consumer data sheet: Removed or updated information related to Media Local Bus interface.Updated Section 4.3.1, “Powering Up.” • Updated values in Table 10, “i.MX35 Power Modes.”