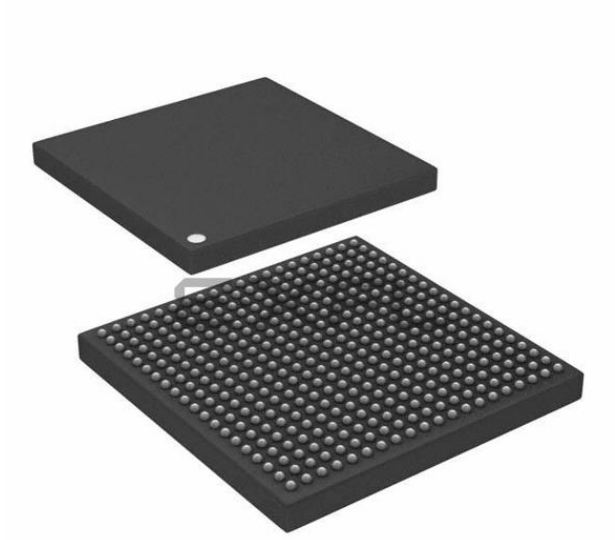

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM1136JF-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 532MHz |
| Co-Processors/DSP | Multimedia; GPU, IPU, VFP |
| RAM Controllers | LPDDR, DDR2 |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keypad, KPP, LCD |
| Ethernet | 10/100Mbps (1) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | Secure Fusebox, Secure JTAG, Tamper Detection |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-LFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx357cjm5b |

SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

## 1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU) (not available for the MCIMX351)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface (CE-ATA is not available for the MCIMX351)
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 $I^2C$ modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)

- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

## 1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

**Table 1. Ordering Information**

| Description | Part Number | Silicon Revision | Package[1] | Speed | Operating Temperature Range (°C) | Signal Ball Map Locations | Ball Map |
|---|---|---|---|---|---|---|---|
| i.MX353 | MCIMX353CVM5B | 2.0 | 5284 | 532 MHz | –40 to 85 | Table 94 | Table 96 |
| i.MX353 | MCIMX353DVM5B | 2.0 | 5284 | 532 MHz | –20 to 70 | Table 94 | Table 96 |
| i.MX357 | MCIMX357CVM5B | 2.0 | 5284 | 532 MHz | –40 to 85 | Table 94 | Table 96 |
| i.MX357 | MCIMX357DVM5B | 2.0 | 5284 | 532 MHz | –20 to 70 | Table 94 | Table 96 |
| i.MX353 | MCIMX353CJQ5C | 2.1 | 5284 | 532MHz | -40 to 85 | Table 95 | Table 97 |
| i.MX353 | MCIMX353DJQ5C | 2.1 | 5284 | 532MHz | -20 to 70 | Table 95 | Table 97 |
| i.MX357 | MCIMX357CJQ5C | 2.1 | 5284 | 532MHz | -40 to 85 | Table 95 | Table 97 |
| i.MX357 | MCIMX357DJQ5C | 2.1 | 5284 | 532MHz | -20 to 70 | Table 95 | Table 97 |

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

**Table 2. Functional Differences in the i.MX35 Parts**

| Module | MCIMX351 | MCIMX353 | MCIMX355 | MCIMX356 | MCIMX357 |
|---|---|---|---|---|---|
| I2C (3) | Yes | Yes | Yes | Yes | Yes |
| CSPI (2) | Yes | Yes | Yes | Yes | Yes |
| SSI/I2S (2) | Yes | Yes | Yes | Yes | Yes |
| ESAI | Yes | Yes | Yes | Yes | Yes |
| SPDIF I/O | Yes | Yes | Yes | Yes | Yes |
| USB HS Host | Yes | Yes | Yes | Yes | Yes |
| USB OTG | Yes | Yes | Yes | Yes | Yes |
| FlexCAN (2) | Yes | Yes | Yes | Yes | Yes |
| MLB | Yes | Yes | Yes | Yes | Yes |

**Table 14. I/O Pin DC Electrical Characteristics (continued)**

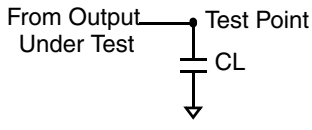
| Pin | DC Electrical Characteristics | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DDR2 | High-level output voltage | Voh | — | NVCC – 0.28 | — | — | V |
| | Low-level output voltage | Vol | — | | — | 0.28 | V |
| | Output min. source current | Ioh | — | –13.4 | — | — | mA |
| | Output min. sink current | Iol | — | 13.4 | — | — | mA |
| | DC input logic high | VIH(dc) | — | NVCC ÷ 2 + 0.125 | — | NVCC + 0.3 | V |
| | DC input logic low | VIL(dc) | — | –0.3 V | — | NVCC ÷ 2 – 0.125 | V |
| | DC input signal voltage (for differential signal) | Vin(dc) | — | –0.3 | — | NVCC + 0.3 | V |
| | DC differential input voltage | Vid(dc) | — | 0.25 | — | NVCC + 0.6 | V |
| | Termination voltage | Vtt | — | NVCC ÷ 2 – 0.04 | NVCC ÷ 2 | NVCC ÷ 2 + 0.04 | V |
| | Input current (no pull-up/down) | IIN | — | — | — | ±1 | μA |
| | Tri-state I/O supply current | Icc – NVCC | — | — | — | ±1 | μA |
| Mobile DDR | High-level output voltage | — | $I_{OH}$ = –1mA<br>$I_{OH}$ = specified drive | NVCC – 0.08<br>0.8 × NVCC | — | — | V |
| | Low-level output voltage | — | $I_{OL}$ = 1mA<br>$I_{OL}$ = specified drive | — | — | 0.08<br>0.2 × NVCC | V |
| | High-level output current (Voh = 0.8 × NVCCV) | — | Standard drive<br>High drive<br>Max. drive | –3.6<br>–7.2<br>–10.8 | — | — | mA |
| | Low-level output current (Vol = 0.2 × NVCCV) | — | Standard Drive<br>High Drive<br>Max. Drive | 3.6<br>7.2<br>10.8 | — | — | mA |
| | High-Level DC CMOS input voltage | VIH | — | 0.7 × NVCC | — | NVCC + 0.3 | V |
| | Low-Level DC CMOS input voltage | VIL | — | –0.3 | — | 0.2 × NVCC | V |
| | Differential receiver VTH+ | VTH+ | — | — | — | 100 | mV |
| | Differential receiver VTH– | VTH– | — | –100 | — | | mV |
| | Input current (no pull-up/down) | IIN | VI = 0<br>VI = NVCC | — | — | ±1 | μA |
| | Tri-state I/O supply current | Icc – NVCC | VI = NVCC or 0 | — | — | ±1 | μA |

**Table 14. I/O Pin DC Electrical Characteristics (continued)**

| Pin | DC Electrical Characteristics | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| SDR (1.8 V) | High-level output voltage | Voh | Ioh = 5.7 mA | OVDD – 0.28 | — | — | V |
| | Low-level output voltage | Vol | Ioh = 5.7 mA | — | — | 0.4 | V |
| | High-level output current | Ioh | Max. drive | 5.7 | — | — | mA |
| | Low-level output current | Iol | Max. drive | 7.3 | — | — | mA |
| | High-level DC Input Voltage | VIH | — | 1.4 | — | 1.98 | V |
| | Low-level DC Input Voltage | VIL | — | –0.3 | — | 0.8 | V |
| | Input current (no pull-up/down) | IIN | VI = 0<br>VI=NVCC | — | — | 150<br>80 | μA |
| | Tri-state I/O supply current | Icc (NVCC) | VI = OVDD or 0 | — | — | 1180 | μA |
| | Tri-state core supply current | Icc (NVCC) | VI = VDD or 0 | — | — | 1220 | μA |
| SDR (3.3 V) | High-level output voltage | Voh | Ioh=specified drive (Ioh = –4, –8, –12, –16 mA) | 2.4 | — | — | V |
| | Low-level output voltage | Vol | Ioh=specified drive (Ioh = 4, 8, 12, 16 mA) | — | — | 0.4 | V |
| | High-level output current | Ioh | Standard drive<br>High drive<br>Max. drive | –4.0<br>–8.0<br>–12.0 | — | — | mA |
| | Low-level output current | Iol | Standard drive<br>High drive<br>Max. drive | 4.0<br>8.0<br>12.0 | — | — | mA |
| | High-level DC Input Voltage | VIH | — | 2.0 | — | 3.6 | V |
| | Low-level DC Input Voltage | VIL | — | –0.3V | — | 0.8 | V |
| | Input current (no pull-up/down) | IIN | VI = 0<br><br>VI = NVCC | — | — | ±1 | μA |
| | Tri-state I/O supply current | Icc (NVCC) | VI = NVCC or 0 | — | — | ±1 | μA |

## 4.8 I/O Pin AC Electrical Characteristics

Figure 5 shows the load circuit for output pins.




CL includes package, probe and jig capacitance

**Figure 5. Load Circuit for Output Pin**

Figure 6 shows the output pin transition time waveform.

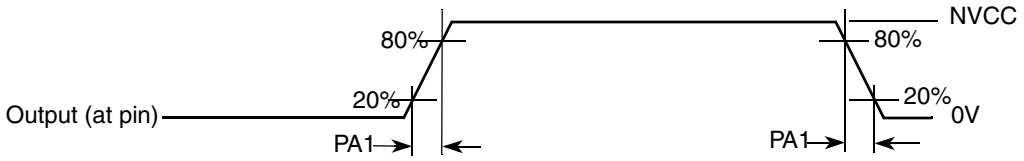



**Figure 6. Output Pin Transition Time Waveform**

### 4.8.1 AC Electrical Test Parameter Definitions

AC electrical characteristics in Table 16 through Table 21 are not applicable for the output open drain pull-down driver.

The dI/dt parameters are measured with the following methodology:

- The zero voltage source is connected between pin and load capacitance.
- The current (through this source) derivative is calculated during output transitions.

**Table 15. AC Requirements of I/O Pins**

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| AC input logic high | VIH(ac) | NVCC ÷ 2 + 0.25 | NVCC + 0.3 | V |
| AC input logic low | VIL(ac) | –0.3 | NVCC ÷ 2 – 0.25 | V |

**Table 16. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 3.0 V–3.6 V]**

| Parameter | Symbol | Test Condition | Min. Rise/Fall | Typ. Rise/Fall | Max. Rise/Fall | Units |
|---|---|---|---|---|---|---|
| Duty cycle | Fduty | — | 40 | — | 60 | % |
| Output pin slew rate (max. drive) | tps | 25 pF<br>50 pF | 0.79/1.12<br>0.49/0.73 | 1.30/1.77<br>0.84/1.23 | 2.02/2.58<br>1.19/1.58 | V/ns |
| Output pin slew rate (high drive) | tps | 25 pF<br>50 pF | 0.48/0.72<br>0.27/0.42 | 0.76/1.10<br>0.41/0.62 | 1.17/1.56<br>0.63/0.86 | V/ns |
| Output pin slew rate (standard drive) | tps | 25 pF<br>50 pF | 0.25/0.40<br>0.14/0.21 | 0.40/0.59<br>0.21/0.32 | 0.60/0.83<br>0.32/0.44 | V/ns |
| Output pin di/dt (max. drive) | tdit | 25 pF<br>50 pF | 15<br>16 | 36<br>38 | 76<br>80 | mA/ns |
| Output pin di/dt (high drive) | tdit | 25 pF<br>50 pF | 8<br>9 | 20<br>21 | 45<br>47 | mA/ns |
| Output pin di/dt (standard drive) | tdit | 25 pF<br>50 pF | 4<br>4 | 10<br>10 | 22<br>23 | mA/ns |

### 4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

Figure 9 depicts the TRACECLK timings of ETM, and Table 30 lists the timing parameters.

**Figure 9. ETM TRACECLK Timing Diagram**

**Table 30. ETM TRACECLK Timing Parameters**

| ID | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | — | ns |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 31 lists the timing parameters.

**Figure 10. Trace Data Timing Diagram**

**Table 31. ETM Trace Data Timing Parameters**

| ID | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_s$ | Data setup | 2 | — | ns |
| $T_h$ | Data hold | 1 | — | ns |

#### 4.9.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same $T_s$ and $T_h$ parameters from Table 31 still apply with respect to the falling edge of the TRACECLK signal.

Recommended drive strength for all controls, address and BCLK is set to maximum drive.

Figure 16 through Figure 21 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 33 for specific control parameter settings.

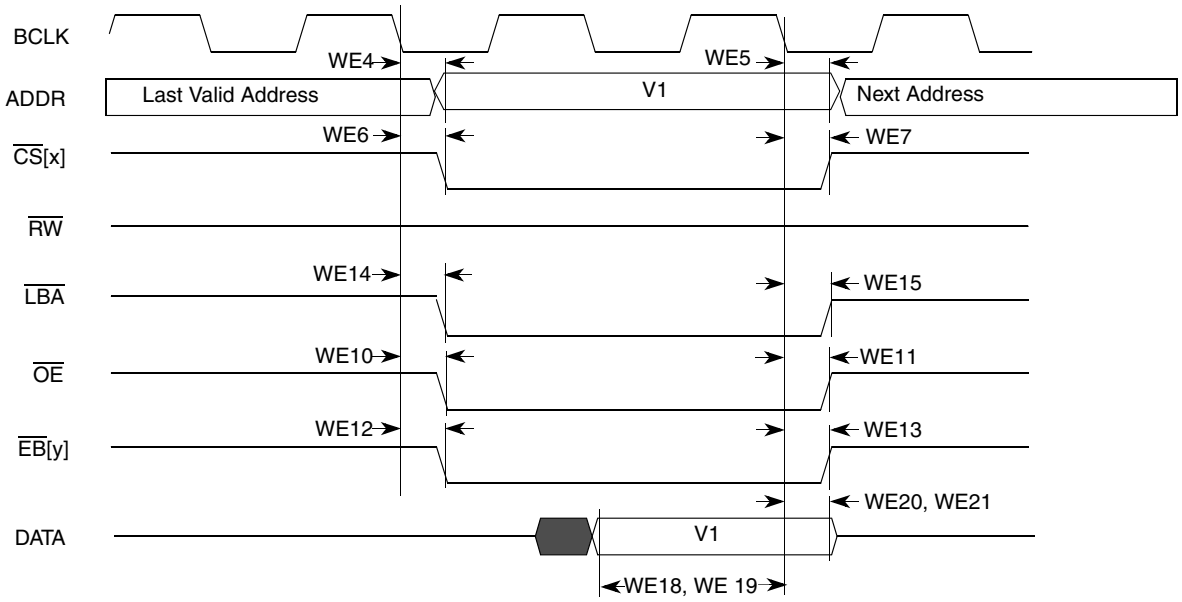



**Figure 16. Synchronous Memory Timing Diagram for Read Access—WSC = 1**

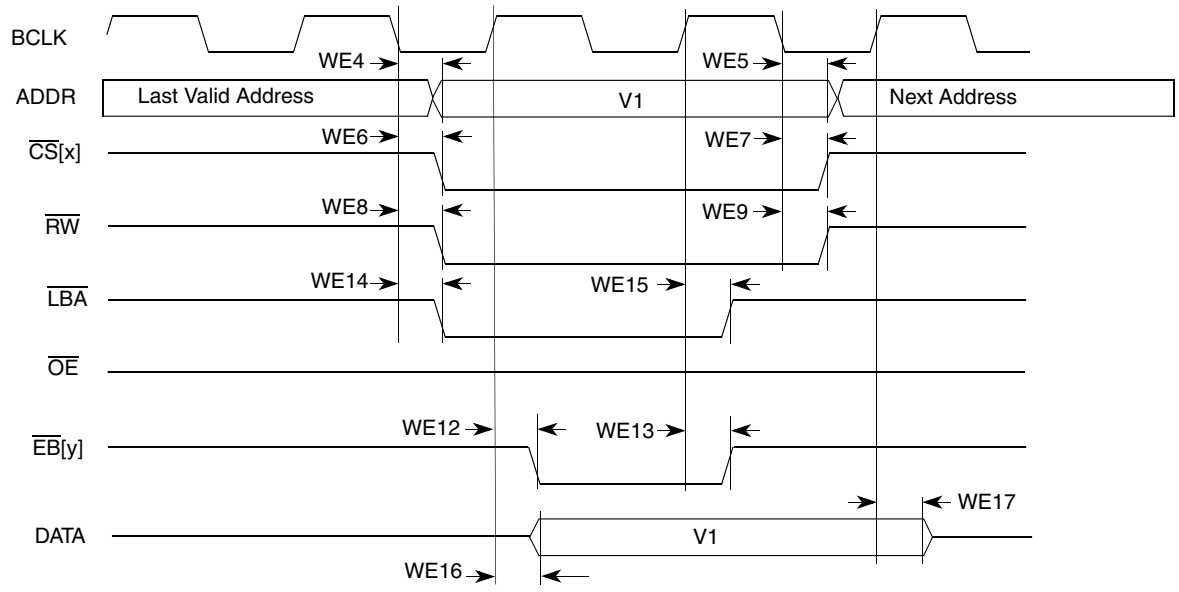



**Figure 17. Synchronous Memory Timing Diagram for Write Access—WSC = 1, EBWA = 1, EBWN = 1, LBN = 1**

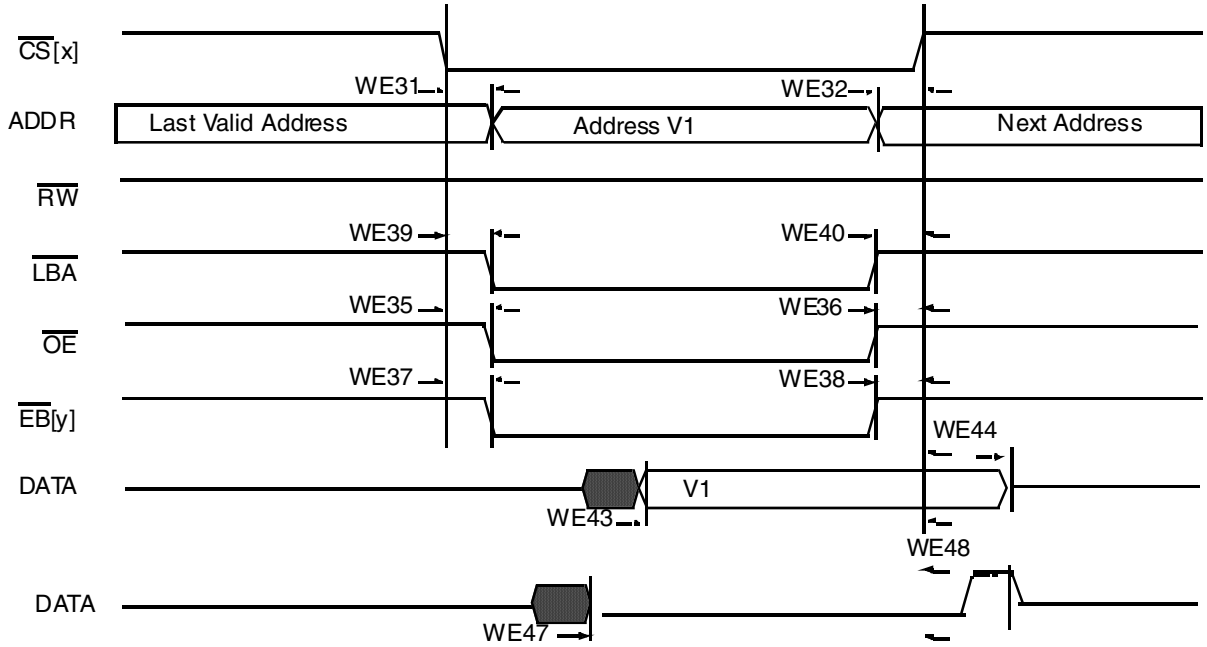



**Figure 26. DTACK Read Access**

**Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table**

| Ref No. | Parameter | Determination By Synchronous Measured Parameters[1] | Min | Max (If 133 MHz is supported by SoC) | Unit |
|---|---|---|---|---|---|
| WE31 | $\overline{CS}$[x] valid to Address valid | WE4 – WE6 – CSA[2] | — | 3 – CSA | ns |
| WE32 | Address invalid to $\overline{CS}$[x] invalid | WE7 – WE5 – CSN[3] | — | 3 – CSN | ns |
| WE32A( muxed A/D | $\overline{CS}$[x] valid to address invalid | WE4 – WE7 + (LBN + LBA + 1 – CSA[2]) | –3 + (LBN + LBA + 1 – CSA) | — | ns |
| WE33 | $\overline{CS}$[x] valid to $\overline{WE}$ valid | WE8 – WE6 + (WEA – CSA) | — | 3 + (WEA – CSA) | ns |
| WE34 | $\overline{WE}$ invalid to $\overline{CS}$[x] invalid | WE7 – WE9 + (WEN – CSN) | — | 3 – (WEN_CSN) | ns |
| WE35 | $\overline{CS}$[x] valid to $\overline{OE}$ valid | WE10 – WE6 + (OEA – CSA) | — | 3 + (OEA – CSA) | ns |
| WE35A (muxed A/D) | $\overline{CS}$[x] valid to $\overline{OE}$ valid | WE10 – WE6 + (OEA + RLBN + RLBA + ADH + 1 – CSA) | –3 + (OEA + RLBN + RLBA + ADH + 1 – CSA) | 3 + (OEA + RLBN + RLBA + ADH + 1 – CSA) | ns |
| WE36 | $\overline{OE}$ invalid to $\overline{CS}$[x] invalid | WE7 – WE11 + (OEN – CSN) | — | 3 – (OEN – CSN) | ns |
| WE37 | $\overline{CS}$[x] valid to $\overline{BE}$[y] valid (read access) | WE12 – WE6 + (RBEA – CSA) | — | 3 + (RBEA[4] – CSA) | ns |
| WE38 | $\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (read access) | WE7 – WE13 + (RBEN – CSN) | — | 3 – (RBEN[5] – CSN) | ns |
| WE39 | $\overline{CS}$[x] valid to $\overline{LBA}$ valid | WE14 – WE6 + (LBA – CSA) | — | 3 + (LBA – CSA) | ns |
| WE40 | $\overline{LBA}$ invalid to $\overline{CS}$[x] invalid | WE7 – WE15 – CSN | — | 3 – CSN | ns |

**Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)**

| ID | Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD8 | SDRAM access time | tAC | — | 6.47 | ns |
| SD9 | Data out hold time[1] | tOH | 1.2 | — | ns |
| SD10 | Active to read/write command period | tRC | 10 | — | clock |

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 44 and Table 45.

**NOTE**

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

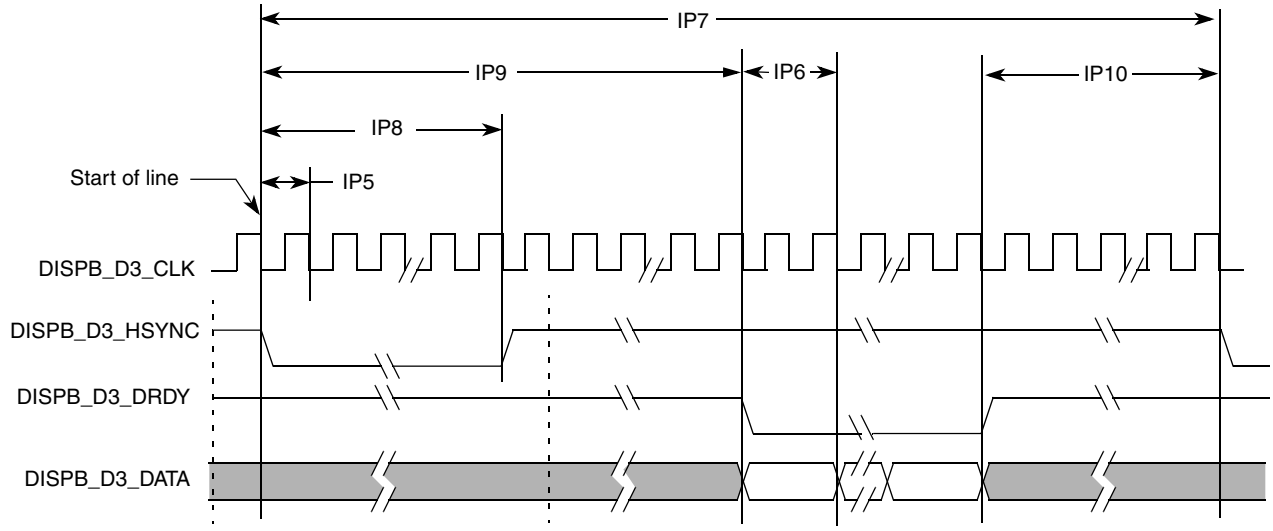



**Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse**

Figure 49 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

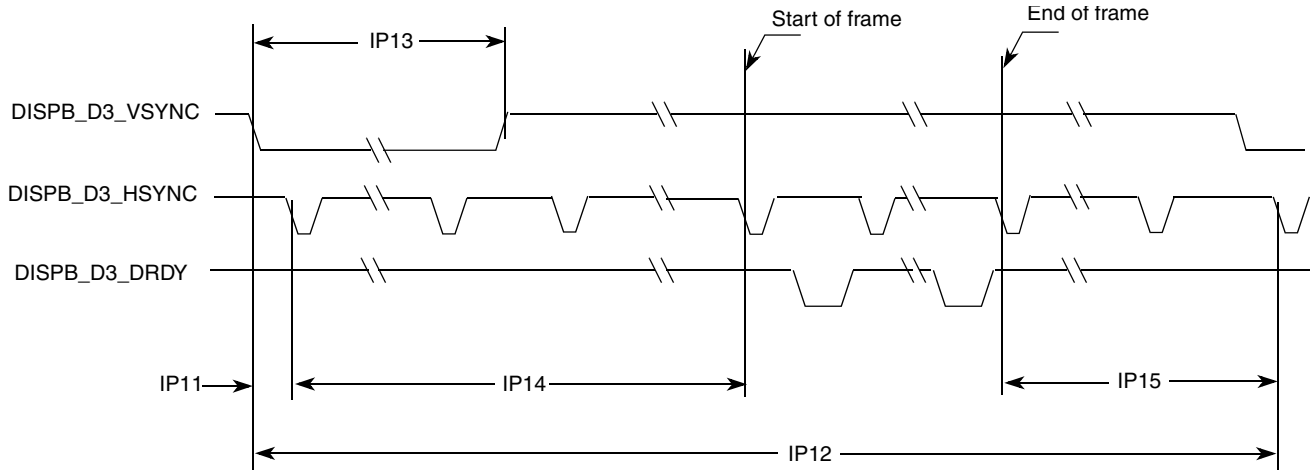



**Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse**

Table 55 shows timing parameters of signals presented in Figure 48 and Figure 49.

**Table 55. Synchronous Display Interface Timing Parameters—Pixel Level**

| ID | Parameter | Symbol | Value | Units |
|---|---|---|---|---|
| IP5 | Display interface clock period | Tdicp | Tdicp[1] | ns |
| IP6 | Display pixel clock period | Tdpcp | (DISP3_IF_CLK_CNT_D + 1) × Tdicp | ns |
| IP7 | Screen width | Tsw | (SCREEN_WIDTH + 1) × Tdpcp | ns |
| IP8 | HSYNC width | Thsw | (H_SYNC_WIDTH + 1) × Tdpcp | ns |

**Table 56. Synchronous Display Interface Timing Parameters—Access Level**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP16 | Display interface clock low time | Tckl | Tdicd – Tdicu – 1.5 | Tdicd[2] – Tdicu[3] | Tdicd – Tdicu + 1.5 | ns |
| IP17 | Display interface clock high time | Tckh | Tdicp – Tdicd + Tdicu – 1.5 | Tdicp – Tdicd + Tdicu | Tdicp – Tdicd + Tdicu + 1.5 | ns |
| IP18 | Data setup time | Tdsu | Tdicd – 3.5 | Tdicu | — | ns |
| IP19 | Data holdup time | Tdhd | Tdicp – Tdicd – 3.5 | Tdicp – Tdicu | — | ns |
| IP20 | Control signals setup time to display interface clock | Tcsu | Tdicd – 3.5 | Tdicu | — | ns |

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

### 4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

### 4.9.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

#### 4.9.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 52 depicts the interface timing.

- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - — At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - — At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

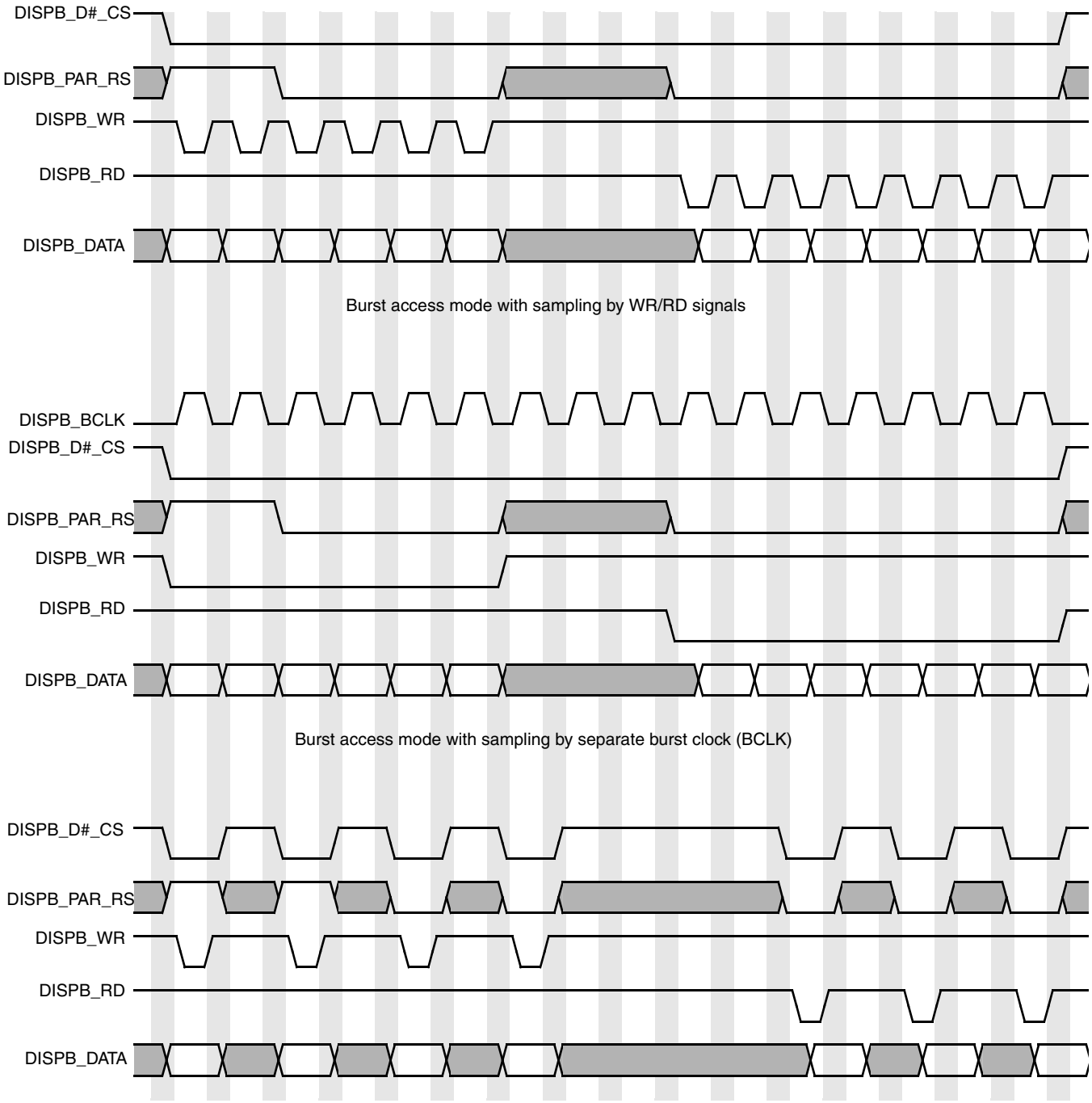



**Figure 54. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram**

**Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP55 | Controls hold time for read | Tdchr | Tdicpr – Tdicdr – 1.5 | Tdicpr – Tdicdr | — | ns |
| IP56 | Controls setup time for write | Tdcsw | Tdicuw – 1.5 | Tdicuw | — | ns |
| IP57 | Controls hold time for write | Tdchw | Tdicpw – Tdicdw – 1.5 | Tdicpw – Tdicdw | — | ns |
| IP58 | Slave device data delay[8] | Tracc | 0 | — | Tdrp[9] – Tlbd[10] – Tdicur – 1.5 | ns |
| IP59 | Slave device data hold time[8] | Troh | Tdrp – Tlbd – Tdicdr + 1.5 | — | Tdicpr – Tdicdr – 1.5 | ns |
| IP60 | Write data setup time | Tds | Tdicdw – 1.5 | Tdicdw | — | ns |
| IP61 | Write data hold time | Tdh | Tdicpw – Tdicdw – 1.5 | Tdicpw – Tdicdw | — | ns |
| IP62 | Read period[2] | Tdicpr | Tdicpr – 1.5 | Tdicpr | Tdicpr + 1.5 | ns |
| IP63 | Write period[3] | Tdicpw | Tdicpw – 1.5 | Tdicpw | Tdicpw + 1.5 | ns |
| IP64 | Read down time[4] | Tdicdr | Tdicdr – 1.5 | Tdicdr | Tdicdr + 1.5 | ns |
| IP65 | Read up time[5] | Tdicur | Tdicur – 1.5 | Tdicur | Tdicur + 1.5 | ns |
| IP66 | Write down time[6] | Tdicdw | Tdicdw – 1.5 | Tdicdw | Tdicdw + 1.5 | ns |
| IP67 | Write up time[7] | Tdicuw | Tdicuw – 1.5 | Tdicuw | Tdicuw + 1.5 | ns |
| IP68 | Read time point[9] | Tdrp | Tdrp – 1.5 | Tdrp | Tdrp + 1.5 | ns |

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

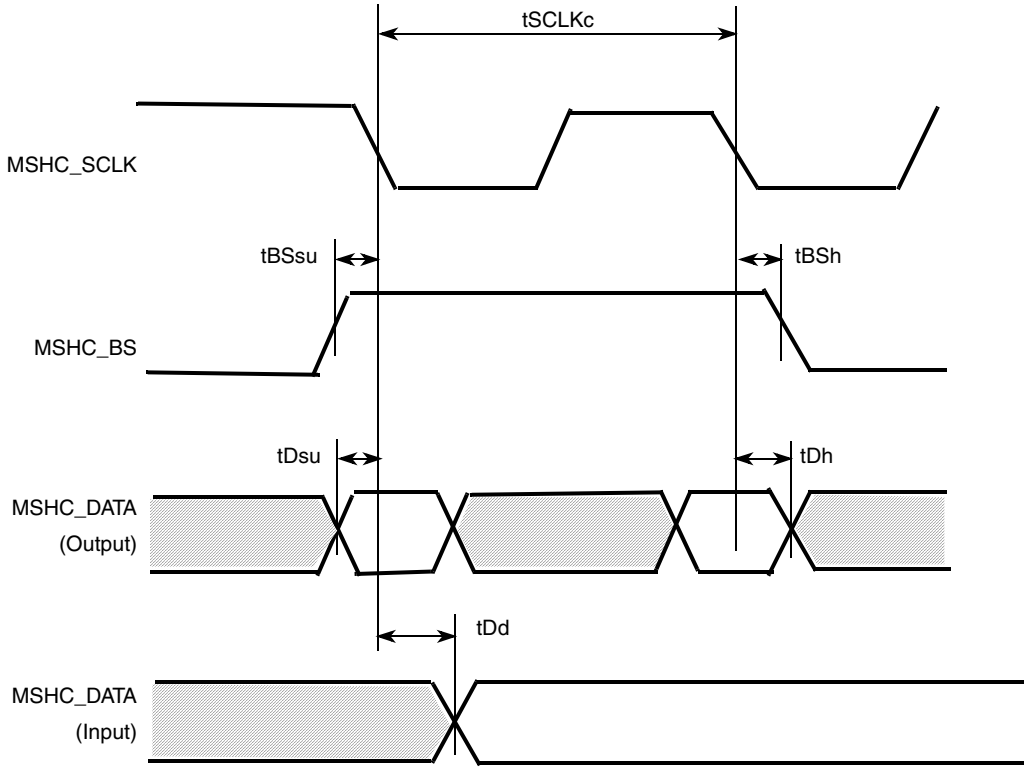



**Figure 69. Transfer Operation Timing Diagram (Parallel)**

## NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

**Table 60. Serial Interface Timing Parameters[1]**

| Signal | Parameter | Symbol | Standards | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| MSHC_SCLK | Cycle | tSCLKc | 50 | — | ns |
| | H pulse length | tSCLKwh | 15 | — | ns |
| | L pulse length | tSCLKwl | 15 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 5 | — | ns |
| | Hold time | tBSh | 5 | — | ns |

**Table 62. MLB 256/512 Fs Timing Parameters (continued)**

| Parameter | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| MLB fall time | $t_{mckf}$ | — | — | 3 | ns | $V_{IH}$ TO $V_{IL}$ |
| MLBCLK cycle time | $t_{mckc}$ | —<br>— | 81<br>40 | —<br>— | ns | 256 × Fs<br>512 × Fs |
| MLBCLK low time | $t_{mckl}$ | 31.5<br>30 | 37<br>35.5 | —<br>— | ns | 256 × Fs<br>256 × Fs PLL unlocked |
| | | 14.5<br>14 | 17<br>16.5 | —<br>— | ns | 512 × Fs<br>512 × Fs PLL unlocked |
| MLBCLK high time | $t_{mckh}$ | 31.5<br>30 | 38<br>36.5 | —<br>— | ns | 256 × Fs<br>256 × Fs PLL unlocked |
| | | 14.5<br>14 | 17<br>16.5 | —<br>— | ns | 512 × Fs<br>512 × Fs PLL unlocked |
| MLBCLK pulse width variation | $t_{mpwv}$ | — | — | 2 | ns pp | Note[2] |
| MLBSIG/MLBDAT input valid to MLBCLK falling | $t_{dsmcf}$ | 1 | — | — | ns | — |
| MLBSIG/MLBDAT input hold from MLBCLK low | $t_{dhmcf}$ | 0 | — | — | ns | — |
| MLBSIG/MLBDAT output high impedance from MLBCLK low | $t_{mcfdz}$ | 0 | — | $t_{mckl}$ | ns | — |
| Bus Hold Time | $t_{mdzh}$ | 4 | — | — | ns | Note[3] |

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

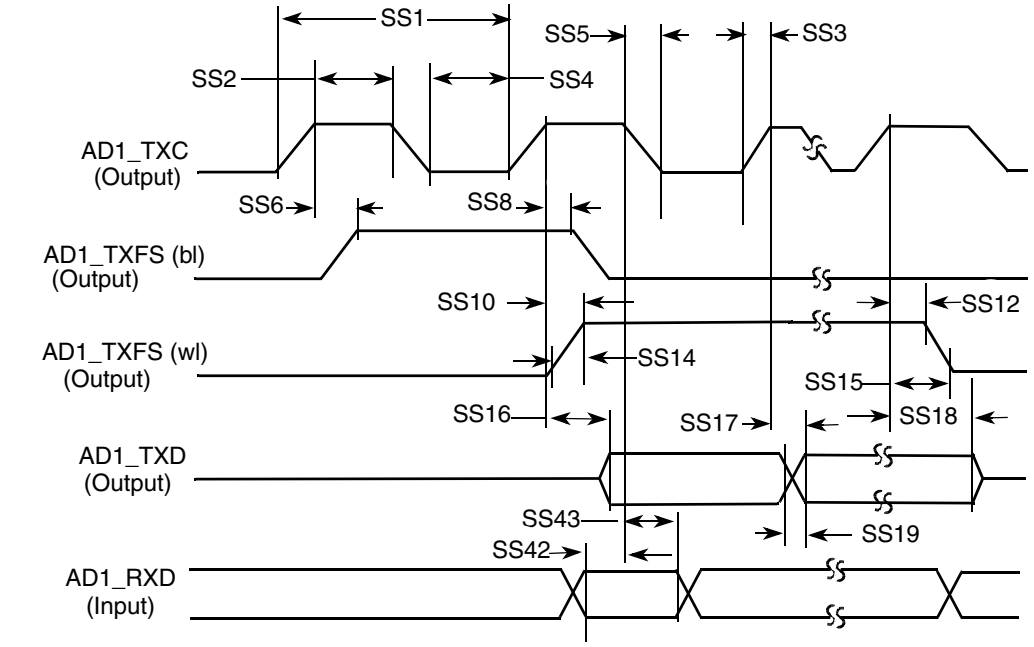
Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below unless otherwise noted.

**Table 63. MLB Device 1024Fs Timing Parameters**

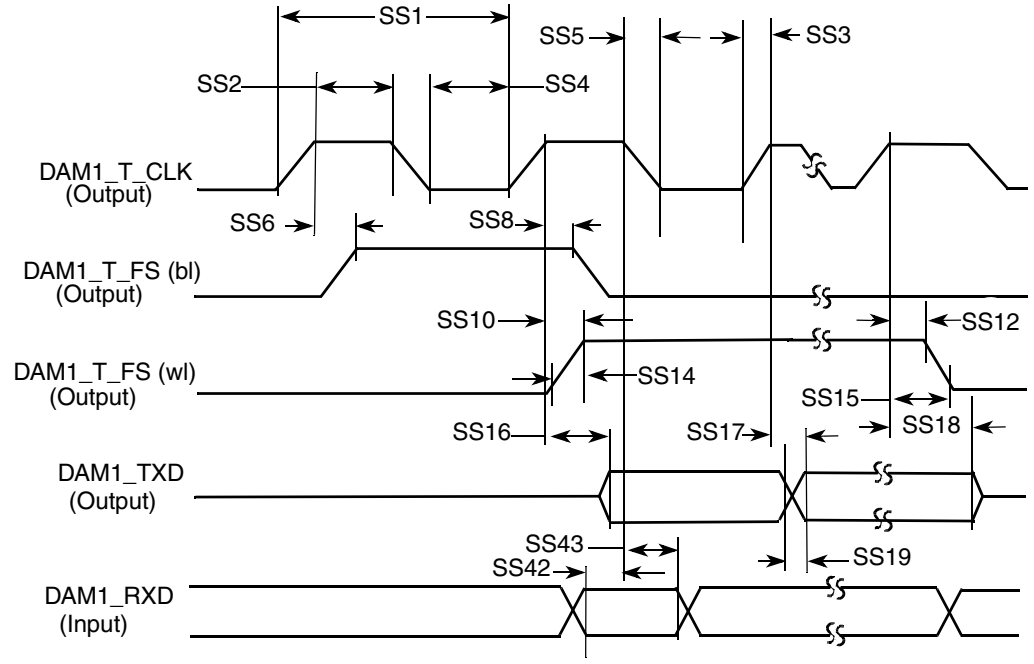
| Parameter | Symbol | Min | Typ | Max | Units | Comment |
|---|---|---|---|---|---|---|
| MLBCLK Operating Frequency[1] | $f_{mck}$ | 45.056 | 49.152 | 49.2544<br>51.200 | MHz | Min: 1024 × Fs at 44.0 kHz<br>Typ: 1024 × Fs at 48.0 kHz<br>Max: 1024 × Fs at 48.1 kHz<br>Max: 1024 × Fs PLL unlocked |
| MLBCLK rise time | $t_{mckr}$ | — | — | 1 | ns | $V_{IL}$ TO $V_{IH}$ |
| MLB fall time | $t_{mckf}$ | — | — | 1 | ns | $V_{IH}$ TO $V_{IL}$ |
| MLBCLK cycle time | $t_{mckc}$ | — | 20.3 | — | ns | — |
| MLBCLK low time | $t_{mckl}$ | 6.5<br>6.1 | 7.7<br>7.3 | — | ns | PLL unlocked |

### 4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter timing with internal clock, and Table 78 lists the timing parameters.




Note: SRXD Input in Synchronous mode only




Note: SRXD Input in Synchronous mode only

**Figure 92. SSI Transmitter with Internal Clock Timing Diagram**

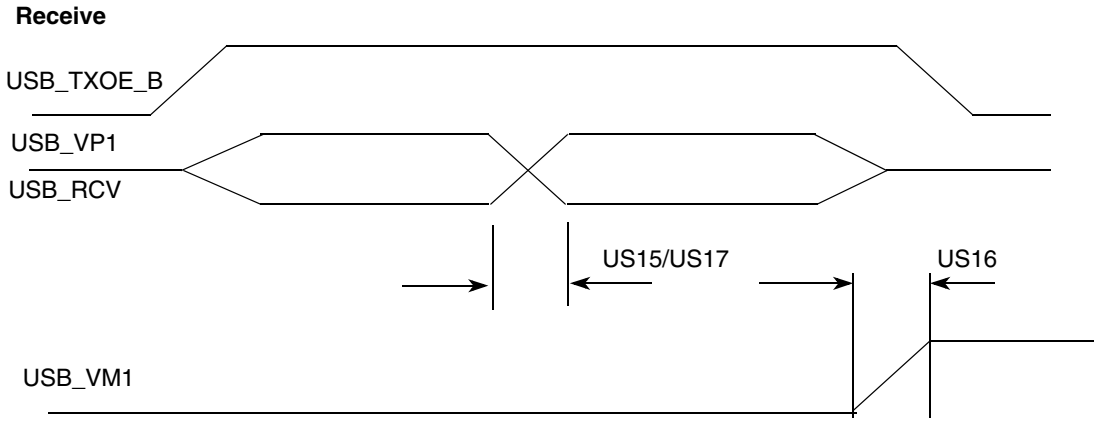



**Figure 103. USB Receive Waveform in DAT_SE0 Unidirectional Mode**

Table 89 describes the port timing specification in DAT_SE0 unidirectional mode.

**Table 89. USB Port Timing Specification in DAT_SE0 Unidirectional Mode**

| No. | Parameter | Signal Name | Signal Source | Min. | Max. | Unit | Condition/ Reference Signal |
|---|---|---|---|---|---|---|---|
| US9 | Tx rise/fall time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| US10 | Tx rise/fall time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| US11 | Tx rise/fall time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| US12 | Tx duty cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| US15 | Rx rise/fall time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| US16 | Rx rise/fall time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| US17 | Rx rise/fall time | USB_RCV | In | — | 3.0 | ns | 35 pF |

### 4.9.24.3 VP_VM Bidirectional Mode

Table 90 defines the signals for VP_VM bidirectional mode. Figure 104 and Figure 105 show the transmit and receive waveforms respectively.

**Table 90. Signal Definitions—VP_VM Bidirectional Mode**

| Name | Direction | Signal Description |
|---|---|---|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out (Tx)<br>In (Rx) | Tx VP data when USB_TXOE_B is low<br>Rx VP data when USB_TXOE_B is high |
| USB_SE0_VM | Out (Tx)<br>In (Rx) | Tx VM data when USB_TXOE_B low<br>Rx VM data when USB_TXOE_B high |
| USB_RCV | In | Differential Rx data |

# 5 Package Information and Pinout

This section includes the following:

- Mechanical package drawing
- Pin/contact assignment information

# 7 Revision History

Table 98 shows the revision history of this document. Note: There were no revisions of this document between revision 1 and revision 4 or between revision 6 and revision 7.

**Table 98. i.MX35 Data Sheet Revision History**

| Revision Number | Date | Substantive Change(s) |
|---|---|---|
| 10 | 06/2012 | • In Table 2, "Functional Differences in the i.MX35 Parts," on page 3, added two columns for part numbers MCIMX353 and MCIMX357.<br>• Added Table 29, "Clock Input Tolerance," on page 31 in Section 4.9.3, “DPLL Electrical Specifications.”<br>• Updated Table 39, "DDR2 SDRAM Timing Parameter Table," on page 50 for DDR2-400 values.<br>• Updated Table 41, "DDR2 SDRAM Write Cycle Parameters," on page 52 for DDR2-400 values.<br>• Added Table 15, "AC Requirements of I/O Pins," on page 24.<br>• Updated WE4 parameter in Table 33, "WEIM Bus Timing Parameters," on page 37. |
| 9 | 08/2010 | • Updated Table 32, “NFC Timing Parameters.”<br>• Updated Table 33, “WEIM Bus Timing Parameters.” |
| 8 | 04/2010 | • Updated Table 14, “I/O Pin DC Electrical Characteristics.” |
| 7 | 12/18/2009 | • Updated Table 1, “Ordering Information.” |
| 6 | 10/21/2009 | • Added information for silicon rev. 2.1<br>• Updated Table 1, “Ordering Information.”<br>• Added Table 95, “Silicon Revision 2.1 Signal Ball Map Locations.”<br>• Added Table 97, “Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch.” |
| 5 | 08/06/2009 | • Added a line for $T_A$ = –40 to 85 $^oC$ in Table 14, “I/O Pin DC Electrical Characteristics”<br>• Filled in TBDs in Table 14.<br>• Revised Figure 15 and Table 33 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table.<br>• Added Table 26, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V).” |
| 4 | 04/30/2009 | Note: There were no revisions of this document between revision 1 and revision 4.<br>• In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6.<br>• Updated values in Table 10, “i.MX35 Power Modes.”<br>• Added Section 4.4, “Reset Timing.”<br>• In Section 4.8.2, “AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes),” removed Slow Slew rate tables, relabeled Table 24, “AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode,” and Table 25, “AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode,” to exclude mention of slew rate.<br>• In Section 4.9.5.2, “Wireless External Interface Module (WEIM),” modified Figure 16, “Synchronous Memory Timing Diagram for Read Access—WSC = 1,” through Figure 21, “Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7.”<br>• In Section 4.9.6, “Enhanced Serial Audio Interface (ESAI) Timing Specifications,” modified Figure 36, “ESAI Transmitter Timing,” and Figure 37, “ESAI Receiver Timing,” to remove extraneous signals. Removed a note from Figure 36, “ESAI Transmitter Timing.” |
| 3 | 03/2009 | • In Section 4.3.1, “Powering Up,” reverse positions of steps 5 and 6. |
| 2 | 02/2009 | • Added the following parts to Table 1, “Ordering Information”: PCIMX357CVM5B, MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B. Throughout consumer data sheet: Removed or updated information related to Media Local Bus interface.Updated Section 4.3.1, “Powering Up.”<br>• Updated values in Table 10, “i.MX35 Power Modes.” |