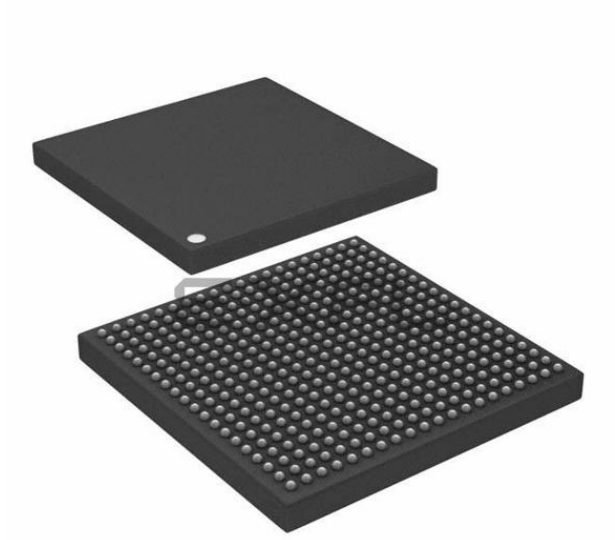

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx357cjq5cr2

Table 2. Functional Differences in the i.MX35 Parts (continued)

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
Ethernet	Yes	Yes	Yes	Yes	Yes
1-Wire	Yes	Yes	Yes	Yes	Yes
KPP	Yes	Yes	Yes	Yes	Yes
SDIO/MMC (2)	Yes	Yes	Yes	Yes	Yes
SDIO/Memory Stick	Yes	Yes	Yes	Yes	Yes
External Memory Controller (EMC)	Yes	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
PATA	—	Yes	Yes	Yes	Yes
CE-ATA	—	Yes	Yes	Yes	Yes
Image Processing Unit (IPU) (inversion and rotation, pre- and post-processing, camera interface, blending, display controller)	—	Yes	Yes	Yes	Yes
Open VG graphics acceleration (GPU)	—	Yes	—	Yes	Yes

1.3 Block Diagram

Figure 1 is the i.MX35 simplified interface block diagram.

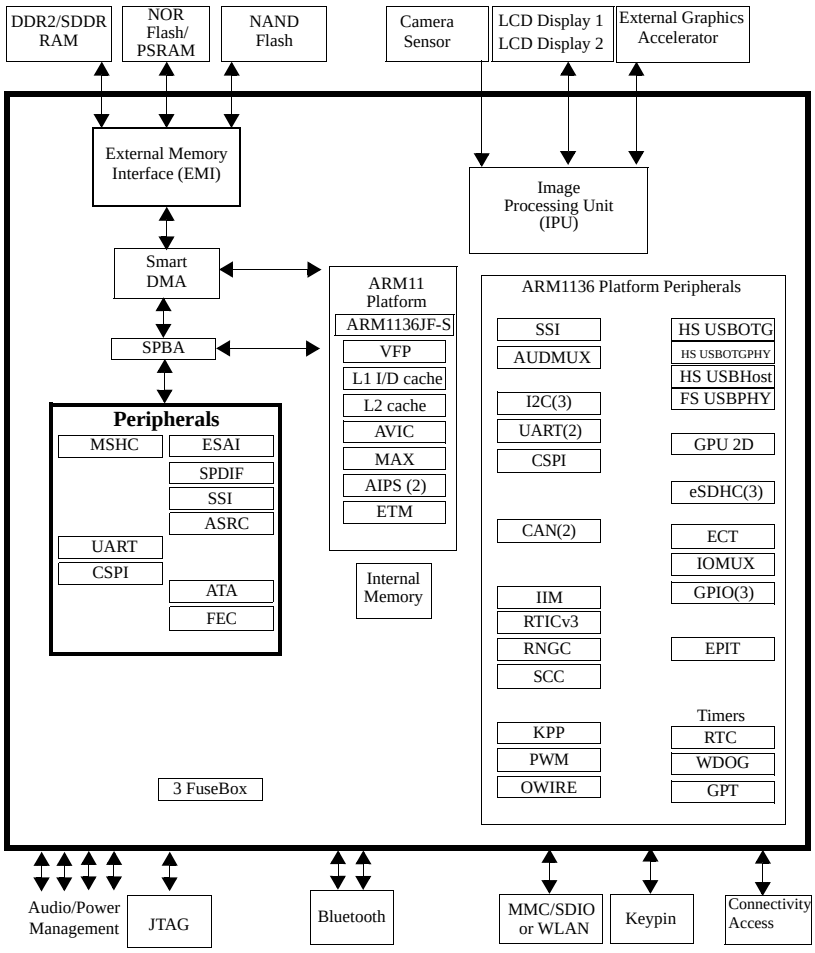

Figure 1. i.MX35 Simplified Interface Block Diagram

2 Functional Description and Application Information

The i.MX35 consists of the following major subsystems:

- ARM1136 Platform—AP domain
- SDMA Platform and EMI—Shared domain

2.1 Application Processor Domain Overview

The applications processor (AP) and its domain are responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The AP domain is built around an ARM1136JF-S core with 16-Kbyte instruction and data L1 caches, an MMU, a 128-Kbyte L2 cache, a multiported crossbar switch, and advanced debug and trace interfaces.

The i.MX35 core is intended to operate at a maximum frequency of 532 MHz to support the required multimedia use cases. Furthermore, an image processing unit (IPU) is integrated into the AP domain to offload the ARM11 core from performing functions such as color space conversion, image rotation and scaling, graphics overlay, and pre- and post-processing.

The functionality of AP Domain peripherals includes the user interface; the connectivity, display, security, and memory interfaces; and 128 Kbytes of multipurpose SRAM.

2.2 Shared Domain Overview

The shared domain is composed of the shared peripherals, a smart DMA engine (SDMA) and a number of miscellaneous modules. For maximum flexibility, some peripherals are directly accessible by the SDMA engine.

The i.MX35 has a hierarchical memory architecture including L1 caches and a unified L2 cache. This reduces the bandwidth demands for the external bus and external memory. The external memory subsystem supports a flexible external memory system, including support for SDRAM (SDR, DDR2 and mobile DDR) and NAND Flash.

2.3 Advanced Power Management Overview

To address the continuing need to reduce power consumption, the following techniques are incorporated in the i.MX35:

- Clock gating
- Power gating
- Power-optimized synthesis
- Well biasing

The insertion of gating into the clock paths allows unused portions of the chip to be disabled. Because static CMOS logic consumes only leakage power, significant power savings can be realized.

"Well biasing" is applying a voltage that is greater than V_{DD} to the nwells, and one that is lower than V_{SS} to the pwells. The effect of applying this well back bias voltage reduces the subthreshold channel leakage. For the 90-nm digital process, it is estimated that the subthreshold leakage is reduced by a factor of ten over the nominal leakage. Additionally, the supply voltage for internal logic can be reduced from 1.4 V to 1.22 V.

2.4 ARM11 Microprocessor Core

The CPU of the i.MX35 is the ARM1136JF-S core, based on the ARM v6 architecture. This core supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes) and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features are as follows:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
I^2C(3)	I^2C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DDR2	High-level output voltage	Voh	—	NVCC – 0.28	—	—	V
	Low-level output voltage	Vol	—		—	0.28	V
	Output min. source current	Ioh	—	–13.4	—	—	mA
	Output min. sink current	Iol	—	13.4	—	—	mA
	DC input logic high	VIH(dc)	—	NVCC ÷ 2 + 0.125	—	NVCC + 0.3	V
	DC input logic low	VIL(dc)	—	–0.3 V	—	NVCC ÷ 2 – 0.125	V
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	NVCC + 0.3	V
	DC differential input voltage	Vid(dc)	—	0.25	—	NVCC + 0.6	V
	Termination voltage	Vtt	—	NVCC ÷ 2 – 0.04	NVCC ÷ 2	NVCC ÷ 2 + 0.04	V
	Input current (no pull-up/down)	IIN	—	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	—	—	—	±1	μA
Mobile DDR	High-level output voltage	—	I_{OH} = –1mA I_{OH} = specified drive	NVCC – 0.08 0.8 × NVCC	—	—	V
	Low-level output voltage	—	I_{OL} = 1mA I_{OL} = specified drive	—	—	0.08 0.2 × NVCC	V
	High-level output current (Voh = 0.8 × NVCCV)	—	Standard drive High drive Max. drive	–3.6 –7.2 –10.8	—	—	mA
	Low-level output current (Vol = 0.2 × NVCCV)	—	Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA
	High-Level DC CMOS input voltage	VIH	—	0.7 × NVCC	—	NVCC + 0.3	V
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	0.2 × NVCC	V
	Differential receiver VTH+	VTH+	—	—	—	100	mV
	Differential receiver VTH–	VTH–	—	–100	—		mV
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	VI = NVCC or 0	—	—	±1	μA

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

Table 26. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Clock frequency	f	—	125	—	—	MHz
Output pin slew rate (max. drive)[1]	tps	25 pF 50 pF	2.83/2.68 1.59/1.49	1.84/1.85 1.03/1.05	1.21/1.40 0.70/0.75	V/ns
Output pin di/dt (max. drive)[2]	didt	25 pF 50 pF	89 95	202 213	435 456	mA/ns
Input pin transition times[3]	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pin propagation delay, 50%–50%	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pin propagation delay, 40%–60%	tpi	1.0 pF	1.18/1.99	1.45/2.35	1.97/2.85	ns

1 Min. condition for tps: wcs model, 1.1 V, IO 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Max. condition for tdit: bcs model, 1.3 V, IO 1.95 V, and –40 °C.

3 Max. condition for tpi and trfi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Min. condition for tpi and trfi: bcs model, 1.3 V, IO 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

4.9 Module-Level AC Electrical Specifications

This section contains the AC electrical information (including timing specifications) for the modules of the i.MX35. The modules are listed in alphabetical order.

4.9.1 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. See the electrical specification for SSI.

4.9.2 CSPI AC Electrical Specifications

The i.MX35 provides two CSPI modules. CSPI ports are multiplexed in the i.MX35 with other pins. See the “External Signals and Multiplexing” chapter of the reference manual for more details.

Table 37. SDRAM Refresh Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 37 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

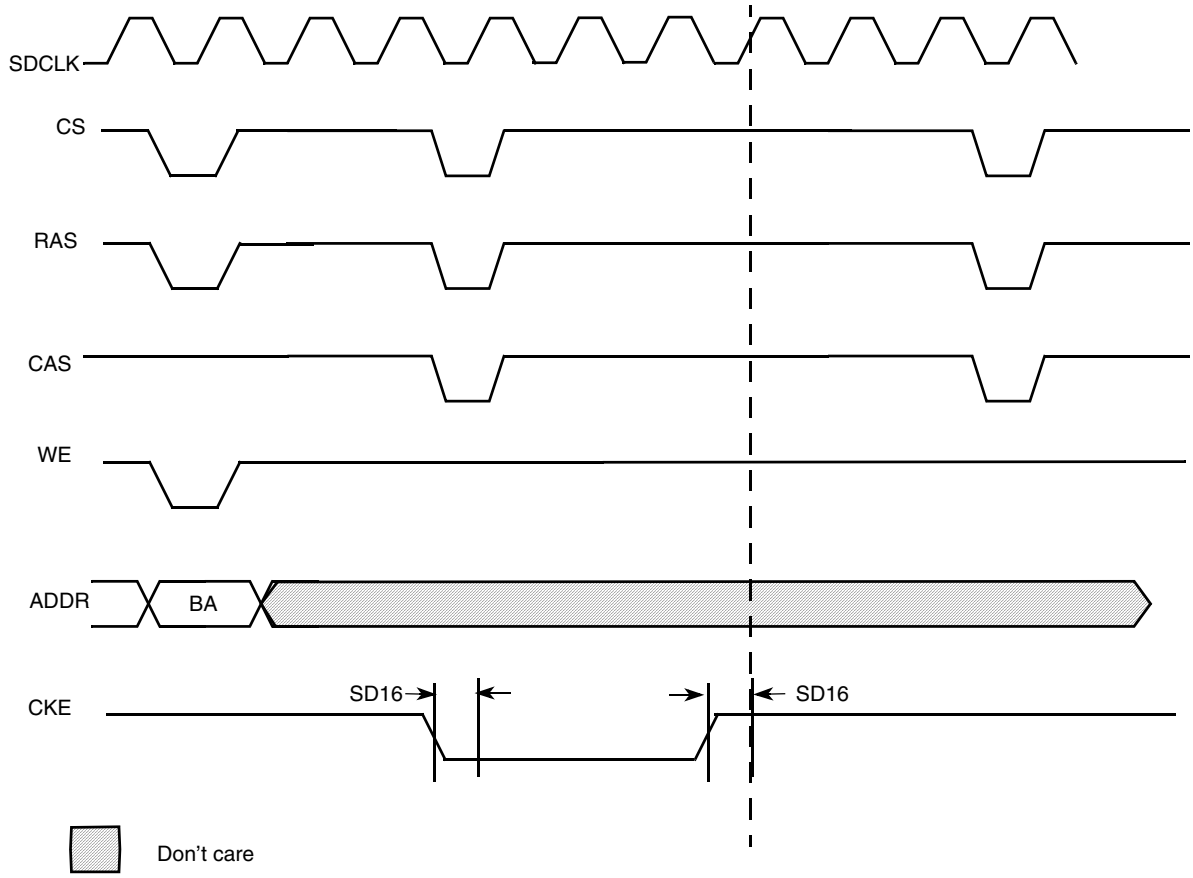

Figure 30. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 38. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

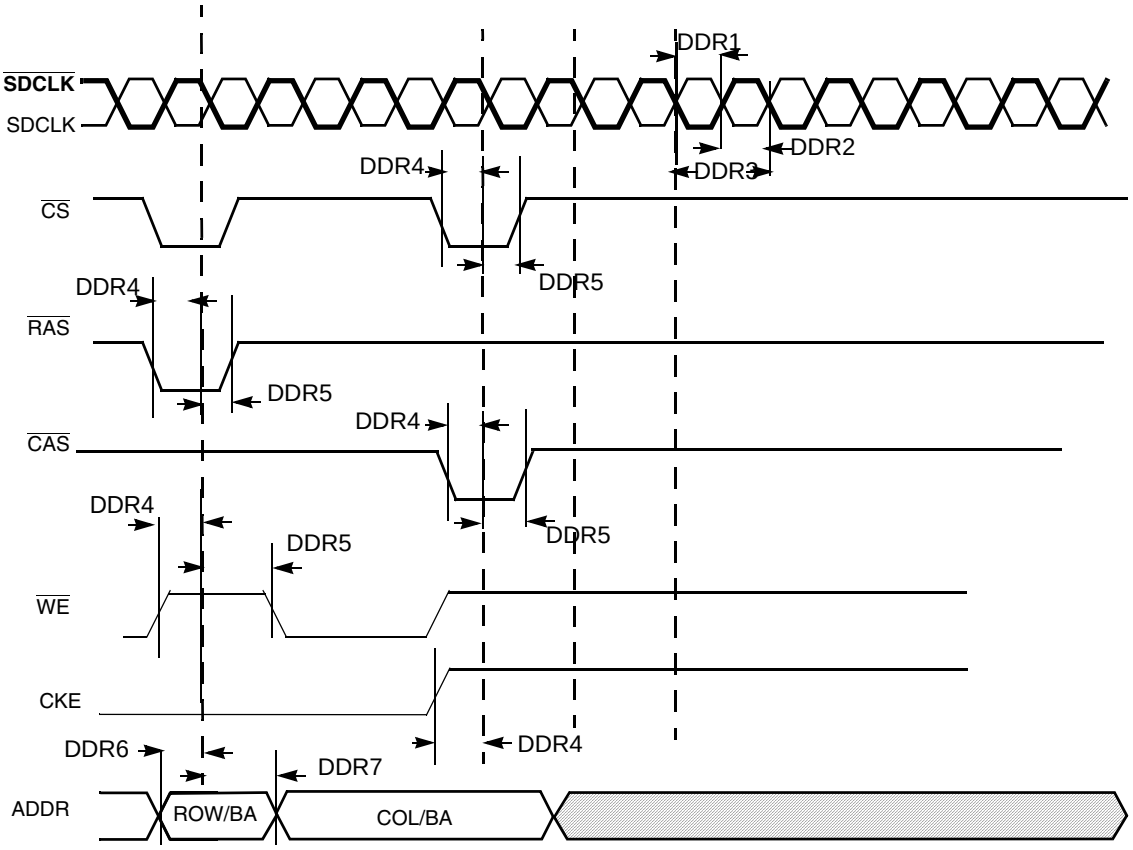

Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	7.0	8.0	ns
DDR4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	1.5	—	ns

Table 56. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd[2] – Tdicu[3]	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

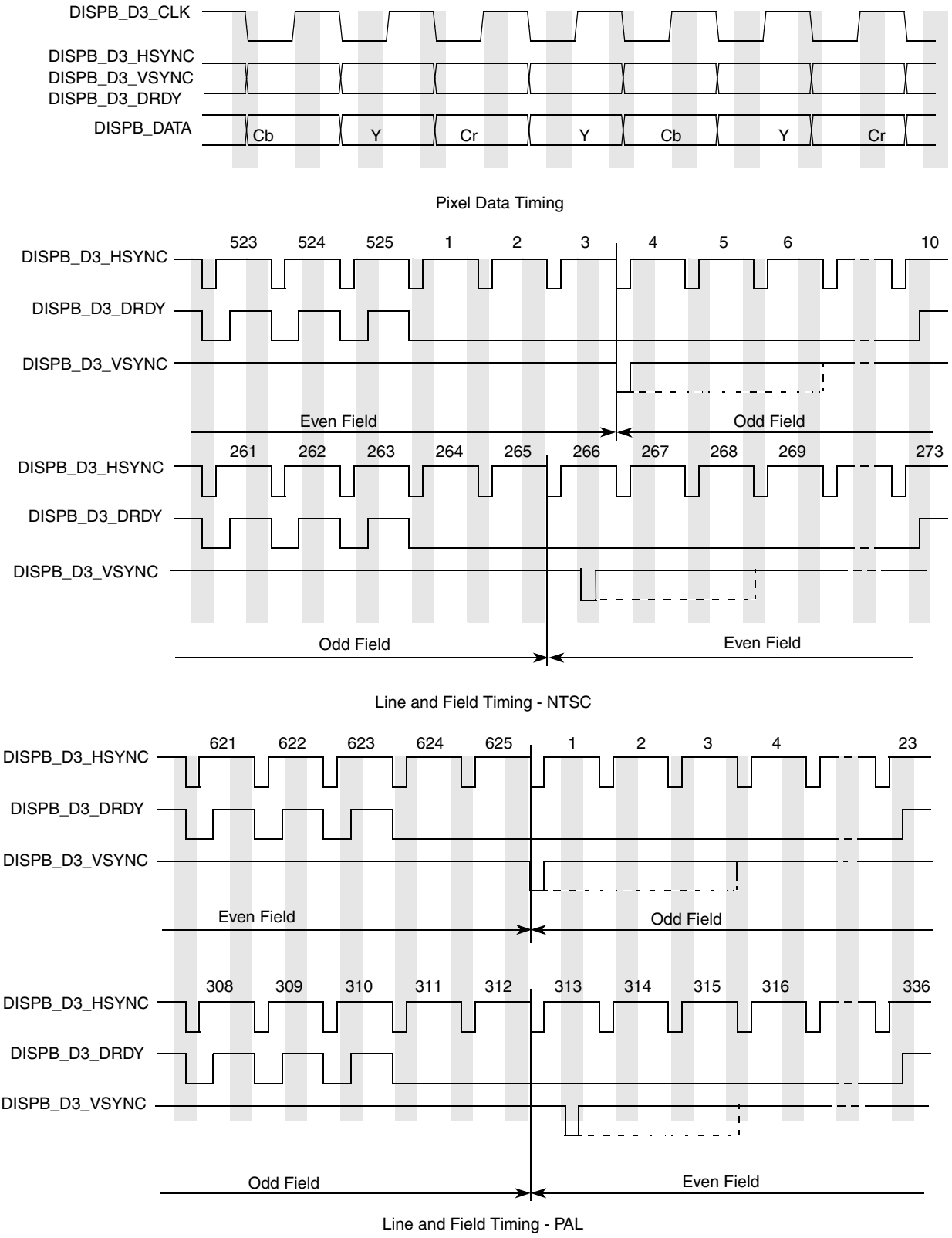

Figure 52. TV Encoder Interface Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

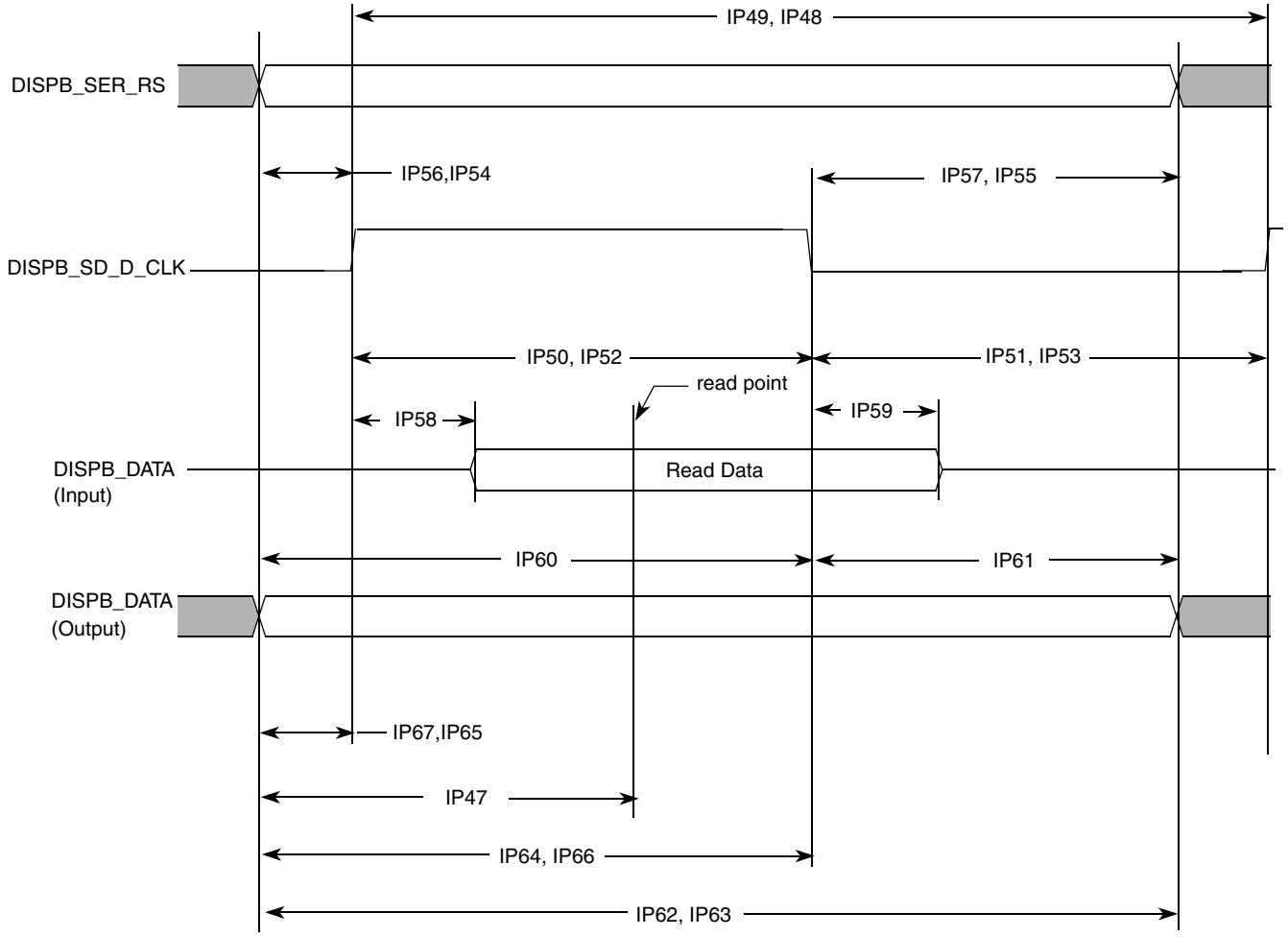

Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

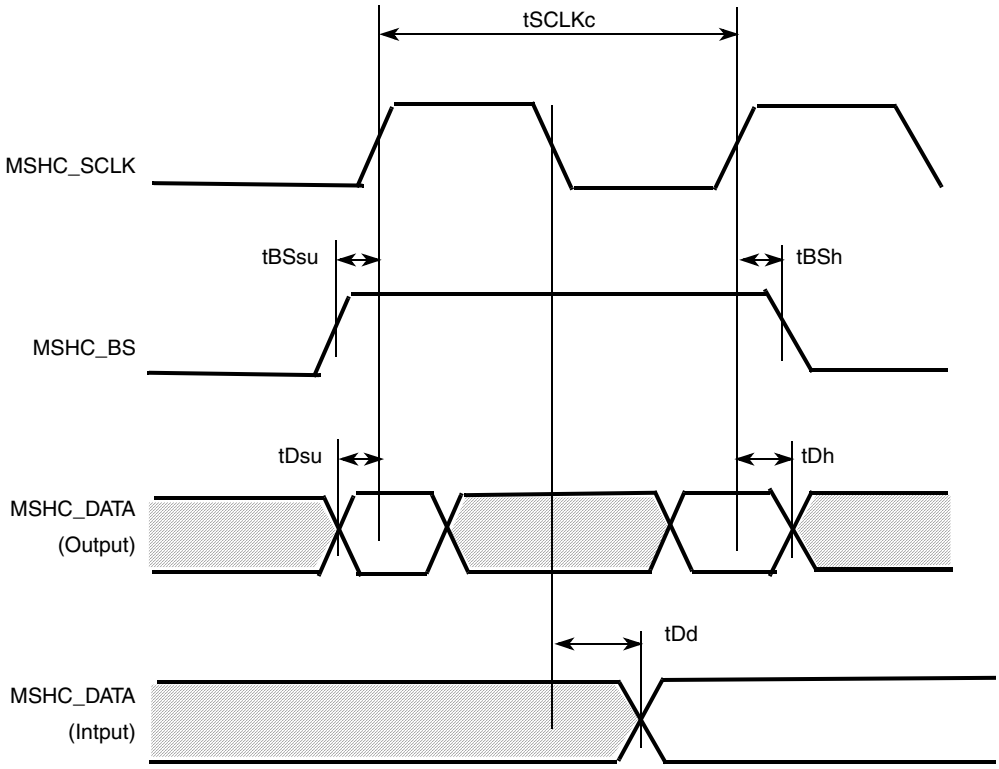

Figure 68. Transfer Operation Timing Diagram (Serial)

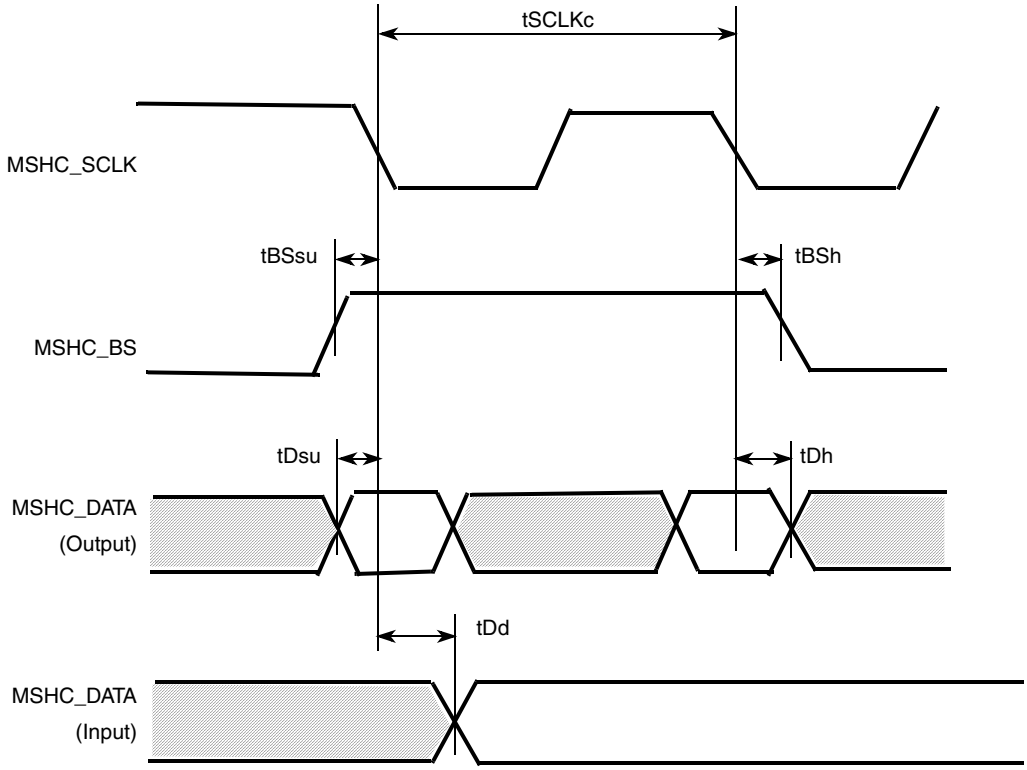

Figure 69. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 60. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 62. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	256 × Fs 512 × Fs
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	256 × Fs 256 × Fs PLL unlocked
		14.5 14	17 16.5	— —	ns	512 × Fs 512 × Fs PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note[2]
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note[3]

1 The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below unless otherwise noted.

Table 63. MLB Device 1024Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: 1024 × Fs at 44.0 kHz Typ: 1024 × Fs at 48.0 kHz Max: 1024 × Fs at 48.1 kHz Max: 1024 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	—
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	PLL unlocked

4.9.22.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver timing with internal clock. Table 79 lists the timing parameters shown in Figure 93.

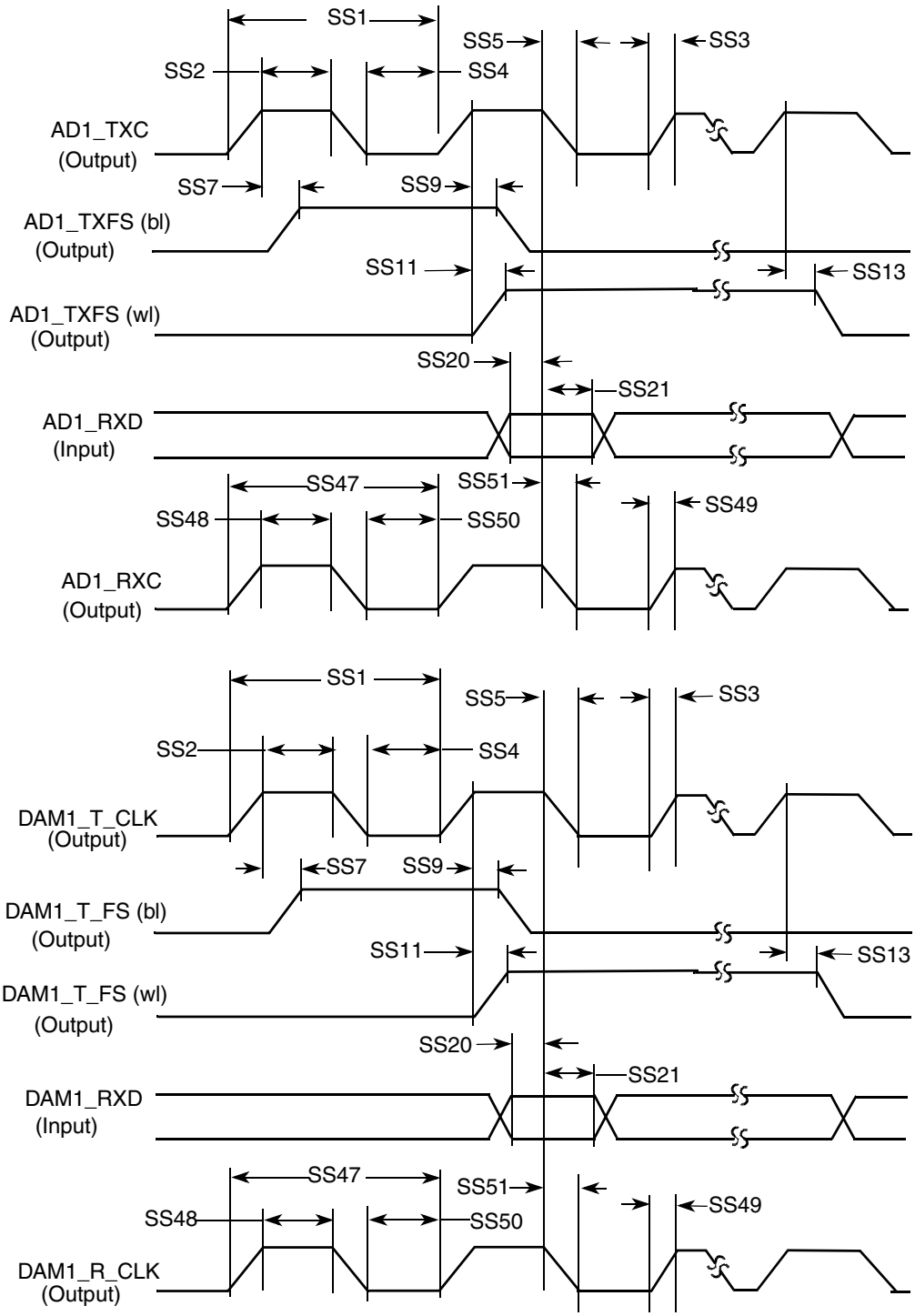

Figure 93. SSI Receiver with Internal Clock Timing Diagram

Table 87 describes the port timing specification in DAT_SE0 bidirectional mode.

Table 87. Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.9.24.2 DAT_SE0 Unidirectional Mode

Table 88 defines the signals for DAT_SE0 unidirectional mode. Figure 102 and Figure 103 show the transmit and receive waveforms respectively.

Table 88. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

Transmit

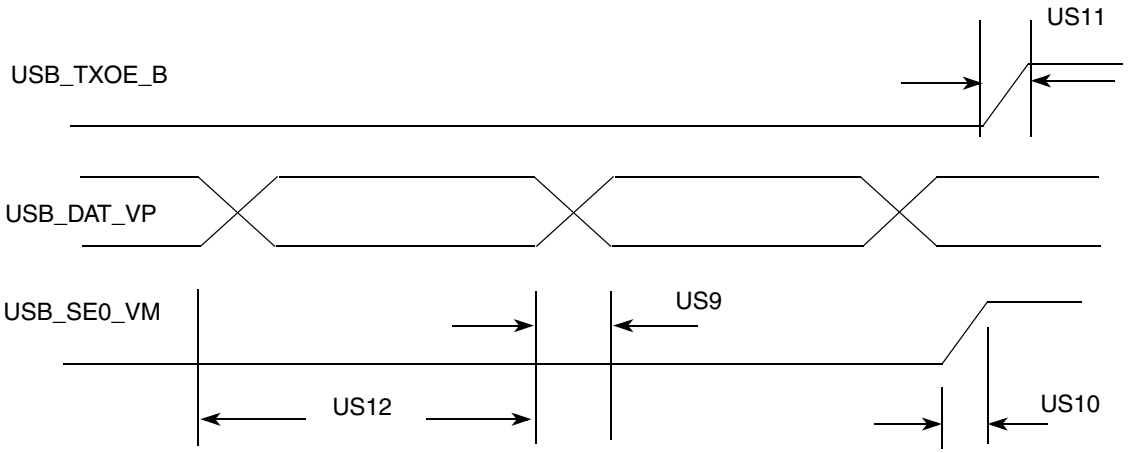

Figure 102. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

5.1 MAPBGA Production Package 1568-01, 17 × 17 mm, 0.8 Pitch

See Figure 108 for the package drawing and dimensions of the production package.

Figure 108. Production Package: Mechanical Drawing

Table 95. Silicon Revision 2.1 Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A18	D12
SDQS1	E11
A19	D11
A2	E7
A21	D10
SDQS2	E10
A22	D9
SDQS3	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN[1]	T5
ATA_CS0	V7
ATA_CS1	T7
ATA_DA0	R4
ATA_DA1	V1
ATA_DA2	R5
ATA_DATA0	Y5
ATA_DATA1	W5
ATA_DATA10	V3
ATA_DATA11	Y2
ATA_DATA12	U3
ATA_DATA13	W2
ATA_DATA14	W1
ATA_DATA15	T4
ATA_DATA2	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4

Signal ID	Ball Location
ATA_DATA7	Y3
ATA_DATA8	U4
ATA_DATA9	W3
ATA_DIOR	Y6
ATA_DIOW	W6
ATA_DMACK	V6
ATA_DMARQ	T3
ATA_INTRQ	V2
ATA_IORDY	U6
ATA_RESET_B	T6
SDQS0	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
RAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10	V16
CSI_D11	T15
CSI_D12	W16
CSI_D13	V15
CSI_D14	U14
CSI_D15	Y16
CSI_D8	U15
CSI_D9	W17
CSI_HSYNC	V14
CSI_MCLK	W15
CSI_PIXCLK	Y15
CSI_VSYNC	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3