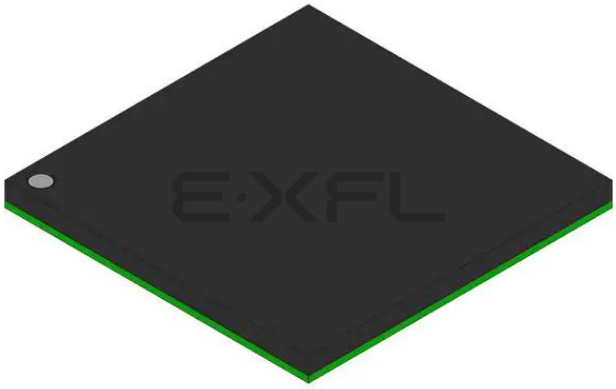

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx357cvm5b

SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU) (not available for the MCIMX351)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface (CE-ATA is not available for the MCIMX351)
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I^2C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)
- Parallel ATA (up to 66 Mbytes) (not available for the MCIMX351)

Table 21. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 22. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 23. AC Requirements of DDR2 Pins

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	VIL(ac)	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output[2]	Vox(ac)	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

[1] The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

Table 35. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns
SD9	Data out hold time[1]	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 44 and Table 45.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

NOTE

Test conditions are: pin voltage 1.7 V–1.95 V, capacitance 15 pF for all pins (both DDR and non-DDR pins), drive strength is high (7.2 mA). “High” is defined as 80% of signal value and “low” is defined as 20% of signal value.

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value. tCH + tCL will not exceed 7.5 ns for 133 MHz. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

The timing parameters are similar to the ones used in SDRAM data sheets. Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

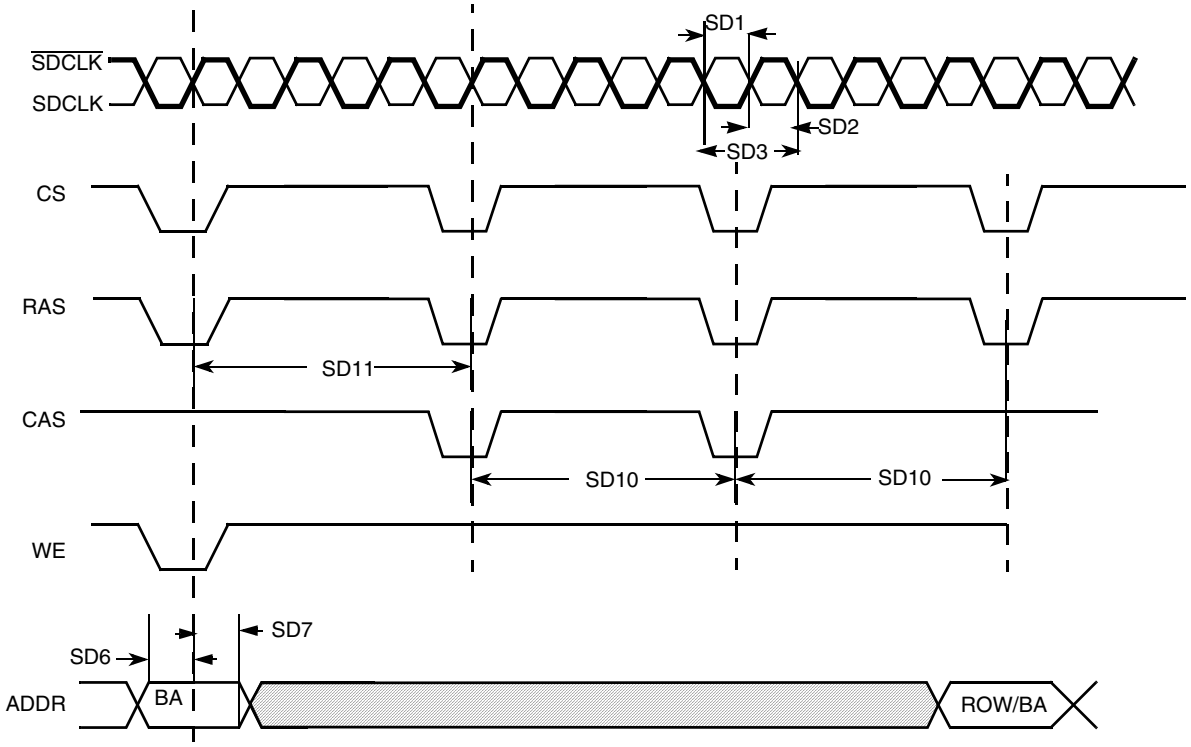

Figure 29. SDRAM Refresh Timing Diagram

Table 37. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns

Table 39. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	1.25	—	ns
DDR6	Address output setup time	t_{IS}[1]	1.5	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 40. Derating Values for DDR2–400, DDR2–533

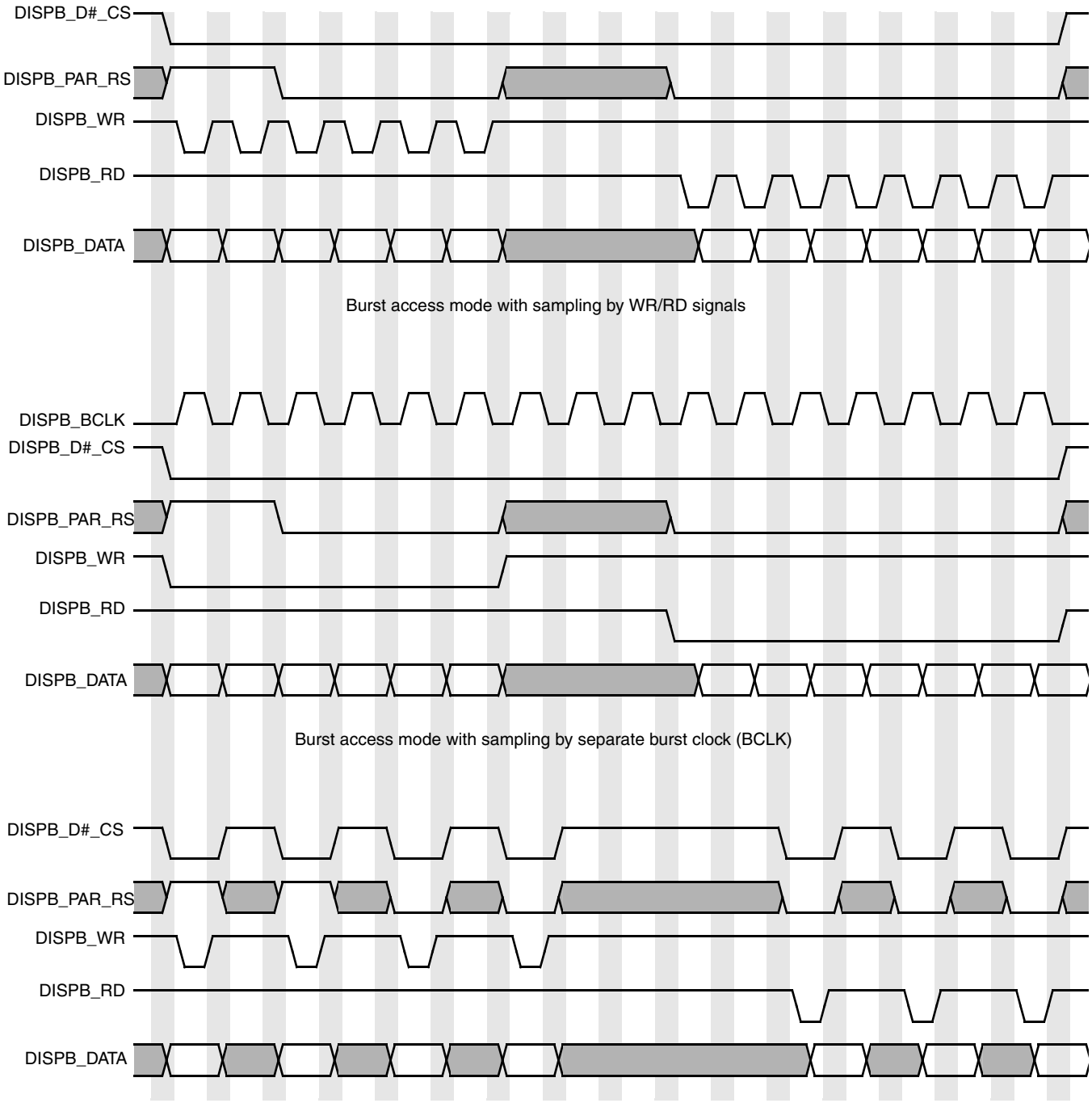

Figure 54. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

timing images are based on active low control signals (signal polarity is controlled via the DI_DISP_SIG_POL register).

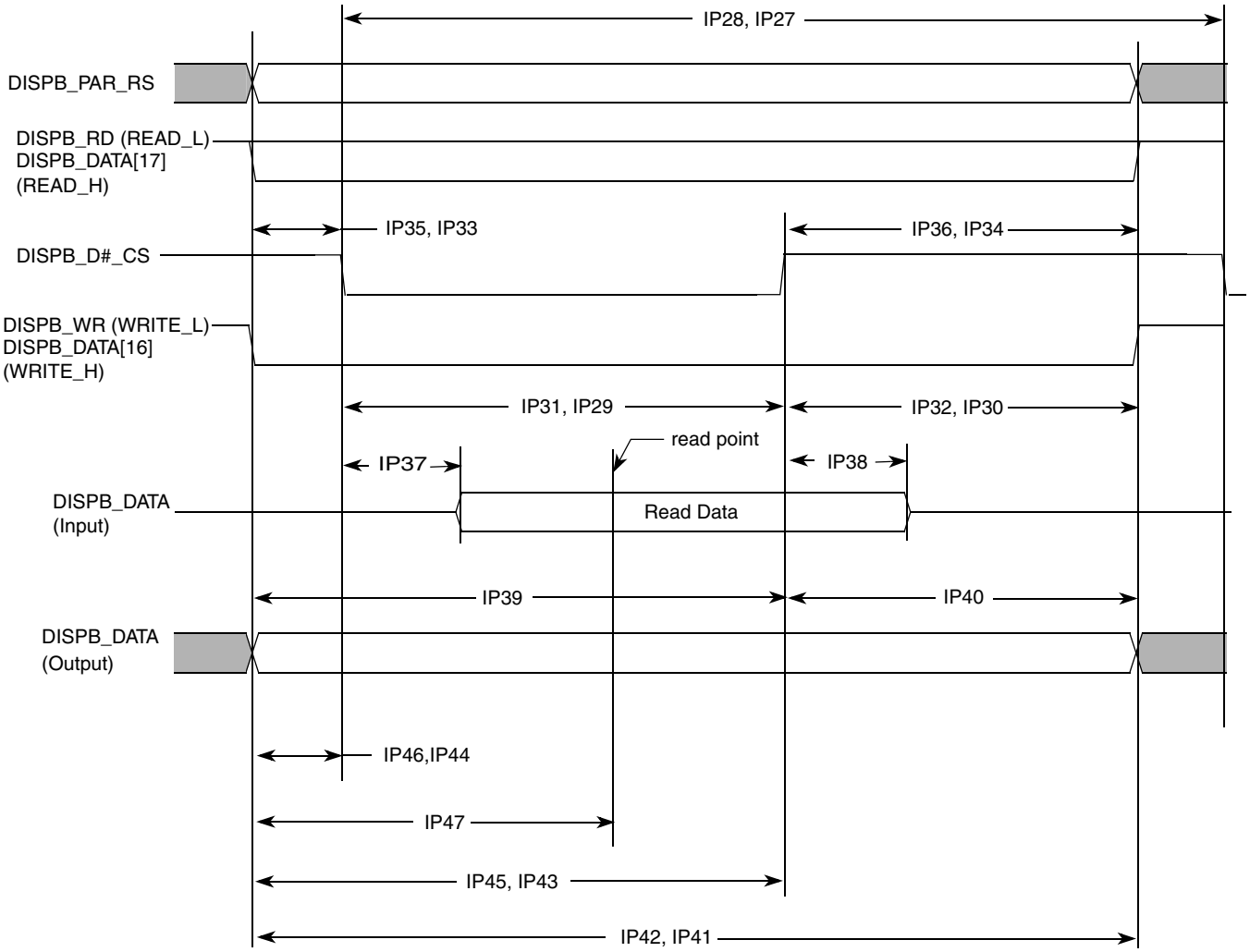

Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

[9] Data read point:

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, and an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR
- DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.14 Memory Stick Host Controller (MSHC)

Figure 67, Figure 68, and Figure 69 depict the MSHC timings, and Table 60 and Table 61 list the timing parameters.

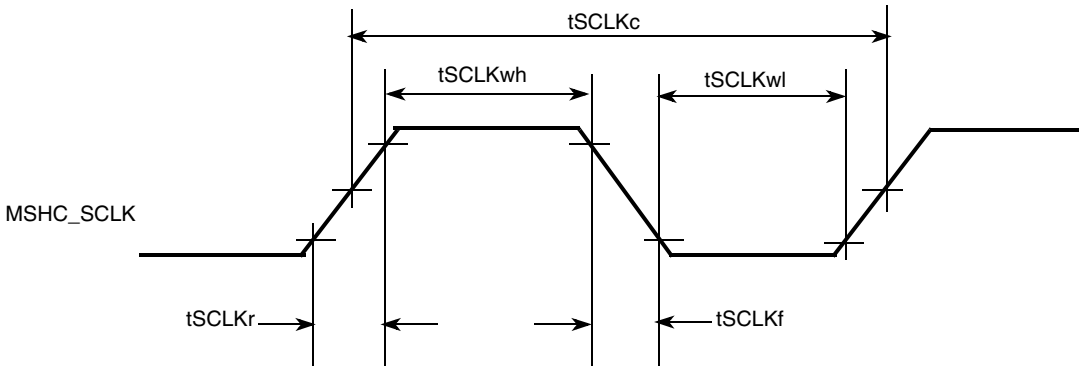

Figure 67. MSHC_CLK Timing Diagram

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

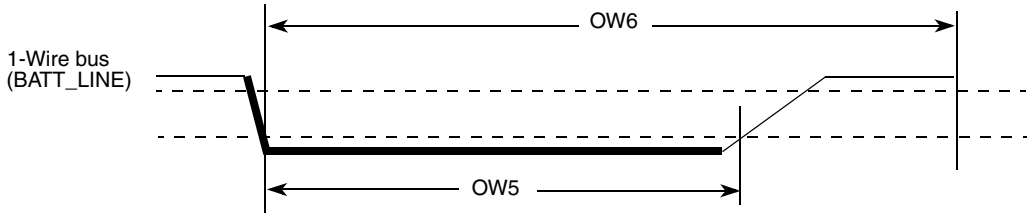

Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

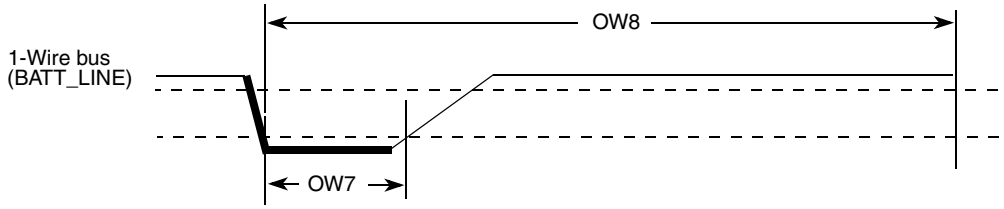

Figure 72. Write 1 Sequence Timing Diagram

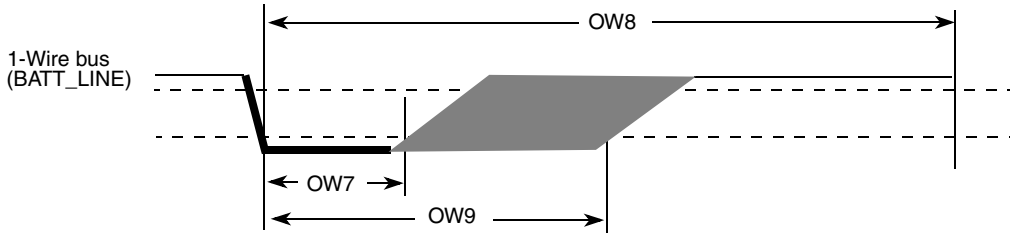

Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

Table 79. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

Table 81. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.9.23 UART Electrical

This section describes the electrical information of the UART module.

4.9.23.1 UART RS-232 Serial Mode Timing

The following subsections give the UART transmit and receive timings in RS-232 serial mode.

4.9.23.1.11 UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 82 lists the UART RS-232 serial mode transmit timing characteristics.

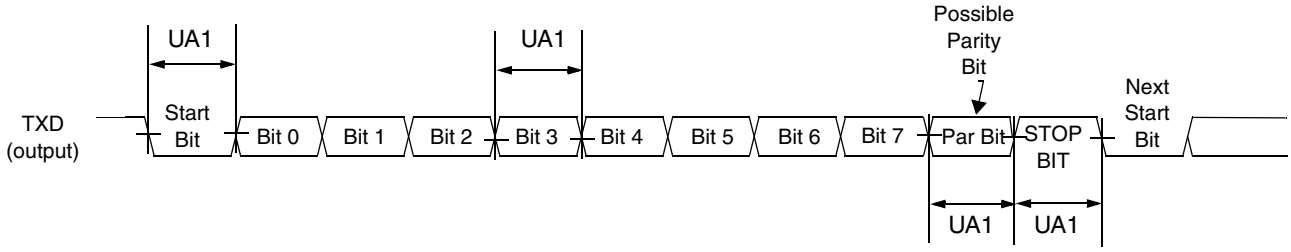

Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Receive

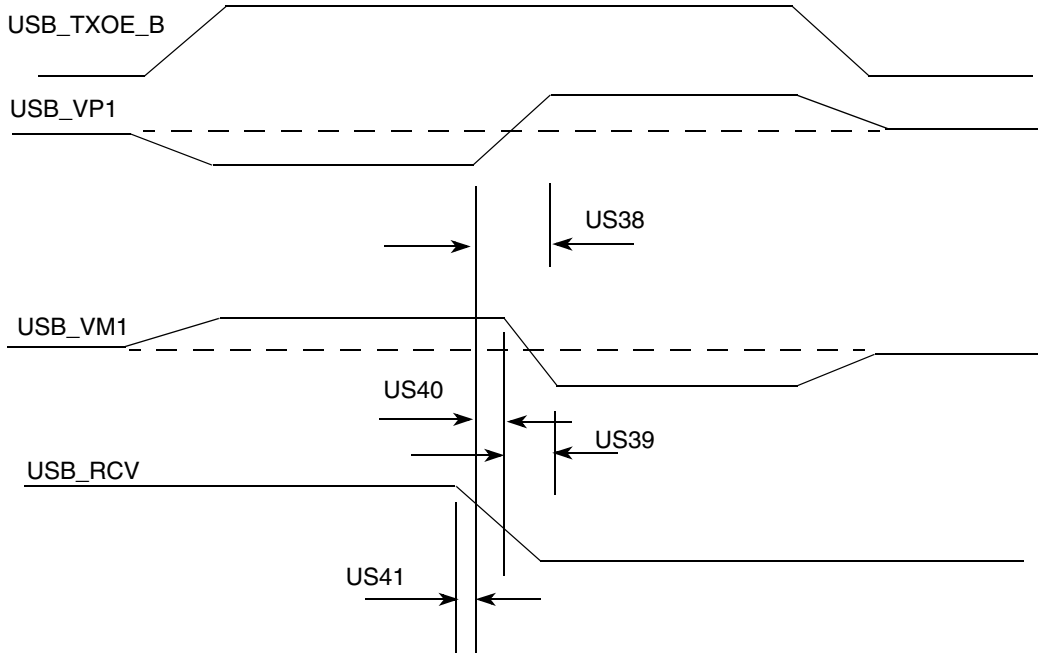

Figure 107. USB Receive Waveform in VP_VM Unidirectional Mode

Table 93 describes the port timing specification in VP_VM unidirectional mode.

Table 93. USB Timing Specification in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx overlap	USB_SE0_VM	Out	–3.0	+3.0	ns	USB_DAT_VP
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	In	–4.0	+4.0	ns	USB_VM1
US41	Rx skew	USB_RCV	In	–6.0	+2.0	ns	USB_VP1

5 Package Information and Pinout

This section includes the following:

- Mechanical package drawing
- Pin/contact assignment information

5.1 MAPBGA Production Package 1568-01, 17 × 17 mm, 0.8 Pitch

See Figure 108 for the package drawing and dimensions of the production package.

Figure 108. Production Package: Mechanical Drawing

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
ATA_DATA13[1]	W2
ATA_DATA14[1]	W1
ATA_DATA15[1]	T4
ATA_DATA2[1]	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS[1]	L17
D3_DRDY[1]	L20
D3_FPSHIFT[1]	L15
D3_HSYNC[1]	L18
D3_REV[1]	M17
D3_SPL[1]	M18
D3_VSYNC[1]	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
DQM1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1

Signal ID	Ball Location
CSI_VSYNC[1]	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0[1]	F20
LD1[1]	G18
LD10[1]	H20
LD11[1]	J18
LD12[1]	J16
LD13[1]	J19
LD14[1]	J17
LD15[1]	J20
LD16[1]	K14
LD17[1]	K19
LD18[1]	K18
LD19[1]	K20
LD2[1]	G17
LD20[1]	K16
LD21[1]	K17
LD22[1]	K15

Table 94. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
NVCC_EMI1	G7
NVCC_EMI1	G8
NVCC_EMI1	G9
NVCC_EMI1	H9
NVCC_EMI1	F10
NVCC_EMI1	G10
NVCC_EMI1	F11
NVCC_EMI1	G11
SD1_CLK	V18
SD1_CMD	Y19
SD1_DATA0	R14
SD1_DATA1	U16
SD1_DATA2	W18
SD1_DATA3	V17
SD10	A15
SD11	B15
SD12	C13
SD13	B14
SD14	A14
SD15	B13
SD16	C12
SD17	C11
SD18	A12
SD19	B12
SD2	B18
SD2_CLK	W14
SD2_CMD	U13
SD2_DATA0	V13
SD2_DATA1	T13
SD2_DATA2	Y14
SD2_DATA3	U12
SD20	B11
SD21	A11
SD22	C10
SD23	B10
SD24	A9
SD25	C9
SD26	B9
SD27	A8
SD28	B8
SD29	C8
SD3	C16
SD30	A7
SD31	B7
SD4	A18
SD5	C15

Signal ID	Ball Location
RXD1	U2
RXD2	H3
SCK4	L4
SCK5	L5
SCKR	K3
SCKT	J4
SD0	C17
SD1	A19
SDCLK	E12
SDCLK_B	E13
SDQS0	B17
SDQS1	A13
SDQS2	A10
SDQS3	C7
SDWE	G15
SJC_MOD	U17
SRXD4	L1
SRXD5	K4
STXD4	M2
STXD5	K1
STXFS4	L2
STXFS5	J6
TCK	R17
TDI	P15
TDO	R15
TEST_MODE	Y7
TMS	R16
TRSTB	T16
TTM_PIN	M16
TX0	G4
TX1	H1
TX2_RX3	H5
TX3_RX2	J2
TX4_RX1	H4
TX5_RX0	J3
TXD1	R6
TXD2	H2
USBOTG_OC	U7
USBOTG_PWR	W7
USBPHY1_DM	N19
USBPHY1_DP	P19
USBPHY1_RREF	R19
USBPHY1_UID	N18
USBPHY1_UPLLGND	N14
USBPHY1_UPLLVDD	N15
USBPHY1_UPLLVDD	P17

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
CTS2	G5
D0	A2
D1	D4
D10	D2
D11	E6
D12	E3
D13	F5
D14	D1
D15	E2
D2	B2
D3	E5
D3_CLS	L17
D3_DRDY	L20
D3_FPSHIFT	L15
D3_HSYNC	L18
D3_REV	M17
D3_SPL	M18
D3_VSYNC	M19
D4	C3
D5	B1
D6	D3
D7	C2
D8	C1
D9	E4
DE_B	W19
DQM0	B19
SDCKE1	D17
DQM2	D16
DQM3	C18
EB0	F18
EB1	F16
ECB	D19
EXT_ARMCLK	V8
EXTAL_AUDIO	W20
EXTAL24M	T20
FEC_COL	P3
FEC_CRS	N5
FEC_MDC	R1
FEC_MDIO	P1
FEC_RDATA0	P2
FEC_RDATA1	N2
FEC_RDATA2	M3
FEC_RDATA3	N1
FEC_RX_CLK	R2
FEC_RX_DV	T2
FEC_RX_ERR	N3

Signal ID	Ball Location
FEC_TDATA0	P5
FEC_TDATA1	M4
FEC_TDATA2	M5
FEC_TDATA3	L6
FEC_TX_CLK	P4
FEC_TX_EN	T1
FEC_TX_ERR	N4
FSR	K5
FST	J1
FUSE_VDD	P13
FUSE_VSS	M11
GPIO1_0	T11
GPIO1_1	Y11
GPIO2_0	U11
GPIO3_0	V11
HCKR	K2
HCKT	J5
I2C1_CLK	M20
I2C1_DAT	N17
I2C2_CLK	L3
I2C2_DAT	M1
LBA	D20
LD0	F20
LD1	G18
LD10	H20
LD11	J18
LD12	J16
LD13	J19
LD14	J17
LD15	J20
LD16	K14
LD17	K19
LD18	K18
LD19	K20
LD2	G17
LD20	K16
LD21	K17
LD22	K15
LD23	L19
LD3	G16
LD4	G19
LD5	H16
LD6	H18
LD7	G20
LD8	H17
LD9	H19

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 97. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	GND	GND	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD3	VDD3	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD4	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_REF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	GND	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMACK	ATA_CS0	EXT_ARMCLK	CSPI1_MISO	CLKO	GPIO3_0	CAPTURE	SD2_DATA0	CSI_HSYNC	CSI_D13	CSI_D10	SD1_DATA3	SD1_CLK	XTAL_AUDIO	OSC_AUDIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIOW	USBOTG_PWR	CSPI1_SCLK	CSPI1_MOSI	BOOT_MODE0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA2	DE_B	EXTAL_AUDIO	W
Y	GND	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIOR	TEST_MODE	CSPI1_SS0	POWER_FAIL	CLK_MODE0	GPIO1_1	WDOG_RST	MLB_DAT	SD2_DATA2	CSI_PIXCLK	CSI_D15	USBPHY2_DM	USBPHY2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at http://www.freescale.com/imx.

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