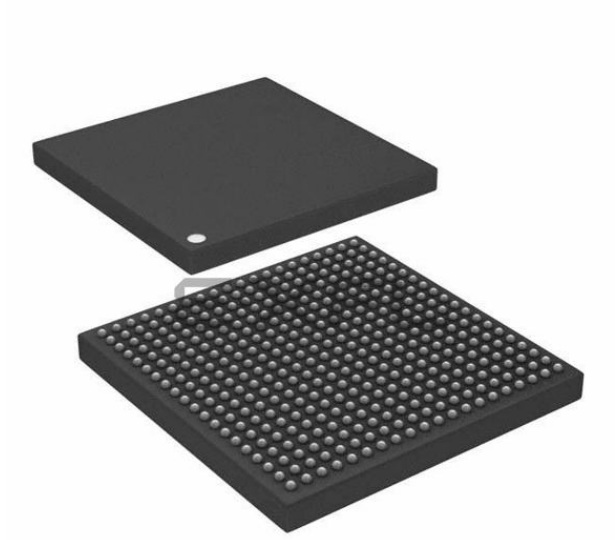

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx357djq5c

- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX353	MCIMX353CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX353	MCIMX353DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX357	MCIMX357CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX357	MCIMX357DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX353	MCIMX353CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX353	MCIMX353DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97
i.MX357	MCIMX357CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX357	MCIMX357DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

Table 2. Functional Differences in the i.MX35 Parts

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
I2C (3)	Yes	Yes	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes	Yes	Yes
ESAI	Yes	Yes	Yes	Yes	Yes
SPDIF I/O	Yes	Yes	Yes	Yes	Yes
USB HS Host	Yes	Yes	Yes	Yes	Yes
USB OTG	Yes	Yes	Yes	Yes	Yes
FlexCAN (2)	Yes	Yes	Yes	Yes	Yes
MLB	Yes	Yes	Yes	Yes	Yes

Table 2. Functional Differences in the i.MX35 Parts (continued)

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
Ethernet	Yes	Yes	Yes	Yes	Yes
1-Wire	Yes	Yes	Yes	Yes	Yes
KPP	Yes	Yes	Yes	Yes	Yes
SDIO/MMC (2)	Yes	Yes	Yes	Yes	Yes
SDIO/Memory Stick	Yes	Yes	Yes	Yes	Yes
External Memory Controller (EMC)	Yes	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
PATA	—	Yes	Yes	Yes	Yes
CE-ATA	—	Yes	Yes	Yes	Yes
Image Processing Unit (IPU) (inversion and rotation, pre- and post-processing, camera interface, blending, display controller)	—	Yes	Yes	Yes	Yes
Open VG graphics acceleration (GPU)	—	Yes	—	Yes	Yes

[1] ARM = ARM1136 platform, SDMA = SDMA platform

3 Signal Descriptions: Special Function Related Pins

Some special functional requirements are supported in the device. The details about these special functions and the corresponding pin names are listed in Table 5.

Table 5. Special Function Related Pins

Function Name	Pin Name	Mux Mode	Detailed Description
External ARM Clock	EXT_ARMCLK	ALT0	External clock input for ARM clock.
External Peripheral Clock	I2C1_CLK	ALT6	External peripheral clock source.
External 32-kHz Clock	CAPTURE	ALT4	External clock input of 32 kHz, used when the internal 24M Oscillator is powered off, which could be configured either from CAPTURE or CSPI1_SS1.
	CSPI1_SS1	ALT2	
Clock Out	CLKO	ALT0	Clock-out pin from CCM, clock source is controllable and can also be used for debug.
Power Ready	GPIO1_0	ALT1	PMIC power-ready signal, which can be configured either from GPIO1_0 or TX1.
	TX1	ALT1	
Tamper Detect	GPIO1_1	ALT6	Tamper-detect logic is used to issue a security violation. This logic is activated if the tamper-detect input is asserted. Tamper-detect logic is enabled by the bit of IOMUXC_GPRA[2]. After enabling the logic, it is impossible to disable it until the next reset.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 7 on page 13
i.MX35 Operating Ranges	Table 8 on page 13
Interface Frequency	Table 9 on page 14

[2] The typical value of Vox(ac) is expected to be about 0.5 × NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload = 25 pF.

Table 24. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 25. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

Figure 7 and Figure 8 depict the master mode and slave mode timings of the CSPI, and Table 27 lists the timing parameters.

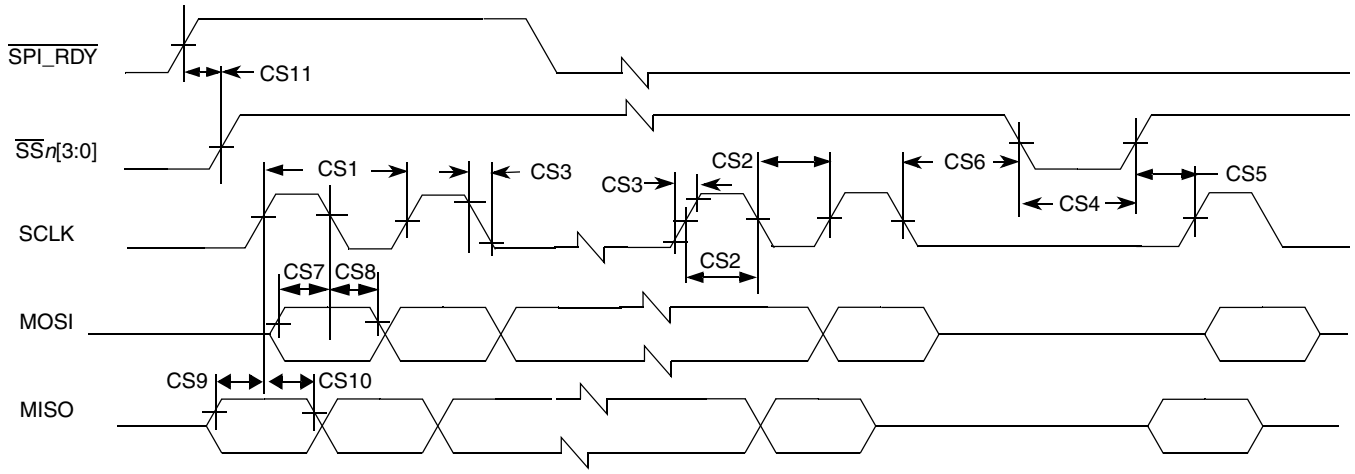

Figure 7. CSPI Master Mode Timing Diagram

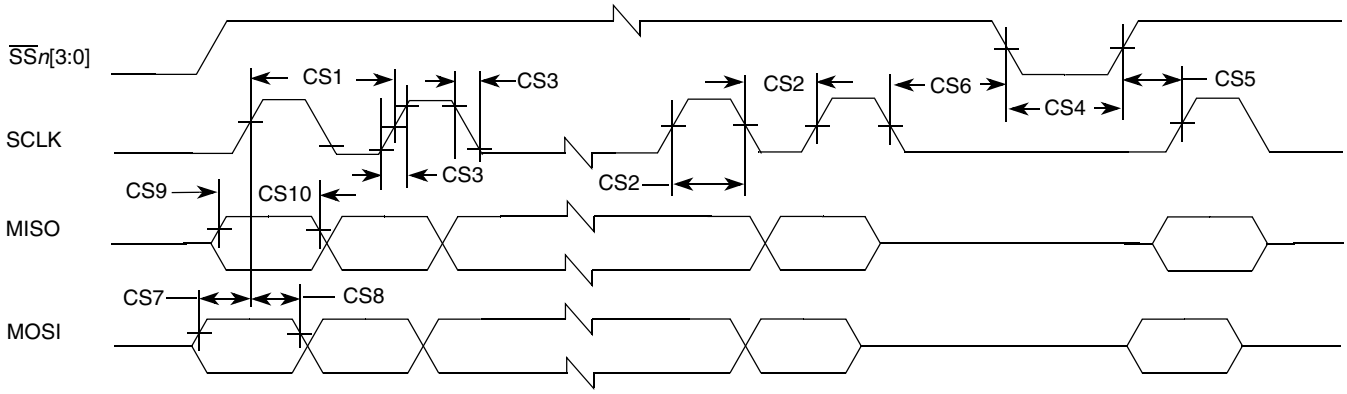

Figure 8. CSPI Slave Mode Timing Diagram

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
CS1	SCLK cycle time	t_{clk}	60	—	ns
CS2	SCLK high or low time	t_{SW}	30	—	ns
CS3	SCLK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SS}n$[3:0] pulse width	t_{CSLH}	30	—	ns
CS5	$\overline{SS}n$[3:0] lead time (CS setup time)	t_{SCS}	30	—	ns
CS6	$\overline{SS}n$[3:0] lag time (CS hold time)	t_{HCS}	30	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns

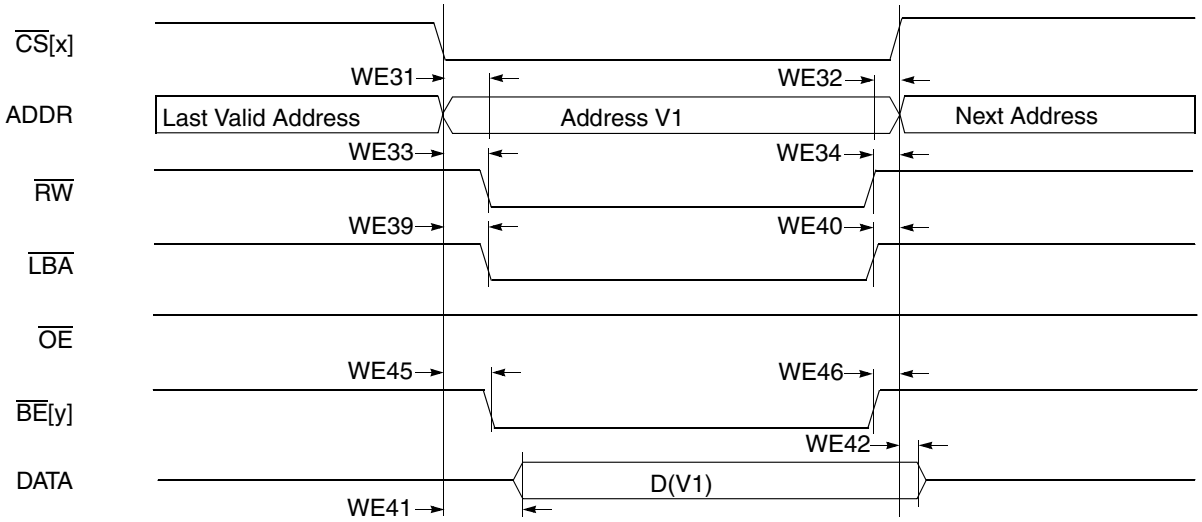

Figure 24. Asynchronous Memory Write Access

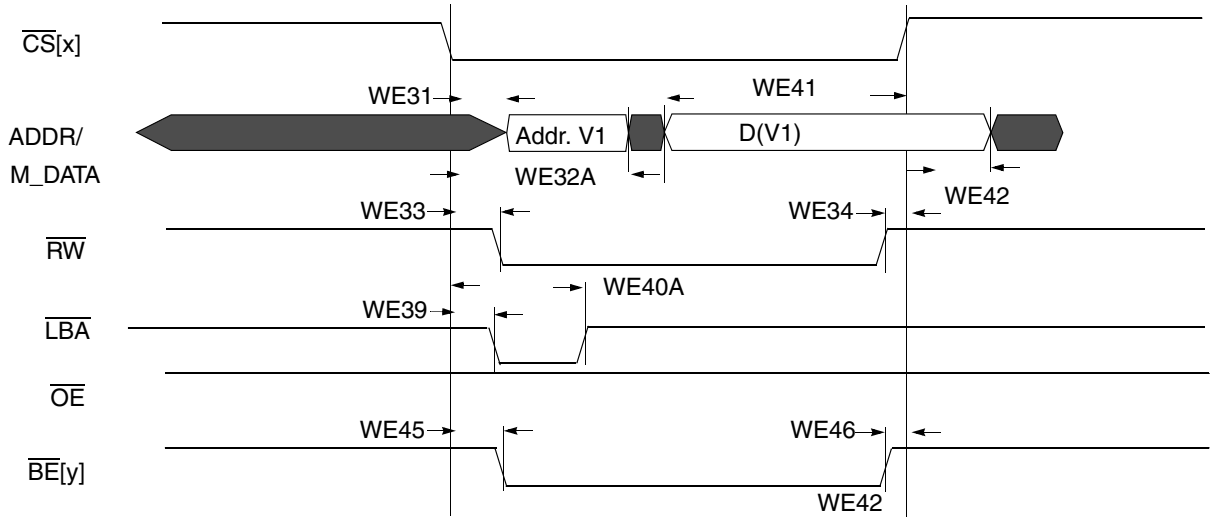

Figure 25. Asynchronous A/D Mux Write Access

Table 34. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE40A (muxed A/D)	$\overline{CS}$[x] valid to $\overline{LBA}$ invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] valid to Output Data valid	WE16 – WE6 + (WLBN + WLBA + ADH + 1 – WCSA)	—	3 + (WLBN + WLBA + ADH + 1 – WCSA)	ns
WE42	Output Data invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] valid to $\overline{BE}$[y] valid (write access)	WE12 – WE6 + (WBEA – CSA)	—	3 + (WBEA – CSA)	ns
WE46	$\overline{BE}$[y] invalid to $\overline{CS}$[x] invalid (write access)	WE7 – WE13 + (WBEN – CSN)	—	–3 + (WBEN – CSN)	ns
WE47	$\overline{DTACK}$ valid to $\overline{CS}$[x] invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

1 For the value of parameters WE4–WE21, see column BCD = 0 in Table 33.

2 $\overline{CS}$ Assertion. This bit field determines when the $\overline{CS}$ signal is asserted during read/write cycles.

3 $\overline{CS}$ Negation. This bit field determines when the $\overline{CS}$ signal is negated during read/write cycles.

4 $\overline{BE}$ Assertion. This bit field determines when the $\overline{BE}$ signal is asserted during read cycles.

5 $\overline{BE}$ Negation. This bit field determines when the $\overline{BE}$ signal is negated during read cycles.

6 Output maximum delay from internal driving ADDR/control FFs to chip outputs.

7 Output maximum delay from $\overline{CS}$[x] internal driving FFs to $\overline{CS}$[x] out.

8 DATA maximum delay from chip input data to its internal FF.

9 DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA, CSN, WBEA, WBEN, LBA, LBN, OEN, OEA, RBEA, and RBEN) are in cycle units.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

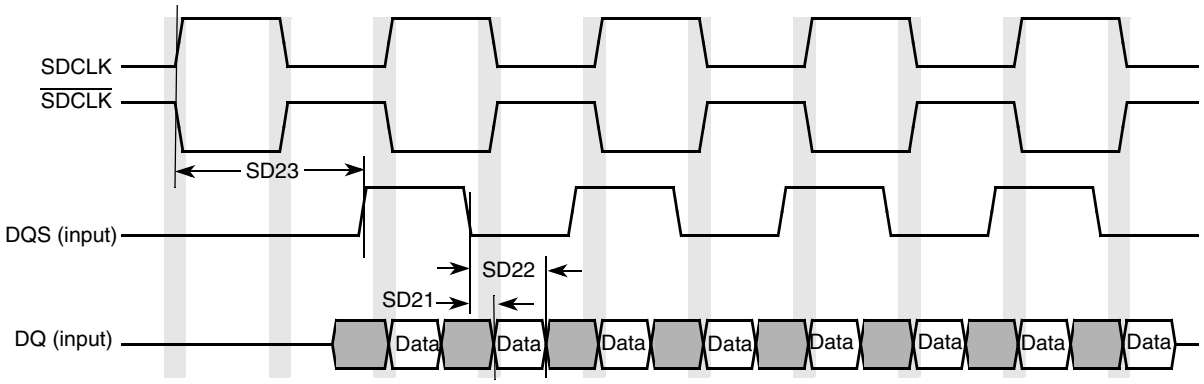

Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value, and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

Table 46. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min.	Max.	Condition[3]	Unit
80	SCKT rising edge to FST out (wr) high[5]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

Figure 41 shows MII asynchronous input timings listed in Table 50.

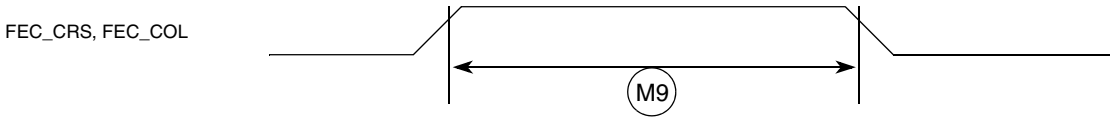

Figure 41. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 51 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 51. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 42 shows MII serial management channel timings listed in Table 51.

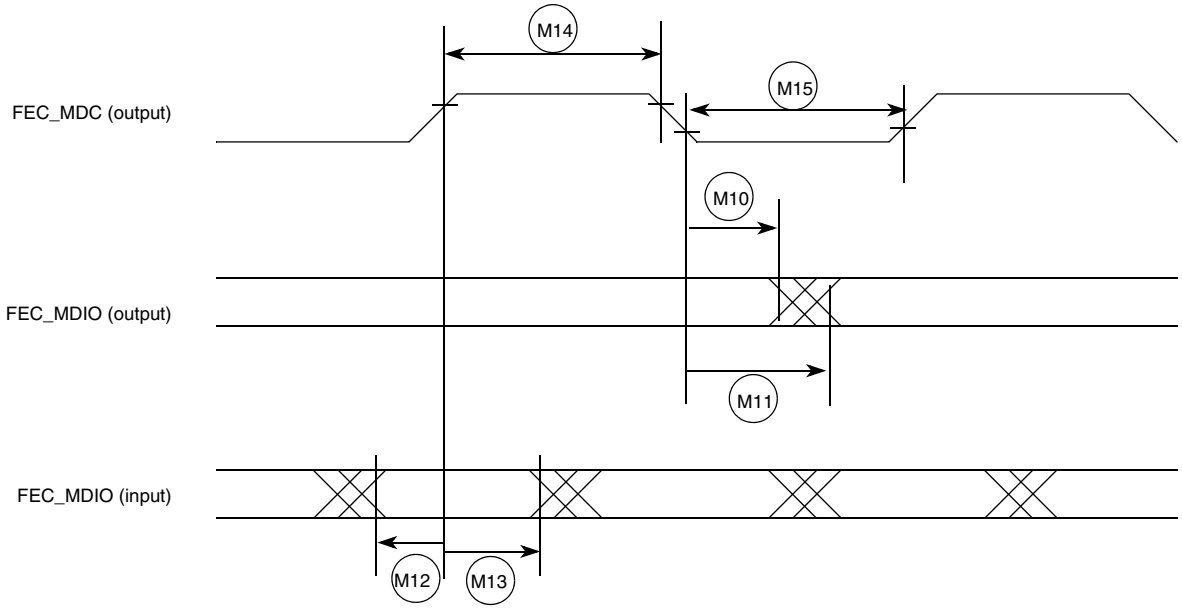

Figure 42. MII Serial Management Channel Timing Diagram

4.9.9 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) defined by IrDA® (Infrared Data Association). Refer to the IrDA® website for details on FIR and MIR protocols.

4.9.10 FlexCAN Module AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver outside the chip. The i.MX35 has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. Refer to the IOMUX chapter of the *MCIMX35 Multimedia Applications Processor Reference Manual* to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

The timing described in Figure 45 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.9.12.3 Electrical Characteristics

Figure 46 depicts the sensor interface timing, and Table 54 lists the timing parameters.

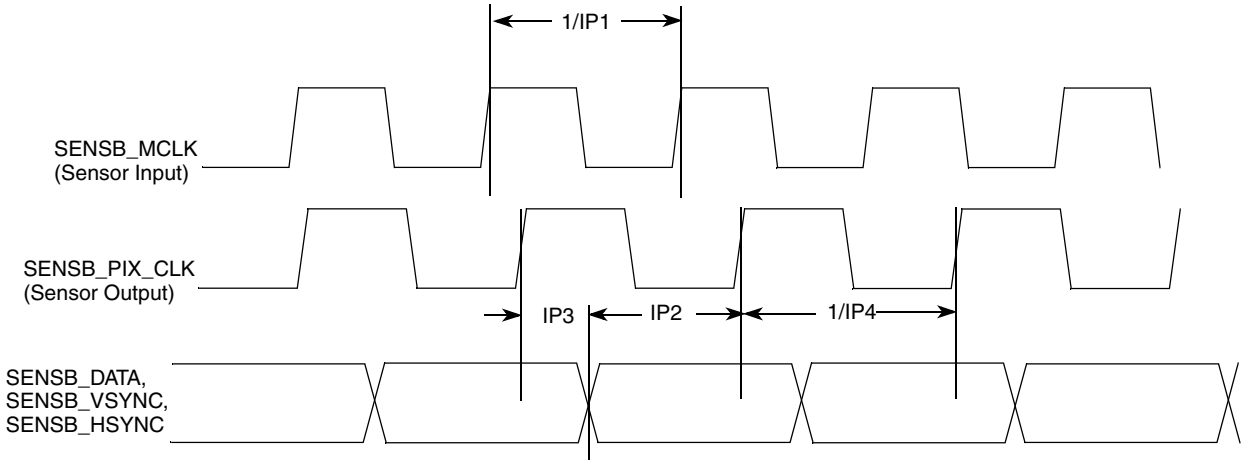

Figure 46. Sensor Interface Timing Diagram

Table 54. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.9.13 IPU–Display Interfaces

This section describes the following types of display interfaces:

- Section 4.9.13.1, “Synchronous Interfaces”
- Section 4.9.13.2, “Interface to Sharp HR-TFT Panels”
- Section 4.9.13.3, “Synchronous Interface to Dual-Port Smart Displays”
- Section 4.9.13.4, “Asynchronous Interfaces”
- Section 4.9.13.5, “Serial Interfaces, Functional Description”

Table 56. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd[2] – Tdicu[3]	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP3\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 51 depicts the Sharp HR-TFT panel interface timing, and Table 57 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

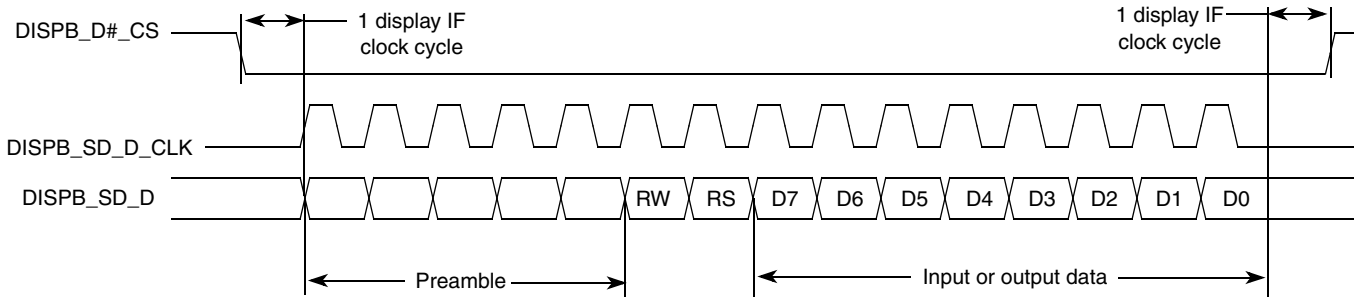

Figure 62. 3-Wire Serial Interface Timing Diagram

Figure 63 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

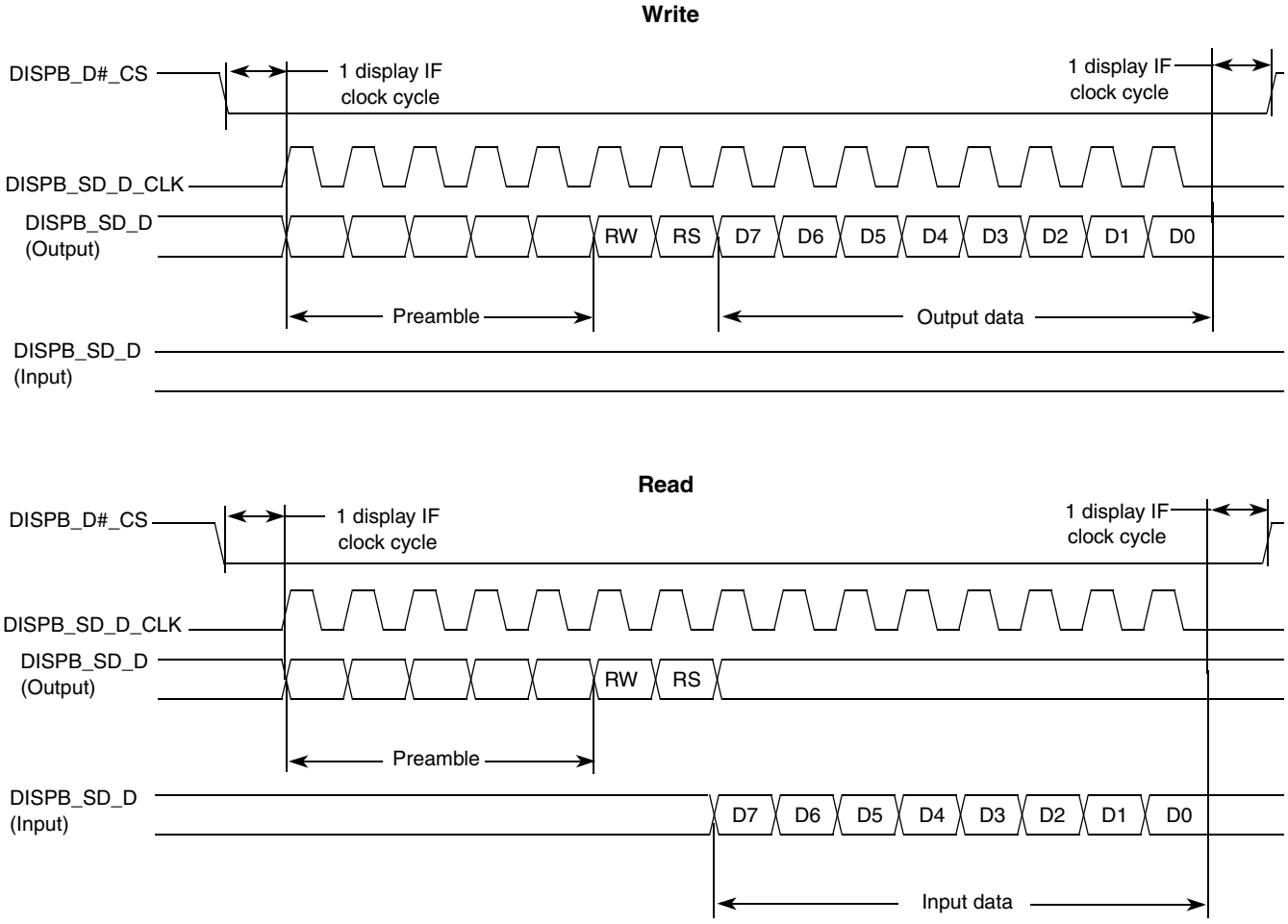

Figure 63. 4-Wire Serial Interface Timing Diagram

Figure 64 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

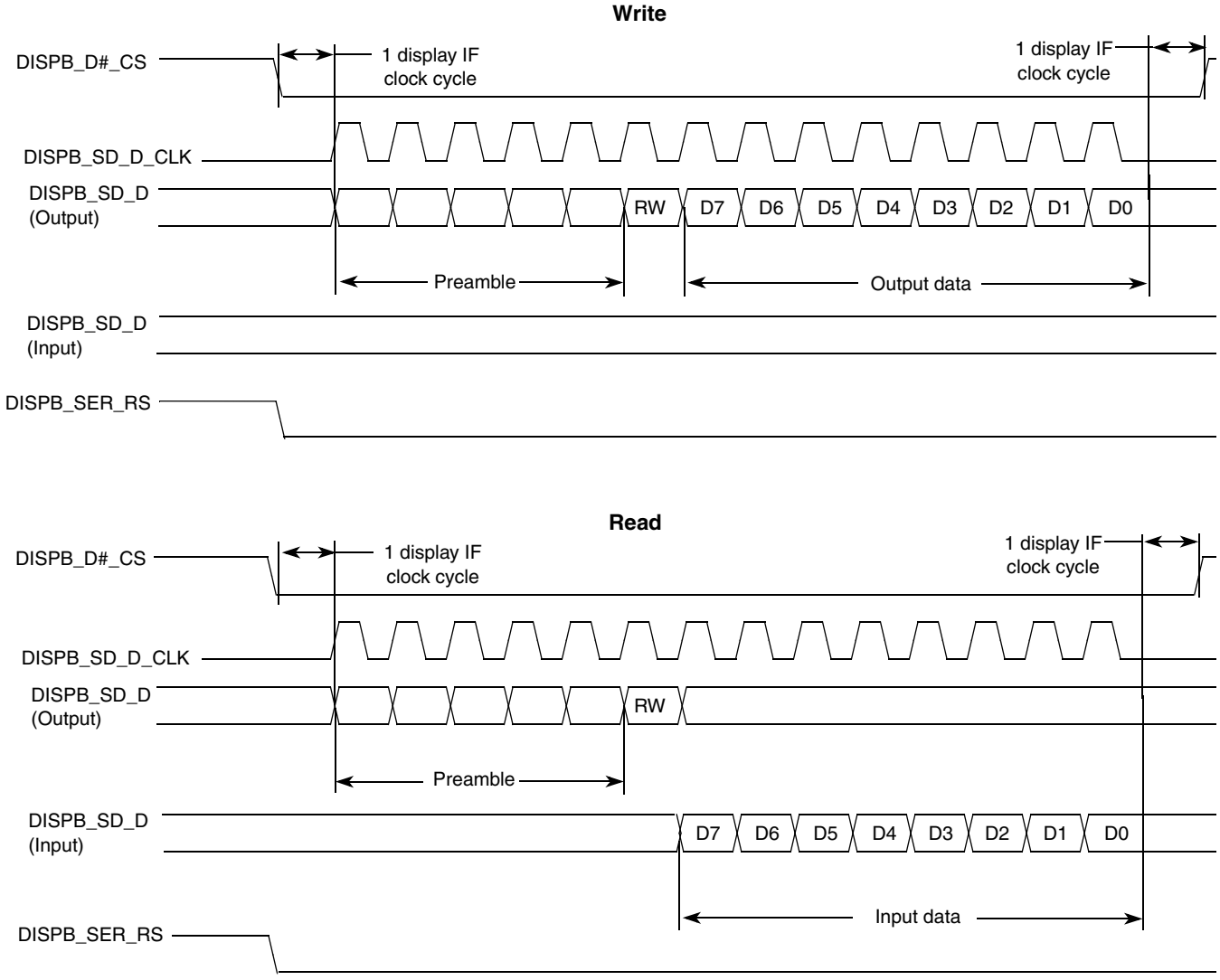

Figure 64. 5-Wire Serial Interface (Type 1) Timing Diagram

Table 60. Serial Interface Timing Parameters[1] (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 61.

Table 61. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in Table 8.

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 62. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} TO V_{IH}

Figure 71 depicts write 0 sequence timing, and Table 65 lists the timing parameters.

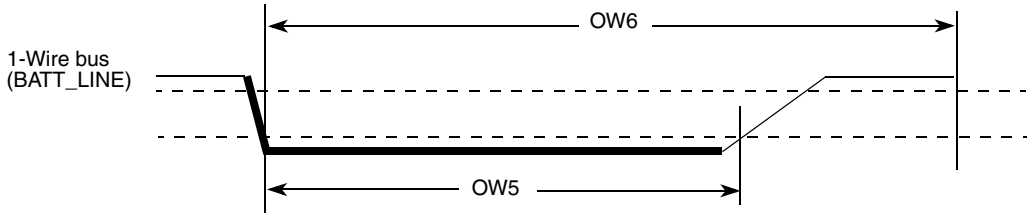

Figure 71. Write 0 Sequence Timing Diagram

Table 65. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	µs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	µs

Figure 72 shows write 1 sequence timing, and Figure 73 depicts the read sequence timing. Table 66 lists the timing parameters.

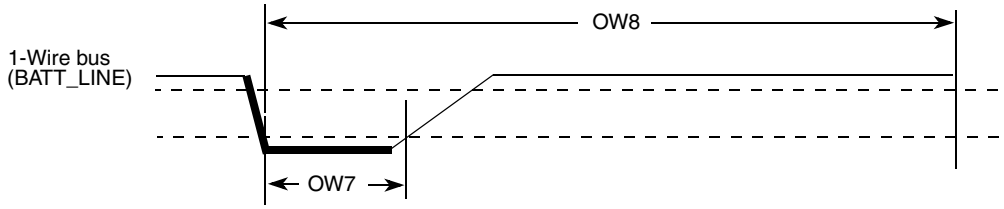

Figure 72. Write 1 Sequence Timing Diagram

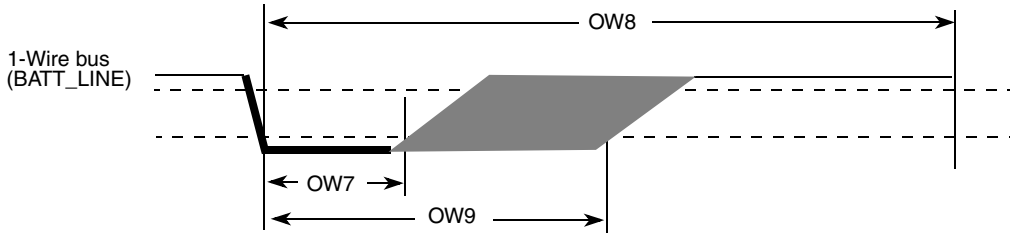

Figure 73. Read Sequence Timing Diagram

Table 66. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

pin. The modulated signal of the module is observed at this pin. It can be viewed as a clock signal whose period and duty cycle can be varied with different settings of the PWM. The smallest period is two ipg_clk periods with duty cycle of 50 percent.

4.9.20 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 86 depicts the SJC test clock input timing. Figure 87 depicts the SJC boundary scan timing, Figure 88 depicts the SJC test access port, Figure 89 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 76 lists the SJC timing parameters.

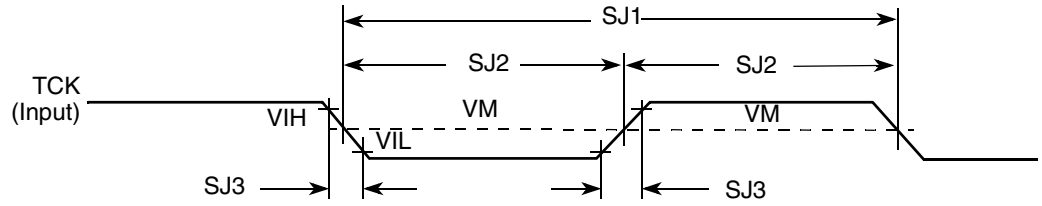

Figure 86. Test Clock Input Timing Diagram

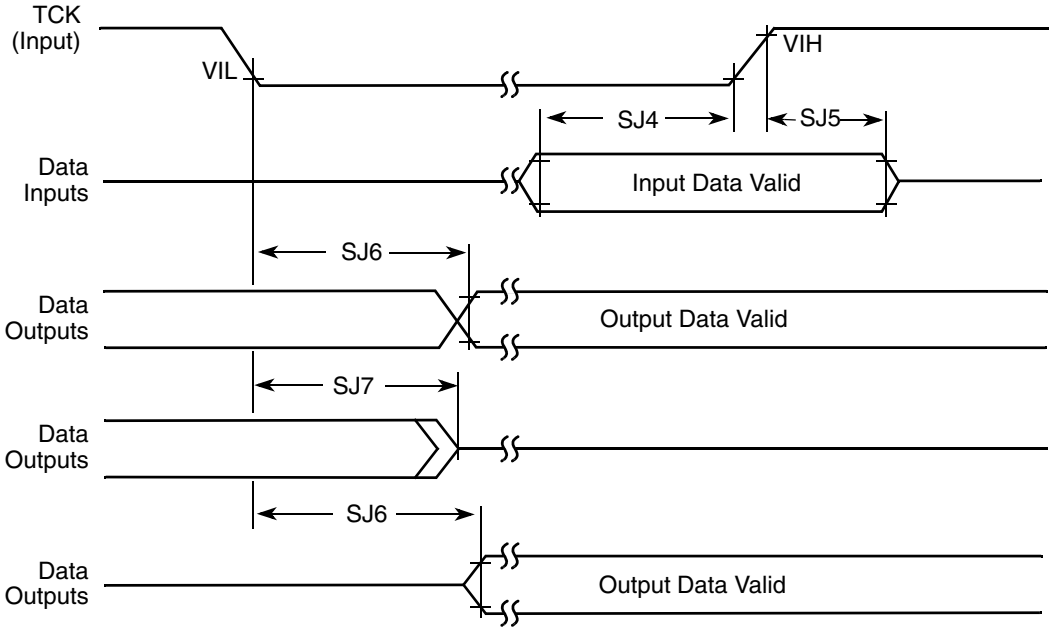

Figure 87. Boundary Scan (JTAG) Timing Diagram

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 98. i.MX35 Data Sheet Revision History (continued)

Revision Number	Date	Substantive Change(s)
1	12/2008	• Updated Section 4.3.1, “Powering Up.” • Section 4.7, “Module-Level AC Electrical Specifications”: Updated NFC, SDRAM and mDDR SDRAM timing. Inserted DDR2 SDRAM timing.
0	10/2008	Initial public release