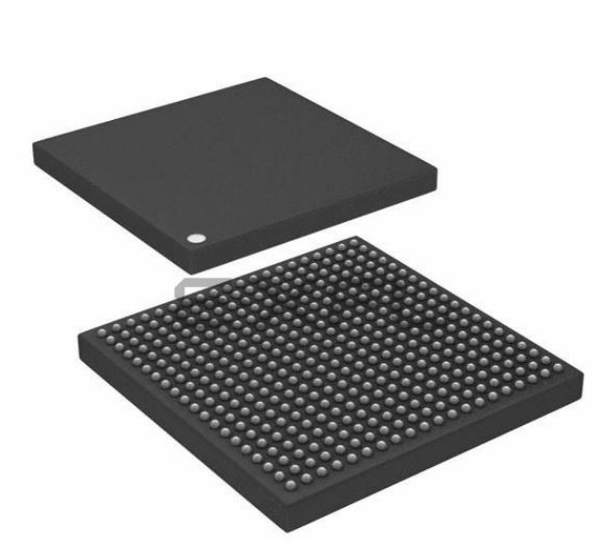

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, VFP
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, KPP, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Secure Fusebox, Secure JTAG, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx357djq5cr2

- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

Table 1. Ordering Information

Description	Part Number	Silicon Revision	Package[1]	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX353	MCIMX353CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX353	MCIMX353DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX357	MCIMX357CVM5B	2.0	5284	532 MHz	–40 to 85	Table 94	Table 96
i.MX357	MCIMX357DVM5B	2.0	5284	532 MHz	–20 to 70	Table 94	Table 96
i.MX353	MCIMX353CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX353	MCIMX353DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97
i.MX357	MCIMX357CJQ5C	2.1	5284	532MHz	-40 to 85	Table 95	Table 97
i.MX357	MCIMX357DJQ5C	2.1	5284	532MHz	-20 to 70	Table 95	Table 97

[1] Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

Table 2 shows the functional differences between the different parts in the i.MX35 family.

Table 2. Functional Differences in the i.MX35 Parts

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
I2C (3)	Yes	Yes	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes	Yes	Yes
ESAI	Yes	Yes	Yes	Yes	Yes
SPDIF I/O	Yes	Yes	Yes	Yes	Yes
USB HS Host	Yes	Yes	Yes	Yes	Yes
USB OTG	Yes	Yes	Yes	Yes	Yes
FlexCAN (2)	Yes	Yes	Yes	Yes	Yes
MLB	Yes	Yes	Yes	Yes	Yes

Table 2. Functional Differences in the i.MX35 Parts (continued)

Module	MCIMX351	MCIMX353	MCIMX355	MCIMX356	MCIMX357
Ethernet	Yes	Yes	Yes	Yes	Yes
1-Wire	Yes	Yes	Yes	Yes	Yes
KPP	Yes	Yes	Yes	Yes	Yes
SDIO/MMC (2)	Yes	Yes	Yes	Yes	Yes
SDIO/Memory Stick	Yes	Yes	Yes	Yes	Yes
External Memory Controller (EMC)	Yes	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	Yes	Yes
PATA	—	Yes	Yes	Yes	Yes
CE-ATA	—	Yes	Yes	Yes	Yes
Image Processing Unit (IPU) (inversion and rotation, pre- and post-processing, camera interface, blending, display controller)	—	Yes	Yes	Yes	Yes
Open VG graphics acceleration (GPU)	—	Yes	—	Yes	Yes

Table 4. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain[1]	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. **Note:** CE-ATA is not available for the MCIMX351.
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. **Note:** Not available for the MCIMX351.

Table 14 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 14. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = –1 mA Ioh = specified drive	NVCC – 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–2.0 –4.0 –8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	–4.0 –6.0 –8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode	VIL	—	–0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—		V
	Schmitt trigger VT–	VT–	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
	External resistance to pull keeper up when enabled	Rkpu	Ipu > 620 μA @ min Vddio = 3.0 V	—	—	4.8	kΩ
	External resistance to pull keeper down when enabled	Rkpd	Ipu > 510 μA @min Vddio = 3.0 V	—	—	5.9	kΩ

Table 14. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DDR2	High-level output voltage	Voh	—	NVCC – 0.28	—	—	V
	Low-level output voltage	Vol	—		—	0.28	V
	Output min. source current	Ioh	—	–13.4	—	—	mA
	Output min. sink current	Iol	—	13.4	—	—	mA
	DC input logic high	VIH(dc)	—	NVCC ÷ 2 + 0.125	—	NVCC + 0.3	V
	DC input logic low	VIL(dc)	—	–0.3 V	—	NVCC ÷ 2 – 0.125	V
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	NVCC + 0.3	V
	DC differential input voltage	Vid(dc)	—	0.25	—	NVCC + 0.6	V
	Termination voltage	Vtt	—	NVCC ÷ 2 – 0.04	NVCC ÷ 2	NVCC ÷ 2 + 0.04	V
	Input current (no pull-up/down)	IIN	—	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	—	—	—	±1	μA
Mobile DDR	High-level output voltage	—	I_{OH} = –1mA I_{OH} = specified drive	NVCC – 0.08 0.8 × NVCC	—	—	V
	Low-level output voltage	—	I_{OL} = 1mA I_{OL} = specified drive	—	—	0.08 0.2 × NVCC	V
	High-level output current (Voh = 0.8 × NVCCV)	—	Standard drive High drive Max. drive	–3.6 –7.2 –10.8	—	—	mA
	Low-level output current (Vol = 0.2 × NVCCV)	—	Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA
	High-Level DC CMOS input voltage	VIH	—	0.7 × NVCC	—	NVCC + 0.3	V
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	0.2 × NVCC	V
	Differential receiver VTH+	VTH+	—	—	—	100	mV
	Differential receiver VTH–	VTH–	—	–100	—		mV
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc – NVCC	VI = NVCC or 0	—	—	±1	μA

Table 19. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode [NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

Table 20. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode [NVCC = 2.25 V–2.75 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

[2] The typical value of Vox(ac) is expected to be about 0.5 × NVCC and Vox(ac) is expected to track variation in NVCC. Vox(ac) indicates the voltage at which the differential output signal must cross. Cload = 25 pF.

Table 24. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 25. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

NOTE

Test conditions are: pin voltage 1.7 V–1.95 V, capacitance 15 pF for all pins (both DDR and non-DDR pins), drive strength is high (7.2 mA). “High” is defined as 80% of signal value and “low” is defined as 20% of signal value.

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value. tCH + tCL will not exceed 7.5 ns for 133 MHz. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

The timing parameters are similar to the ones used in SDRAM data sheets. Table 36 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

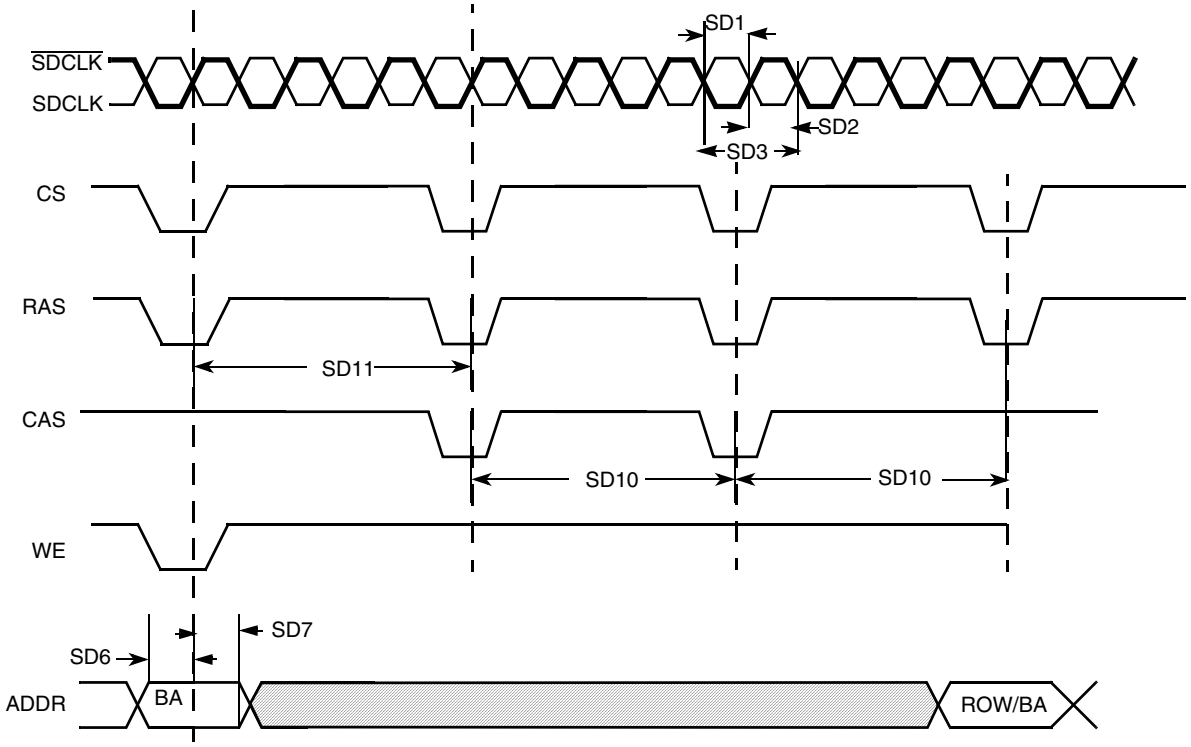

Figure 29. SDRAM Refresh Timing Diagram

Table 37. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 44 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

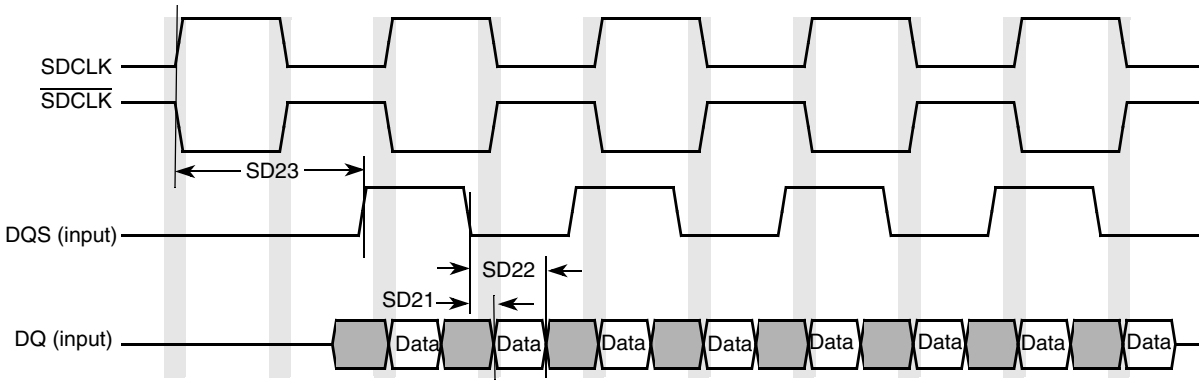

Figure 35. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 45. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, "high" is defined as 50% of signal value, and "low" is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. Table 45 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

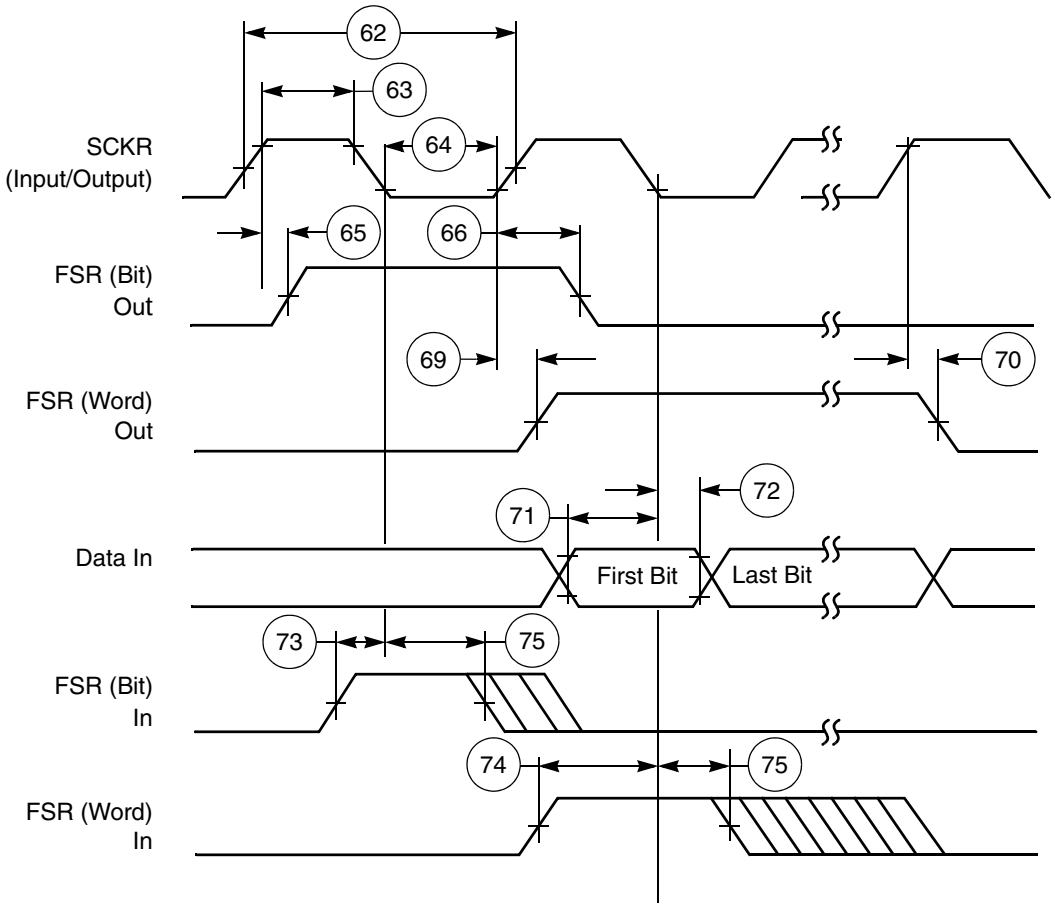

Figure 37. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 38 depicts the timing of eSDHCv2, and Table 47 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 47:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

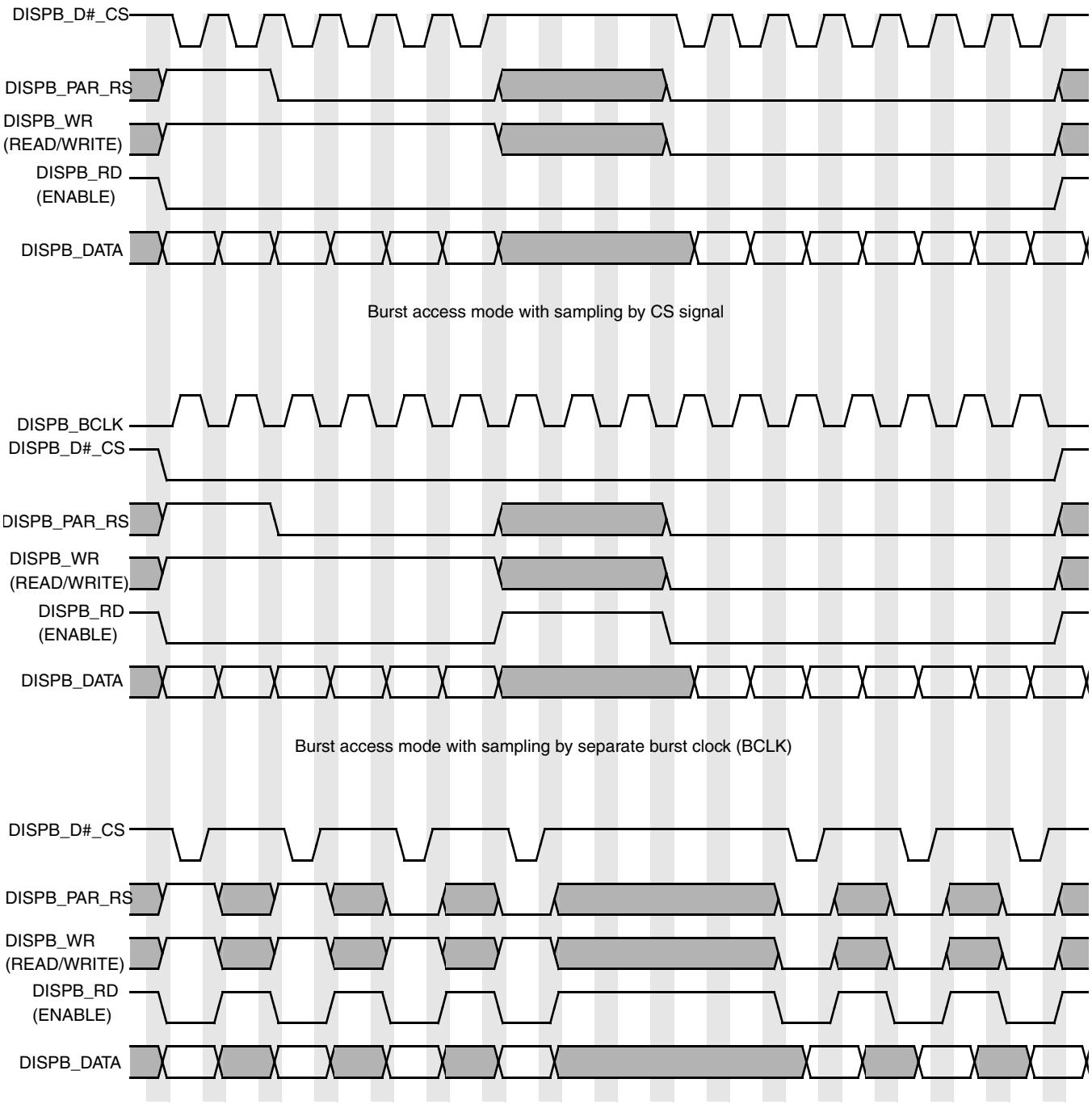

Figure 55. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

Table 58. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP36	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP37	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP39	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP41	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP42	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP43	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP44	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP45	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP46	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP47	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device-specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2, and DI_HSP_CLK_PER registers:

- DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD
- HSP_CLK_PERIOD
- DISP#_IF_CLK_DOWN_WR
- DISP#_IF_CLK_UP_WR
- DISP#_IF_CLK_DOWN_RD
- DISP#_IF_CLK_UP_RD
- DISP#_READ_EN

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 62 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux connects the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP*n*_CONF registers (*n* = 1, 2).

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 66 depicts timing of the serial interface. Table 59 lists the timing parameters at display access level.

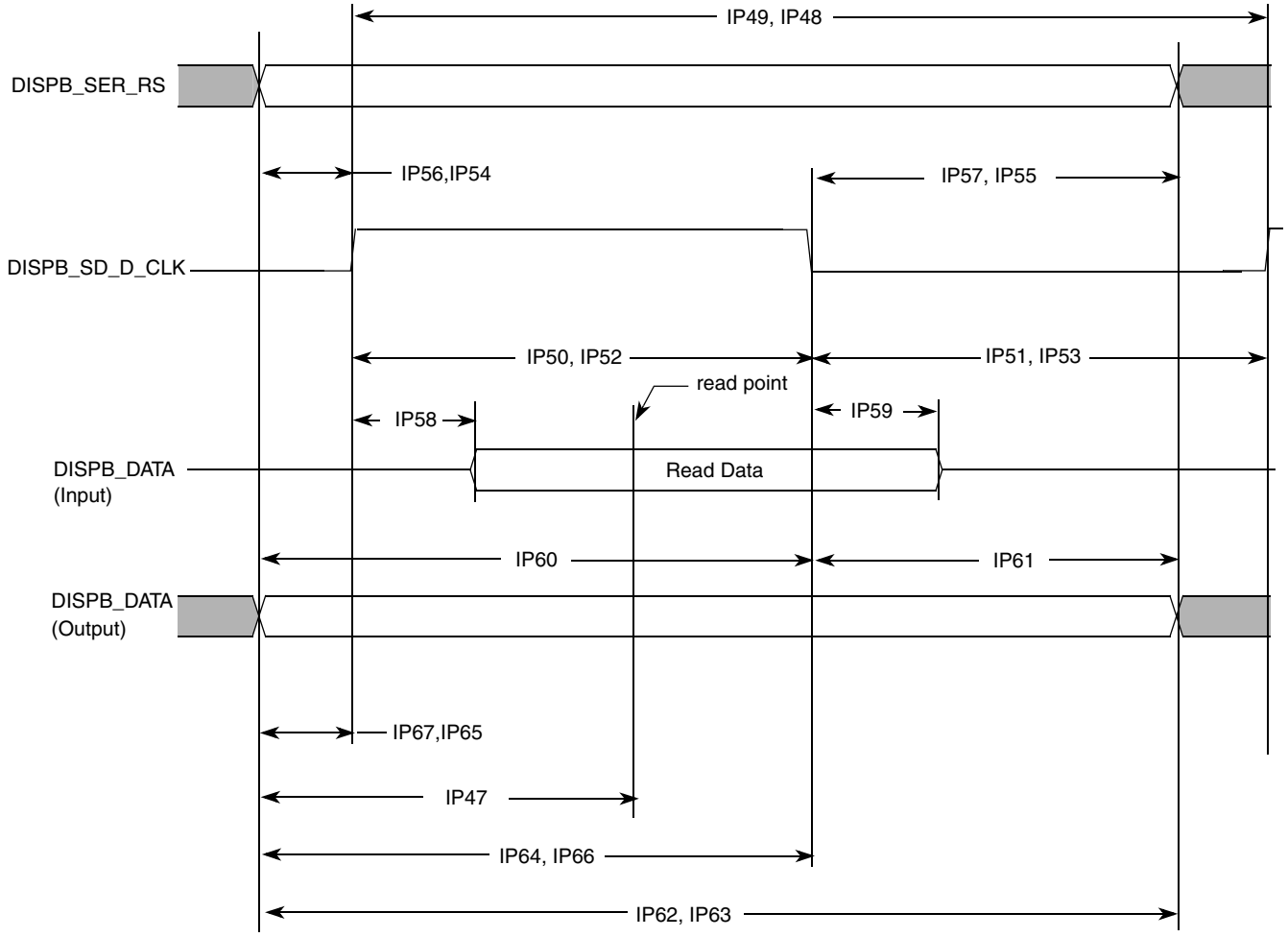

Figure 66. Asynchronous Serial Interface Timing Diagram

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr[2]	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw[3]	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr[4] – Tdicur[5]	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw[6] – Tdicuw[7]	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 59. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9] – Tlbd[10] – Tdicur – 1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

4.9.22.4 SSI Receiver Timing with External Clock

Figure 95 depicts the SSI receiver timing with external clock, and Table 81 lists the timing parameters.

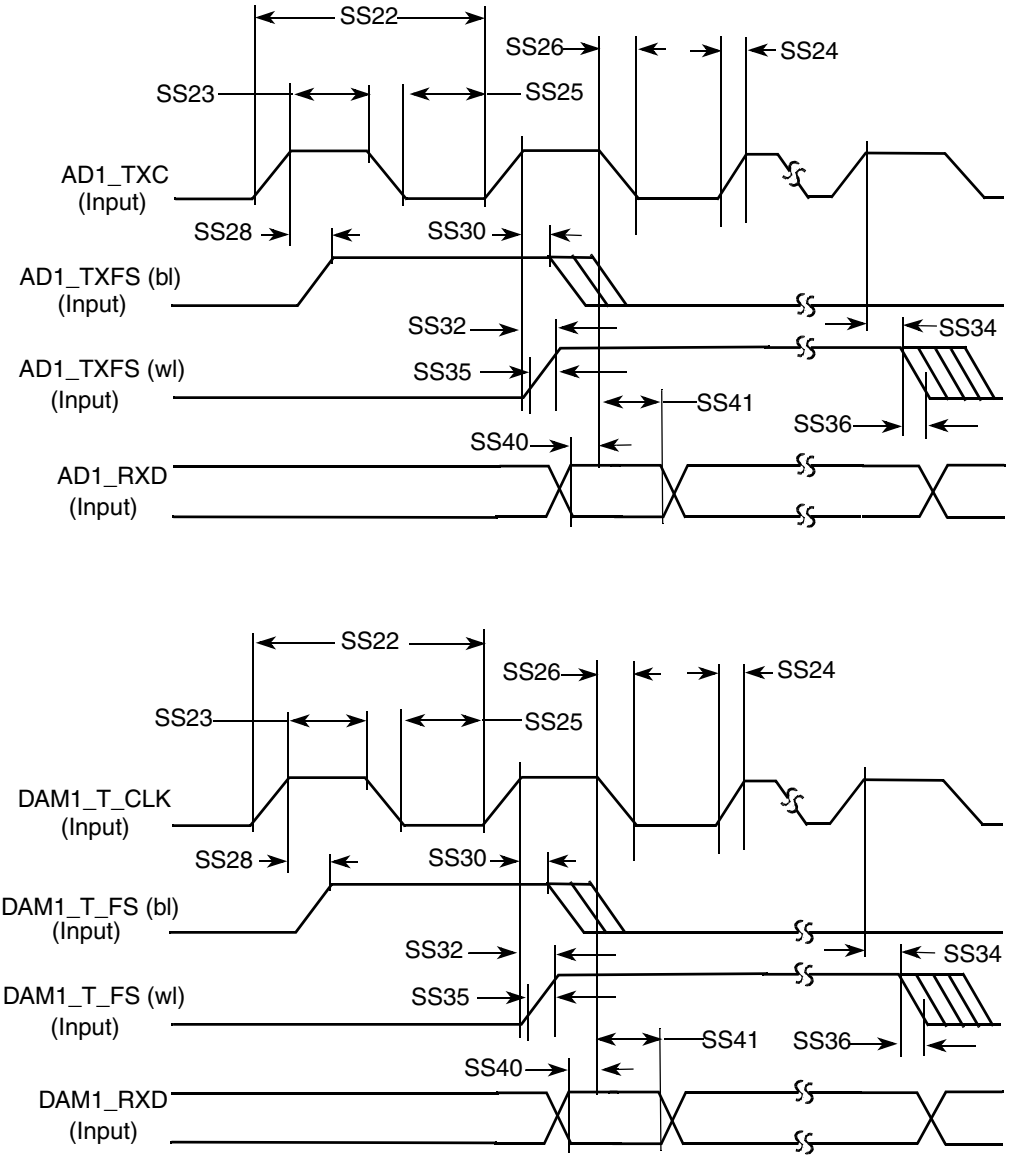

Figure 95. SSI Receiver with External Clock Timing Diagram

Table 81. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns

Table 95. Silicon Revision 2.1 Signal Ball Map Locations

Signal ID	Ball Location
A0	A5
A1	D7
A10	F15
A11	D5
A12	F6
A13	B3
A14	D14
A15	D15
A16	D13
A18	D12
SDQS1	E11
A19	D11
A2	E7
A21	D10
SDQS2	E10
A22	D9
SDQS3	E9
A24	D8
A25	E8
A3	C6
A4	D6
A5	B5
A6	C5
A7	A4
A8	B4
A9	A3
ATA_BUFF_EN[1]	T5
ATA_CS0	V7
ATA_CS1	T7
ATA_DA0	R4
ATA_DA1	V1
ATA_DA2	R5
ATA_DATA0	Y5
ATA_DATA1	W5
ATA_DATA10	V3
ATA_DATA11	Y2
ATA_DATA12	U3
ATA_DATA13	W2
ATA_DATA14	W1
ATA_DATA15	T4
ATA_DATA2	V5
ATA_DATA3	U5
ATA_DATA4	Y4
ATA_DATA5	W4
ATA_DATA6	V4

Signal ID	Ball Location
ATA_DATA7	Y3
ATA_DATA8	U4
ATA_DATA9	W3
ATA_DIOR	Y6
ATA_DIOW	W6
ATA_DMACK	V6
ATA_DMARQ	T3
ATA_INTRQ	V2
ATA_IORDY	U6
ATA_RESET_B	T6
SDQS0	E14
BOOT_MODE0	W10
BOOT_MODE1	U9
CAPTURE	V12
RAS	E16
CLK_MODE0	Y10
CLK_MODE1	T10
CLKO	V10
COMPARE	T12
CONTRAST	L16
CS0	F17
CS1	E19
CS2	B20
CS3	C19
CS4	E18
CS5	F19
CSI_D10	V16
CSI_D11	T15
CSI_D12	W16
CSI_D13	V15
CSI_D14	U14
CSI_D15	Y16
CSI_D8	U15
CSI_D9	W17
CSI_HSYNC	V14
CSI_MCLK	W15
CSI_PIXCLK	Y15
CSI_VSYNC	T14
CSPI1_MISO	V9
CSPI1_MOSI	W9
CSPI1_SCLK	W8
CSPI1_SPI_RDY	T8
CSPI1_SS0	Y8
CSPI1_SS1	U8
CTS1	R3

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
SD1_CLK	V18
SD1_CMD	Y19
SD1_DATA0	R14
SD1_DATA1	U16
SD1_DATA2	W18
SD1_DATA3	V17
SD10	A15
SD11	B15
A17	C13
SD13	B14
SD14	A14
SD12	B13
SD16	C12
SD17	C11
SD18	A12
SD19	B12
SD2	B18
SD2_CLK	W14
SD2_CMD	U13
SD2_DATA0	V13
SD2_DATA1	T13
SD2_DATA2	Y14
SD2_DATA3	U12
SD20	B11
SD21	A11
A20	C10
SD22	B10
SD24	A9
SD25	C9
SD26	B9
SD27	A8
SD28	B8
SD29	C8
SD3	C16
SD30	A7
SD31	B7
SD4	A18
SD5	C15
SD6	A17
SD7	B16
SD8	C14
SD9	A16
SDBA0	A6
SDBA1	B6
SDCKE0	D18
CAS	E17

Signal ID	Ball Location
SDCLK	E12
SDCLK_B	E13
SD0	B17
SD15	A13
SD23	A10
A23	C7
SDWE	G15
SJC_MOD	U17
SRXD4	L1
SRXD5	K4
STXD4	M2
STXD5	K1
STXFS4	L2
STXFS5	J6
TCK	R17
TDI	P15
TDO	R15
TEST_MODE	Y7
TMS	R16
TRSTB	T16
TTM_PIN	M16
TX0	G4
TX1	H1
TX2_RX3	H5
TX3_RX2	J2
TX4_RX1	H4
TX5_RX0	J3
TXD1	R6
TXD2	H2
USBOTG_OC	U7
USBOTG_PWR	W7
USBPHY1_DM	N19
USBPHY1_DP	P19
USBPHY1_RREF	R19
USBPHY1_UID	N18
USBPHY1_UPLLGND	N14
USBPHY1_UPLLVDD	N15
USBPHY1_UPLLVDD	P17
USBPHY1_VBUS	P18
USBPHY1_VDDA_BIAS	R20
USBPHY1_VSSA_BIAS	R18
USBPHY2_DM	Y17
USBPHY2_DP	Y18
VDD	M6
VDD	F7
VDD	J7

Table 95. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

[1] Not available for the MCIMX351.

Table 96. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	D0	A9	A7	A0	SDBA0	SD30	SD27	SD24	SDQS2	SD21	SD18	SDQS1	SD14	SD10	SD9	SD6	SD4	SD1	VSS	A
B	D5	D2	A13	A8	A5	SDBA1	SD31	SD28	SD26	SD23	SD20	SD19	SD15	SD13	SD11	SD7	SDQS0	SD2	DQM0	CS2	B
C	D8	D7	D4	MA10	A6	A3	SDQS3	SD29	SD25	SD22	SD17	SD16	SD12	SD8	SD5	SD3	SD0	DQM3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM2	DQM1	SDCKE0	ECB	LBA	D
E	NFCLE	D15	D12	D9	D3	D11	A2	A25	A23	A21	A18	SDCLK	SDCLK_B	BCLK	RAS	CAS	SDCKE1	CS4	CS1	OE	E
F	NFRE_B	NFALE	NFRB	NFWP_B	D13	A12	VDD	VDD	VDD	NVCC_EMI1	NVCC_EMI1	VDD	NVCC_EMI2	NVCC_EMI2	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS2	NFWE_B	NF_CE0	TX0	CTS2	NVCC_NFC	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD	NVCC_EMI3	SDWE	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD2	RXD2	TX4_RX1	TX2_RX3	NVCC_NFC	NVCC_NFC	NGND_EMI1	NVCC_EMI1	NGND_EMI1	VSS	VSS	VSS	NVCC_LCDC	VDD	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCKT	HCKT	STXFS5	VDD	VSS	VSS	NGND_EMI1	NGND_EMI2	NGND_EMI3	VSS	NVCC_LCDC	VDD	LD12	LD14	LD11	LD13	LD15	J
K	STXD5	HCKR	SCKR	SRXD5	FSR	NVCC_MISC	NVCC_MISC	NGND_MISC	NGND_NFC	VSS	NGND_LCDC	NGND_EMI3	VSS	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRXD4	STXFS4	I2C2_CLK	SCK4	SCK5	FEC_TDATA3	VDD	NVCC_MISC	VSS	NGND_ATA	NGND_CRM	NGND_LCDC	VSS	NVCC_LCDC	D3_FPSHIFT	CONTRAST	D3_CLS	D3_HSYNC	LD23	D3_DRDY	L
M	I2C2_DAT	STXD4	FEC_RDATA2	FEC_TDATA1	FEC_TDATA2	VDD	NGND_MISC	VSS	NGND_ATA	NGND_MLB	FUSE_VSS	PGND	NGND_JTAG	NVCC_LCDC	PHY1_VDDA	TTM_PIN	D3_REV	D3_SPL	D3_VSYNC	I2C1_CLK	M
N	FEC_RDATA3	FEC_RDATA1	FEC_RX_ER	FEC_TX_ERR	FEC_CRS	NVCC_ATA	VDD	VSS	VSS	NGND_CSI	MGND	NGND_SDIO	PVDD	USBPHY1_UPLLGND	USBPHY1_UPLLVDD	PHY1_VSSA	I2C1_DAT	USBPHY1_UID	USBPHY1_DM	PHY1_VDDA	N
P	FEC_MDIO	FEC_RDATA0	FEC_COL	FEC_TX_CLK	FEC_TDATA0	NVCC_ATA	NVCC_ATA	NVCC_ATA	NGND_ATA	VSS	MVDD	PHY2_VSS	FUSE_VDD	NVCC_SDIO	TDI	NVCC_JTAG	USBPHY1_UPLLVDD	USBPHY1_VBUS	USBPHY1_DP	PHY1_VSSA	P
R	FEC_MDC	FEC_RX_CLK	CTS1	ATA_DA0	ATA_DA2	TXD1	VDD	VDD	NVCC_CRM	NVCC_MLB	NVCC_CSI	VDD	PHY2_VDD	SD1_DATA0	TDO	TMS	TCK	USBPHY1_VSSA_BIAS	USBPHY1_RREF	USBPHY1_VDDA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMARQ	ATA_DATA15	ATA_BUFF_EN	ATA_RESET_B	ATA_CS1	CSPI1_SPI_RDY	VSTBY	CLK_MODE1	GPIO1_0	COMPARE	SD2_DATA1	CSI_VSYNC	CSI_D11	TRSTB	VSS	OSC24M_VSS	OSC24M_VDD	EXTAL24M	T
U	RTS1	RXD1	ATA_DATA12	ATA_DATA8	ATA_DATA3	ATA_IORDY	USBOTG_OC	CSPI1_SS1	BOOT_MODE1	RESET_IN_B	GPIO2_0	SD2_DATA3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA1	SJC_MOD	RTCK	OSC_AUDIO_VSS	XTAL24M	U