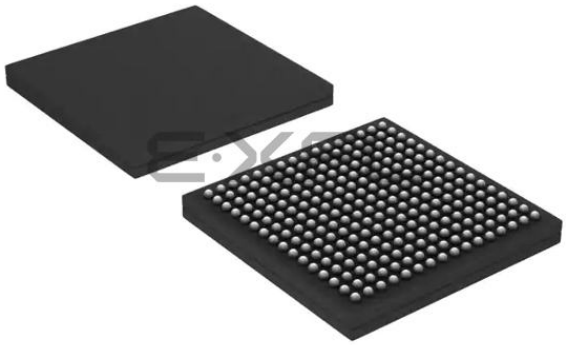

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	150
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5280cvf66j

byte, word, longword or 16-byte burst line transfers. These transfers are triggered by software, explicitly setting a DCR*n*[START] bit or the occurrence of a hardware event from one of the on-chip peripheral devices, such as a capture event or an output reference event in a DMA timer (DTIM*n*) for each channel. The DMA controller supports dual-address mode to on-chip devices.

1.1.17 Reset

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. The power management registers for the internal low-voltage detect (LVD) circuit are implemented in the reset module. There are seven sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase-locked loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detection (LVD) reset

External reset on the $\overline{\text{RSTO}}$ pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset, and LVD control and status bits for setup and use of LVD reset or interrupt.

1.2 MCF5282-Specific Features

1.2.1 Fast Ethernet Controller (FEC)

The MCF5282's integrated Fast Ethernet Controller (FEC) performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media.

NOTE

The MCF5214 and MCF5216 devices do not contain an FEC module.

1.2.2 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of real-time processing, reliable operation in a harsh EMI environment, cost-effectiveness, and required bandwidth. FlexCAN contains 16 message buffers.

1.2.3 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

execution until all previous operations, including all pending write operations, are complete. If any previous write terminates with an access error, it is guaranteed to be reported on the NOP instruction.

2.3.4.2 Address Error Exception

Any attempted execution transferring control to an odd instruction address (if bit 0 of the target address is set) results in an address error exception.

Any attempted use of a word-sized index register (Xn.w) or a scale factor of eight on an indexed effective addressing mode generates an address error, as does an attempted execution of a full-format indexed addressing mode, which is defined by bit 8 of extension word 1 being set.

If an address error occurs on a JSR instruction, the Version 2 ColdFire processor calculates the target address then the return address is pushed onto the stack. If an address error occurs on an RTS instruction, the Version 2 ColdFire processor overwrites the faulting return PC with the address error stack frame.

2.3.4.3 Illegal Instruction Exception

The ColdFire variable-length instruction set architecture supports three instruction sizes: 16, 32, or 48 bits. The first instruction word is known as the operation word (or opword), while the optional words are known as extension word 1 and extension word 2. The opword is further subdivided into three sections: the upper four bits segment the entire ISA into 16 instruction lines, the next 6 bits define the operation mode (opmode), and the low-order 6 bits define the effective address. See Figure 2-17. The opword line definition is shown in Table 2-8.

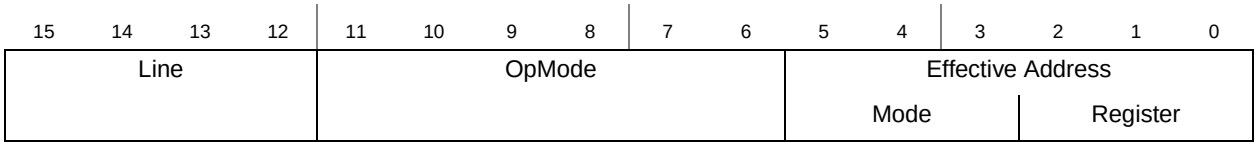


Figure 2-17. ColdFire Instruction Operation Word (Opword) Format

Table 2-8. ColdFire Opword Line Definition

Opword[Line]	Instruction Class
0x0	Bit manipulation, Arithmetic and Logical Immediate
0x1	Move Byte
0x2	Move Long
0x3	Move Word
0x4	Miscellaneous
0x5	Add (ADDQ) and Subtract Quick (SUBQ), Set according to Condition Codes (Scc)
0x6	PC-relative change-of-flow instructions Conditional (Bcc) and unconditional (BRA) branches, subroutine calls (BSR)
0x7	Move Quick (MOVEQ), Move with sign extension (MVS) and zero fill (MVZ)
0x8	Logical OR (OR)
0x9	Subtract (SUB), Subtract Extended (SUBX)

Table 10-7. IMRL*n* Field Descriptions

Bits	Name	Description
31–1	INT_MASK	Interrupt mask. Each bit corresponds to an interrupt source. The corresponding IMRL*n* bit determines whether an interrupt condition can generate an interrupt. The corresponding IPRL*n* bit reflects the state of the interrupt signal even if the corresponding IMRL*n* bit is set. 0 The corresponding interrupt source is not masked 1 The corresponding interrupt source is masked
0	MASKALL	Mask all interrupts. Setting this bit will force the other 63 bits of the IMRH*n* and IMRL*n* to ones, disabling all interrupt sources, and providing a global mask-all capability.

NOTE

If an interrupt source is being masked in the interrupt controller mask register (IMR) or a module's interrupt mask register while the interrupt mask in the status register (SR[I]) is set to a value lower than the interrupt's level, a spurious interrupt may occur. This is because by the time the status register acknowledges this interrupt, the interrupt has been masked. A spurious interrupt is generated because the CPU cannot determine the interrupt source. To avoid this situation for interrupts sources with levels 1-6, first write a higher level interrupt mask to the status register, before setting the mask in the IMR or the module's interrupt mask register. After the mask is set, return the interrupt mask in the status register to its previous value. Since level seven interrupts cannot be disabled in the status register prior to masking, use of the IMR or module interrupt mask registers to disable level seven interrupts is not recommended.

10.3.3 Interrupt Force Registers (INTFRCH*n*, INTFRCL*n*)

The INTFRCH*n* and INTFRCL*n* registers are each 32 bits in size and provide a mechanism to allow software generation of interrupts for each possible source for functional or debug purposes. The system design may reserve one or more sources to allow software to self-schedule interrupts by forcing one or more of these bits (1 = force request, 0 = negate request) in the appropriate INTFRC*n* register. The assertion of an interrupt request via the INTFRC*n* register is not affected by the interrupt mask register. The INTFRC*n* register is cleared by reset.

Table 15-23. Processor to SDRAM Interface (32-Bit Port, 12-Column Address Lines)

Processor Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A21	A23
Row	15	14	13	12	11	10	9	17	19	21	23
Column	2	3	4	5	6	7	8	16	18	20	22
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

15.2.3.2 SDRAM Byte Strobe Connections

Figure 15-5 shows SDRAM connections for port sizes of 32, 16, or 8 bits.

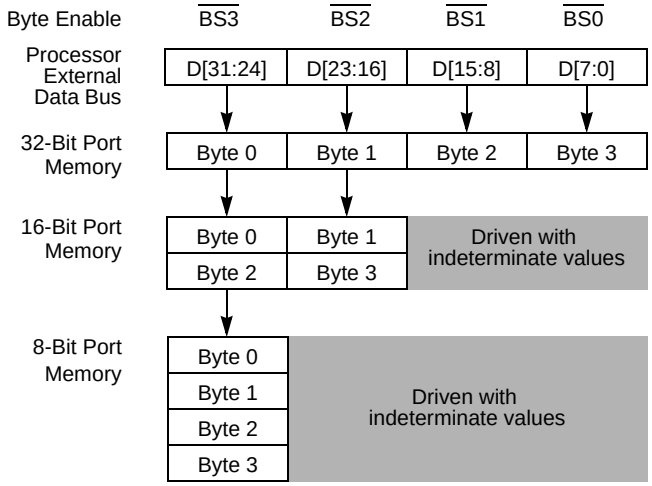


Figure 15-5. Connections for External Memory Port Sizes

15.2.3.3 Interfacing Example

The tables in the previous section can be used to configure the interface in the following example. To interface one 2M x 32-bit x 4 bank SDRAM component (8 columns), use the connections shown in Table 15-24.

Table 15-24. SDRAM Hardware Connections

SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10 = CMD	BA0	BA1
Processor Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22

15.2.3.4 Burst Page Mode

SDRAM can efficiently provide data when an SDRAM page is opened. As soon as $\overline{\text{SCAS}}$ is issued, the SDRAM accepts a new address and asserts $\overline{\text{SCAS}}$ every CLKOUT for as long as accesses occur in that page. In burst page mode, there are multiple read or write operations for every ACTV command in the SDRAM if the requested transfer size exceeds the port size of the associated SDRAM. The primary cycle of the transfer generates the ACTV and READ or WRITE commands; secondary cycles generate only READ or WRITE commands. As soon as the transfer completes, the PALL command is generated to prepare for the next access.

Table 17-35. MII Mode (continued)

Signal Description	EMAC pin
Collision	FEC_COL
Carrier Sense	FEC_CRS
Receive Clock	FEC_RXCLK
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[3:0]
Receive Error	FEC_RXER
Management Data Clock	FEC_MDC
Management Data Input/Output	FEC_MDIO

The 7-wire serial mode interface (RCR[MII_MODE] cleared) is generally referred to as AMD mode. Table 17-36 shows the 7-wire mode connections to the external transceiver.

Table 17-36. 7-Wire Mode Configuration

Signal description	EMAC Pin
Transmit Clock	FEC_TXCLK
Transmit Enable	FEC_TXEN
Transmit Data	FEC_TXD[0]
Collision	FEC_COL
Receive Clock	FEC_RXCLK
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[0]

17.5.7 FEC Frame Transmission

The Ethernet transmitter is designed to work with almost no intervention from software. After ECR[ETHER_EN] is set and data appears in the transmit FIFO, the Ethernet MAC can transmit onto the network. The Ethernet controller transmits bytes least significant bit (lsb) first.

When the transmit FIFO fills to the watermark (defined by TFWR), MAC transmit logic asserts FEC_TXEN and starts transmitting the preamble (PA) sequence, the start frame delimiter (SFD), and then the frame information from the FIFO. However, the controller defers the transmission if the network is busy (FEC_CRS is asserted). Before transmitting, the controller waits for carrier sense to become inactive, then determines if carrier sense stays inactive for 60 bit times. If so, transmission begins after waiting an additional 36 bit times (96 bit times after carrier sense originally became inactive). See Section 17.5.15.1, “Transmission Errors,” for more details.

The PORTT*n* data direction register controls the data direction of an input capture pin. External pin conditions trigger input captures on input capture pins configured as inputs.

To configure a pin for input capture:

1. Clear the pin's IOS bit in GPTIOS.
2. Clear the pin's DDR bit in PORTT*n*DDR.
3. Write to GPTCTL2 to select the input edge to detect.

PORTT*n*DDR does not affect the data direction of an output compare pin. The output compare function overrides the data direction register but does not affect the state of the data direction register.

To configure a pin for output compare:

1. Set the pin's IOS bit in GPTIOS.
2. Write the output compare value to GPTC*n*.
3. Clear the pin's DDR bit in PORTT*n*DDR.
4. Write to the OM*n*/OL*n* bits in GPTCTL1 to select the output action.

Table 20-23 shows how various timer settings affect pin functionality.

Table 20-23. GPT Settings and Pin Functions

GPTEN	DDR[1]	GPTIOS	EDGx [B:A]	OMx/OLx[2]	OC3Mx[3]	Pin Data Dir.	Pin Driven by	Pin Function	Comments
0	0	X[4]	X	X	X	In	Ext.	Digital input	GPT disabled by GPTEN = 0
0	1	X	X	X	X	Out	Data reg.	Digital output	GPT disabled by GPTEN = 0
1	0	0 (IC)	0 (IC disabled)	X	0	In	Ext.	Digital input	Input capture disabled by EDG*n* setting
1	1	0	0	X	0	Out	Data reg.	Digital output	Input capture disabled by EDG*n* setting
1	0	0	<> 0	X	0	In	Ext.	IC and digital input	Normal settings for input capture
1	1	0	<> 0	X	0	Out	Data reg.	Digital output	Input capture of data driven to output pin by CPU
1	0	0	<> 0	X	1	In	Ext.	IC and digital input	OC3M setting has no effect because IOS = 0
1	1	0	<> 0	X	1	Out	Data reg.	Digital output	OC3M setting has no effect because IOS = 0; input capture of data driven to output pin by CPU
1	0	1 (OC)	X(3)	0[5]	0	In	Ext.	Digital input	Output compare takes place but does not affect the pin because of the OM*n*/OL*n* setting
1	1	1	X	0	0	Out	Data reg.	Digital output	Output compare takes place but does not affect the pin because of the OM*n*/OL*n* setting
1	0	1	X	<> 0	0	Out	OC action	Output compare	Pin readable only if DDR = 0(5)
1	1	1	X	<> 0	0	Out	OC action	Output compare	Pin driven by OC action(5)

Table 23-8. UIPCR*n* Field Descriptions

Field	Description
7–5	Reserved
4 COS	Change of state (high-to-low or low-to-high transition). 0 No change-of-state since the CPU last read UIPCR*n*. Reading UIPCR*n* clears UISR*n*[COS]. 1 A change-of-state longer than 25–50 μs occurred on the $\overline{\text{UCTS}}$*n* input. UACR*n* can be programmed to generate an interrupt to the CPU when a change of state is detected.
3–1	Reserved
0 CTS	Current state of clear-to-send. Starting two serial clock periods after reset, CTS reflects the state of $\overline{\text{UCTS}}$*n*. If $\overline{\text{UCTS}}$*n* is detected asserted at that time, COS is set, which initiates an interrupt if UACR*n*[IEC] is enabled. 0 The current state of the $\overline{\text{UCTS}}$*n* input is asserted. 1 The current state of the $\overline{\text{UCTS}}$*n* input is deasserted.

23.3.9 UART Auxiliary Control Register (UACR*n*)

The UACRs control the input enable.

IPSBAR 0x00_0210 (UACR0) Access: User write-only
Offset: 0x00_0250 (UACR1)
0x00_0290 (UACR2)

	7	6	5	4	3	2	1	0
R								
W	0	0	0	0	0	0	0	IEC
Reset:	0	0	0	0	0	0	0	0

Figure 23-11. UART Auxiliary Control Registers (UACR*n*)

Table 23-9. UACR*n* Field Descriptions

Field	Description
7–1	Reserved, must be cleared.
0 IEC	Input enable control. 0 Setting the corresponding UIPCR*n* bit has no effect on UISR*n*[COS]. 1 UISR*n*[COS] is set and an interrupt is generated when the UIPCR*n*[COS] is set by an external transition on the $\overline{\text{UCTS}}$*n* input (if UIMR*n*[COS] = 1).

23.3.10 UART Interrupt Status/Mask Registers (UISR*n*/UIMR*n*)

The UISRs provide status for all potential interrupt sources. UISR*n* contents are masked by UIMR*n*. If corresponding UISR*n* and UIMR*n* bits are set, internal interrupt output is asserted. If a UIMR*n* bit is cleared, state of the corresponding UISR*n* bit has no effect on the output.

The UISR*n* and UIMR*n* registers share the same space in memory. Reading this register provides the user with interrupt status, while writing controls the mask bits.

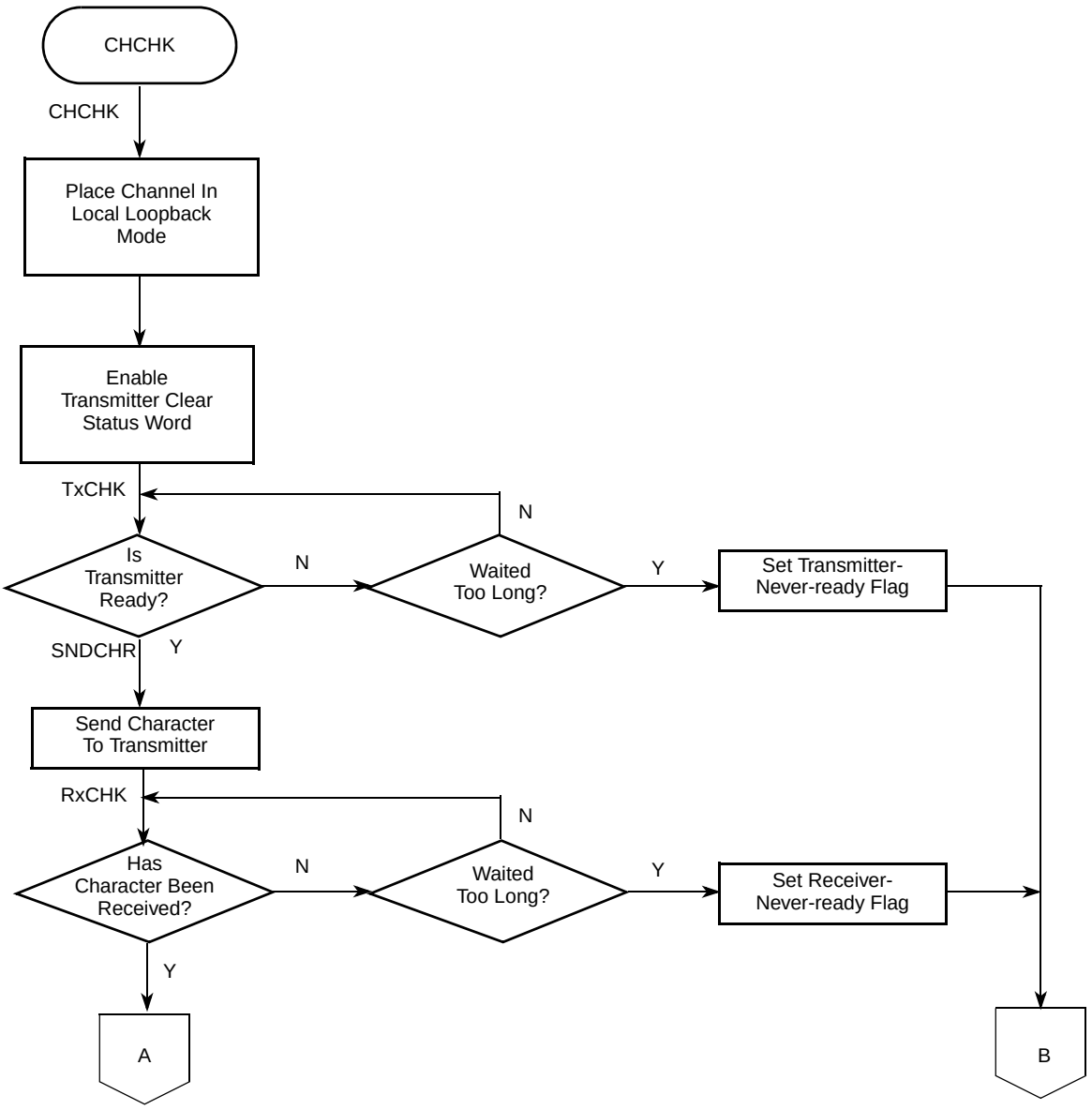
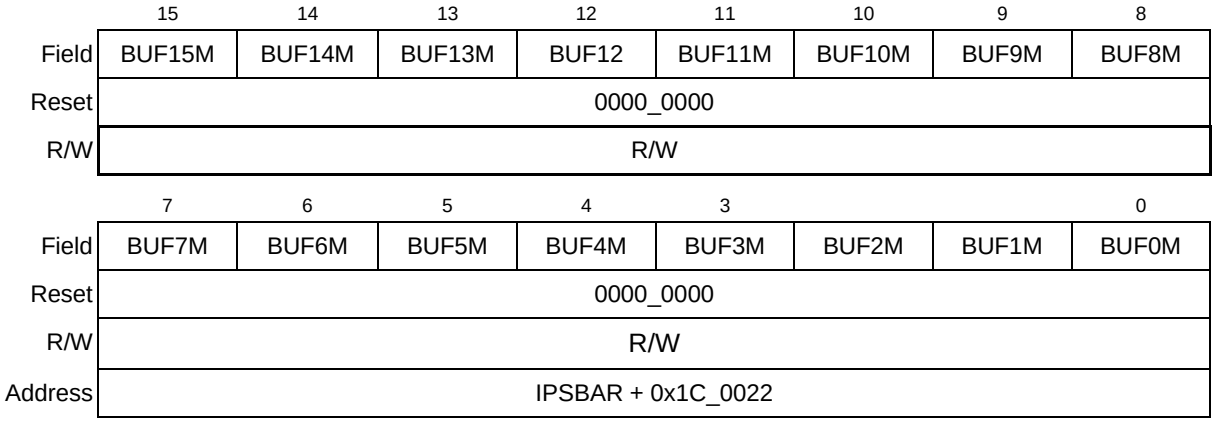


Figure 23-25. UART Mode Programming Flowchart (Sheet 2 of 5)

The interrupt mask register contains two 8-bit fields: bits 15-8 (IMASK_H) and bits 7-0 (IMASK_L). The register can be accessed by the master as a 16-bit register, or each byte can be accessed individually using an 8-bit (byte) access cycle.



	15	14	13	12	11	10	9	8
Field	BUF15M	BUF14M	BUF13M	BUF12	BUF11M	BUF10M	BUF9M	BUF8M
Reset	0000_0000							
R/W	R/W							

	7	6	5	4	3			0
Field	BUF7M	BUF6M	BUF5M	BUF4M	BUF3M	BUF2M	BUF1M	BUF0M
Reset	0000_0000							
R/W	R/W							
Address	IPSBAR + 0x1C_0022							

Figure 25-14. Interrupt Mask Register (IMASK)

Table 25-18 describes the IMASK fields.

Table 25-18. IMASK Field Descriptions

Bits	Name	Description
15–0	BUF*n*M	IMASK contains one interrupt mask bit per buffer. It allows the CPU to designate which buffers will generate interrupts after successful transmission/reception. 0 The interrupt for the corresponding buffer is disabled. 1 The interrupt for the corresponding buffer is enabled.

25.5.10 Interrupt Flag Register (IFLAG)

IFLAG contains one interrupt flag bit per buffer. Each successful transmission/reception sets the corresponding IFLAG bit and, if the corresponding IMASK bit is set, will generate an interrupt.

This register contains two 8-bit fields: bits 15-8 (IFLAG_H) and bits 7-0 (IFLAG_L). The register can be accessed by the master as a 16-bit register, or each byte can be accessed individually using an 8-bit (byte) access cycle.

26.3.2.6 Port E Pin Assignment Register (PEPAR)

The PEPAR controls the pin function of port E.

The PEPAR register is read/write.

	15	14	13	12	11	10	9	8
Field	—	PEPA7	—	PEPA6	—	PEPA5	—	PEPA4
Reset	0	See Note 1	0	See Note 1	0	See Note 1	0	See Note 1
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

	7	6	5	4	3	2	1	0
Field	—	PEPA3	—	PEPA2	PEPA1		PEPA0	
Reset	0	See Note 1	0	See Note 1	See Note 1		See Note 1	
R/W:	R	R/W	R	R/W	R/W		R/W	
Address	IPSBAR + 0x10_0052							

Figure 26-20. Port E Pin Assignment Register (PEPAR)

[1] Reset state determined during reset configuration as shown in Table 26-10.

Table 26-9. PEPAR Field Descriptions

Bits	Name	Description
14	PEPA7	Port E pin assignment 7. This bit configures the port E7 pin for its primary function ($\overline{OE}$) or digital I/O. 1 Port E7 pin configured for primary function ($\overline{OE}$) 0 Port E7 pin configured for digital I/O
12	PEPA6	Port E pin assignment 6. This bit configures the port E6 pin for its primary function ($\overline{TA}$) or digital I/O. 1 Port E6 pin configured for primary function ($\overline{TA}$) 0 Port E6 pin configured for digital I/O
10	PEPA5	Port E pin assignment 5. This bit configures the port E5 pin for its primary function ($\overline{TEA}$) or digital I/O. 1 Port E5 pin configured for primary function ($\overline{TEA}$) 0 Port E5 pin configured for digital I/O
8	PEPA4	Port E pin assignment 4. This bit configures the port E4 pin for its primary function (R/$\overline{W}$) or digital I/O. 1 Port E4 pin configured for primary function (R/$\overline{W}$) 0 Port E4 pin configured for digital I/O

26.3.2.7 Port F Pin Assignment Register (PFPAR)

The PFPAR controls the pin function of port F[7:5].

	7	6	5	4 … 0
Field	PFPA7	PFPA6	PFPA5	—
Reset	See Note 1			0_0000
R/W:	R/W			R
Address	IPSBAR + 0x10_0051			

Figure 26-21. Port F Pin Assignment Register (PFPAR)

[1] Reset state determined during reset configuration. PFPA*n* = 1 in master mode and 0 in all other modes.

Table 26-11. PFPAR Field Descriptions

Bits	Name	Description
7	PFPA7	Port F pin assignment 1. The PFPA7 bit configures the port F7 pin for its primary function (A23), alternate function ($\overline{CS6}$), or digital I/O. 1 Port F7 pin configured for primary function (A23) or alternate function ($\overline{CS6}$), depending on the chip configuration. 0 Port F7 pin configured for digital I/O Refer to Chapter 27, “Chip Configuration Module (CCM)” for more information on reset configuration.
6	PFPA6	Port F pin assignment 6. The PFPA6 bit configures the port F6 pin for its primary function (A22), alternate function ($\overline{CS5}$), or digital I/O. 1 Port F6 pin configured for primary function (A22) or alternate function ($\overline{CS5}$), depending on the chip configuration. 0 Port F6 pin configured for digital I/O Refer to Chapter 27, “Chip Configuration Module (CCM)” for more information on reset configuration.
5	PFPA5	Port F pin assignment 5. The PFPAR bit configures the port F5 pin for its primary function (A21), alternate function ($\overline{CS4}$), or digital I/O. 1 Port F5 pin configured for primary function (A21) or alternate function ($\overline{CS4}$), depending on the chip configuration. 0 Port F5 pin configured for digital I/O Refer to Chapter 27, “Chip Configuration Module (CCM)” for more information on reset configuration.
4–0	—	Reserved, should be cleared.

28.4.1.1 Port QA Analog Input Signals

When used as analog inputs, the four port QA signals are referred to as AN[56:55, 53:52].

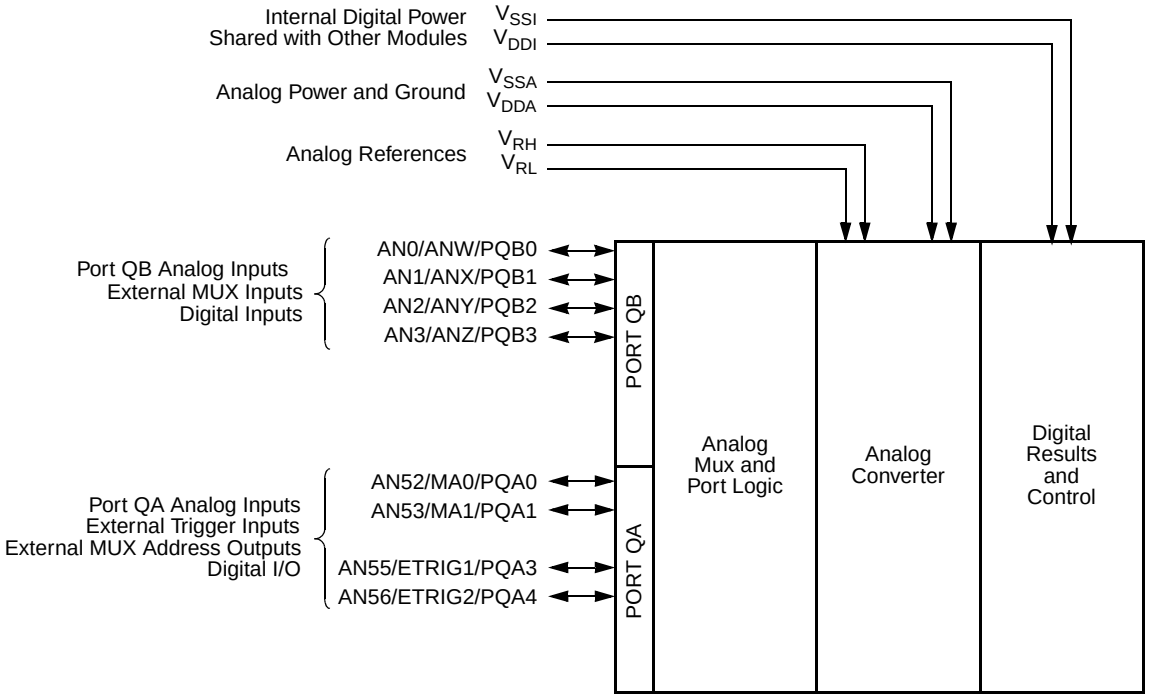


Figure 28-2. QADC Input and Output Signals

28.4.1.2 Port QA Digital Input/Output Signals

Port QA signals are referred to as PQA[4:3, 1:0] when used as a bidirectional 4-bit digital input/output port. These four signals may be used for general-purpose digital input or digital output.

Port QA signals are connected to a digital input synchronizer during reads and may be used as general-purpose digital inputs when the applied voltages meet high-voltage input (V_{IH}) and low-voltage input (V_{IL}) requirements.

Each port QA signal is configured as an input or output by programming the port data direction register (DDRQA). The digital input signal states are read from the port QA data register (PORTQA) when DDRQA specifies that the signals are inputs. The digital data in PORTQA is driven onto the port QA signals when the corresponding bits in DDRQA specify output. See Section 28.6.4, “Port QA and QB Data Direction Register (DDRQA & DDRQB).

28.4.2 Port QB Signal Functions

The four port QB signals can be used as analog inputs or as a 4-bit digital I/O port.

28.4.2.1 Port QB Analog Input Signals

When used as analog inputs, the four port QB signals are referred to as AN[3:0].

	7	6	5	4	3	2	1	0
Field	QS7	QS6	CWP5	CWP4	CWP3	CWP2	CWP1	CWP0
Reset	0000_0000							
R/W:	R							
Address	IPSBAR + 0x19_0010, 0x19_0011							

Figure 28-11. QADC Status Register 0 (QASR0)

Table 28-10. QASR0 Field Descriptions

Bit(s)	Name	Description
15, 13	CF*n*	Queue completion flag. Indicates that a queue scan has been completed. CF[1:2] is set by the QADC when the input channel sample requested by the last CCW in the queue is converted, and the result is stored in the result table. When CF*n* is set and queue completion interrupts are enabled (QACR*n*[CIE*n*] = 1), the QADC requests an interrupt. The interrupt request is cleared when a 0 is written to the CF1 bit after it has been read as a 1. Once set, CF1 can be cleared only by a reset or by writing a 0 to it. CF[1:2] is updated by the QADC regardless of whether the corresponding interrupt is enabled. This allows polled recognition of the queue scan completion.
14, 12	PF*n*	Queue pause flag. Indicates that a queue scan has reached a pause. PF[1:2] is set by the QADC when the current queue 1 CCW has the pause bit set, the selected input channel has been converted, and the result has been stored in the result table. When PF*n* is set and interrupts are enabled (QACR*n*[PIE*n*] = 1), the QADC requests an interrupt. The interrupt request is cleared when a 0 is written to PF*n*, after it has been read as a 1. Once set, PF*n* can be cleared only by reset or by writing a 0 to it. PF1: 1 Queue 1 has reached a pause or gate closed before end-of-queue in gated mode. 0 Queue 1 has not reached a pause or gate has not closed before end-of-queue in gated mode. PF2: 1 Queue 2 has reached a pause. 0 Queue 2 has not reached a pause. See Table 28-11 for a summary of CCW pause bit response in all scan modes.
11–10	TOR*n*	Queue trigger overrun flag. Indicates that an unexpected trigger event has occurred for queue 1. TOR[1:2] can be set only while the queue is in the active state. Once set, TOR[1:2] is cleared only by a reset or by writing a 0 to it. 1 At least one unexpected queue 1 trigger event has occurred or queue 1 reaches an end-of-queue condition for the second time in externally gated continuous scan. 0 No unexpected queue 1 trigger events have occurred.

Table 28-15. Input Sample Times

IST[1:0]	Input Sample Times
00	Input sample time = QCLK period × 2
01	Input sample time = QCLK period × 4
10	Input sample time = QCLK period × 8
11	Input sample time = QCLK period × 16

Table 28-16. Non-Multiplexed Channel Assignments and Signal Designations

Non-Multiplexed Input Signals				Channel Number[1] in CCW CHAN Field	
Port Signal Name	Analog Signal Name	Other Functions	Signal Type	Binary	Decimal
PQB0 PQB1 PQB2 PQB3	AN0 AN1 AN2 AN3	— — — —	Input Input Input Input	000000 000001 000010 000011	0 1 2 3
PQA0 PQA1	AN52 AN53	— —	Input/Output Input/Output	110100 110101	52 53
PQA3 PQA4	AN55 AN56	ETRIG1 ETRIG2	Input/Output Input/Output	110111 111000	55 56
V_{RL} V_{RH} —	Low reference High reference —	— — $(V_{RH}–V_{RL})/2$	Input Input —	111100 111101 111110	60 61 62
—	—	End-of-Queue Code	—	111111	63

1 All channels not listed are reserved or unimplemented and return undefined results.

Table 28-17. Multiplexed Channel Assignments and Signal Designations

Multiplexed Input Signals				Channel Number[1] in CCW CHAN Field	
Port Signal Name	Analog Signal Name	Other Functions	Signal Type	Binary	Decimal
PQB0 PQB1 PQB2 PQB3	ANW ANX ANY ANZ	— — — —	Input Input Input Input	000XX0 000XX1 010XX0 010XX1	0, 2, 4, 6 1, 3, 5, 7 16, 18, 20, 22 17, 19, 21, 23
PQA0 PQA1	— —	MA0 MA1	Output Output	—	52 53
PQA3 PQA4	AN55 AN56	ETRIG1 ETRIG2	Input/Output Input/Output	110111 111000	55 56
V_{RL} V_{RH} —	Low Reference High Reference —	— — $(V_{RH}–V_{RL})/2$	Input Input —	111100 111101 111110	60 61 62
—	—	End-of-Queue Code	—	111111	63

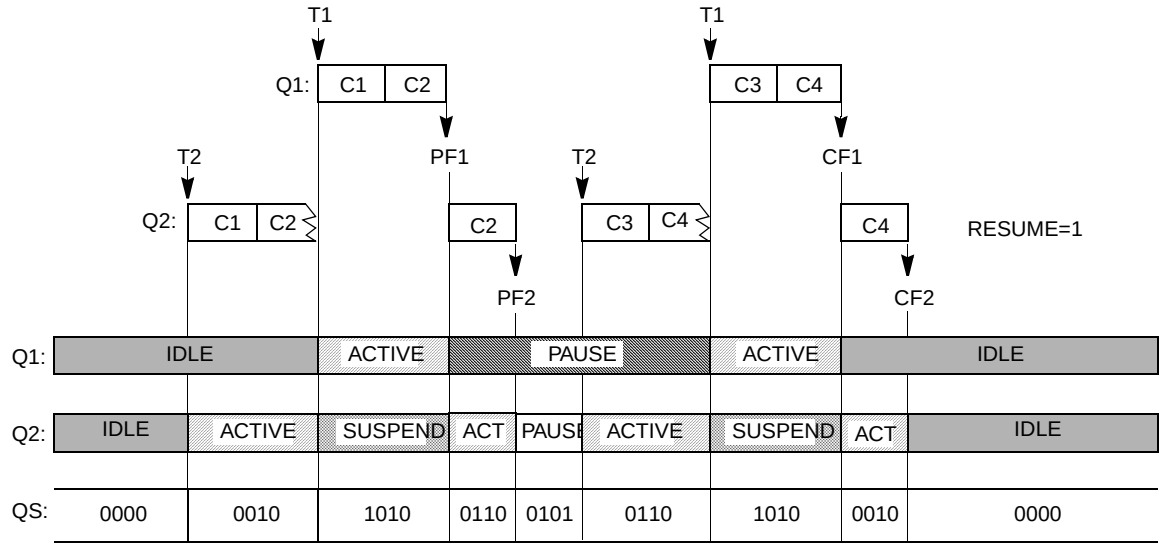


Figure 28-31. CCW Priority Situation 9

Situations S10 and S11 (Figure 28-32 and Figure 28-33) show that when an additional trigger event is detected for queue 2 while the queue is suspended, the trigger overrun error bit is set, the same as if queue 2 were being executed when a new trigger event occurs. Trigger overrun on queue 2 thus allows the user to know that queue 1 is taking up so much QADC time that queue 2 trigger events are being lost.

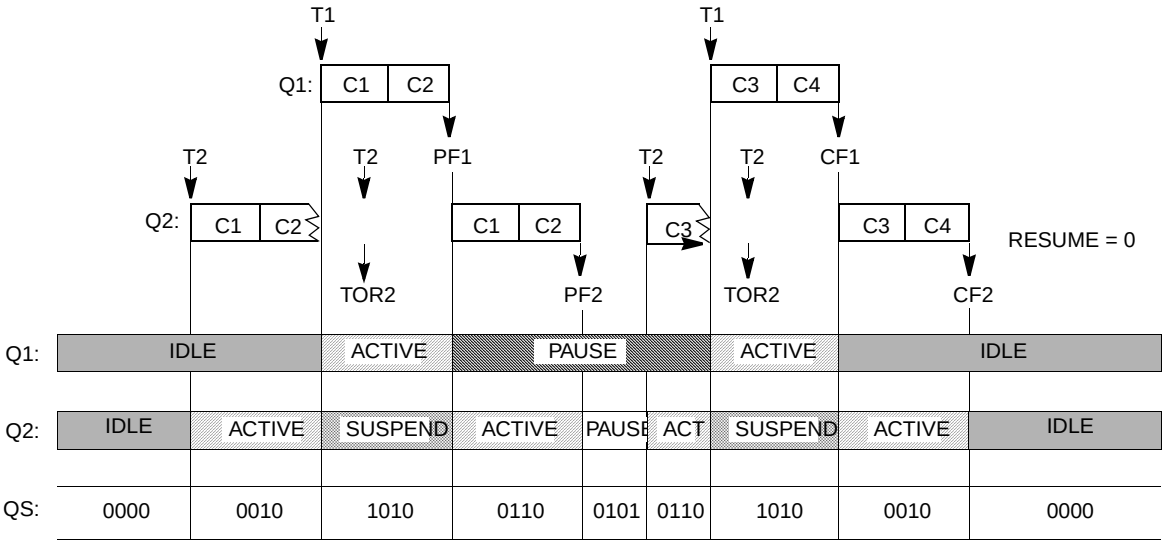


Figure 28-32. CCW Priority Situation 10

Table 33-3. DC Electrical Specifications[1] (continued)

(V_{SS} = V_{SSPLL} = V_{SSF} = V_{SSA} = 0 V_{DC})

Characteristic	Symbol	Min	Max	Unit
Load Capacitance[3] (50% Partial Drive) (100% Full Drive)	C_L		 25 50	pF
Supply Voltage (includes core modules and pads)	V_{DD}	2.7	3.6	V
RAM Memory Standby Supply Voltage Normal Operation: $V_{DD} > V_{STBY}$ - 0.3 V Standby Mode: $V_{DD} < V_{STBY}$ - 0.3 V	V_{STBY}	 0.0 1.8	 3.6 3.6	V
Flash Memory Supply Voltage (not applicable to MCF5280)	V_{DDF}	2.7	3.6	V

1 Refer to Table 33-8 through Table 33-12 for additional PLL, QADC, and Flash specifications.
2 This parameter is characterized before qualification rather than 100% tested.
3 Refer to the chip configuration section for more information. Drivers for the SDRAM pins are at 25pF drive strength.Drivers for the QADC pins are at 50pF drive strength.

33.4 Power Consumption Specifications

Table 33-4. STOP Mode Current Consumption Specifications

Characteristic	Symbol	Typical– Master Mode	Typical– Single Chip Mode[1]	Max[2]	Unit
System clocks disabled (LPCR[STPMD] = 00)	I_{DD}	25	7.9	—	mA
System clocks and CLKOUT disabled (LPCR[STPMD] = 01)	I_{DD}	7.3	5.6	—	mA
System clocks, CLKOUT, and PLL disabled (LPCR[STPMD] = 10)	I_{DD}	4.5	4.7	—	mA
System clocks, CLKOUT, PLL, and OSC disabled (LPCR[STPMD] = 11)	I_{DD}	400	750	1000	µA

1 Single chip mode current measured with all pins in general purpose input mode except for the UART0 and FEC pins that are enabled for their module functionality.
2 Maximum values can vary depending on the system's state and signal loading.

Figure 33-1 shows typical WAIT/DOZE and RUN mode power consumption for both master and single chip mode as measured on an M5282EVB.

For master mode the RUN mode current was measured executing a continuous loop that performs no operation while running from the on-chip SRAM.

For WAIT/DOZE mode measurements the peripherals on the device are in their default power savings mode, so the WAIT and DOZE power consumption are the same. Some modules can be programmed to shutdown in WAIT and/or DOZE modes. Refer to module chapters for more information.

All single chip mode measurements were taken with all pins in general purpose input mode except for the UART0 and FEC pins that are enabled for their module functionality; however, neither module is being accessed at the time of the current measurement. Single chip RUN mode current was measured executing a continuous loop that performs no operation while running from the on-chip Flash.

Table A-3. Register Memory Map (continued)

Address	Name	Mnemonic	Size
IPSBAR + 0xCEC	Level 3 Interrupt Acknowledge Register 0	L3IACKR0	8
IPSBAR + 0xCF0	Level 4 Interrupt Acknowledge Register 0	L4IACKR0	8
IPSBAR + 0xCF4	Level 5 Interrupt Acknowledge Register 0	L5IACKR0	8
IPSBAR + 0xCF8	Level 6 Interrupt Acknowledge Register 0	L6IACKR0	8
IPSBAR + 0xCFC	Level 7 Interrupt Acknowledge Register 0	L7IACKR0	8
Interrupt Controller 1			
IPSBAR + 0xD00	Interrupt Pending Register High 1	IPRH1	32
IPSBAR + 0xD04	Interrupt Pending Register Low 1	IPRL1	32
IPSBAR + 0xD08	Interrupt Mask Register High 1	IMRH1	32
IPSBAR + 0xD0C	Interrupt Mask Register Low 1	IMRL1	32
IPSBAR + 0xD10	Interrupt Force Register High 1	INTFRCH1	32
IPSBAR + 0xD14	Interrupt Force Register Low 1	INTFRCL1	32
IPSBAR + 0xD18	Interrupt Level Request Register 1	ILRR1	8
IPSBAR + 0xD19	Interrupt Acknowledge Level and Priority Register 1	IACKLPR1	8
IPSBAR + 0xD48	Interrupt Control Register 1-08	ICR108	8
IPSBAR + 0xD49	Interrupt Control Register 1-09	ICR109	8
IPSBAR + 0xD4A	Interrupt Control Register 1-10	ICR110	8
IPSBAR + 0xD4B	Interrupt Control Register 1-11	ICR111	8
IPSBAR + 0xD4C	Interrupt Control Register 1-12	ICR112	8
IPSBAR + 0xD4D	Interrupt Control Register 1-13	ICR113	8
IPSBAR + 0xD4E	Interrupt Control Register 1-14	ICR114	8
IPSBAR + 0xD4F	Interrupt Control Register 1-15	ICR115	8
IPSBAR + 0xD50	Interrupt Control Register 1-16	ICR116	8
IPSBAR + 0xD51	Interrupt Control Register 1-17	ICR117	8
IPSBAR + 0xD52	Interrupt Control Register 1-18	ICR118	8
IPSBAR + 0xD53	Interrupt Control Register 1-19	ICR119	8
IPSBAR + 0xD54	Interrupt Control Register 1-20	ICR120	8
IPSBAR + 0xD55	Interrupt Control Register 1-21	ICR121	8
IPSBAR + 0xD56	Interrupt Control Register 1-22	ICR122	8
IPSBAR + 0xD57	Interrupt Control Register 1-23	ICR123	8
IPSBAR + 0xD58	Interrupt Control Register 1-24	ICR124	8
IPSBAR + 0xD59	Interrupt Control Register 1-25	ICR125	8

F

G

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