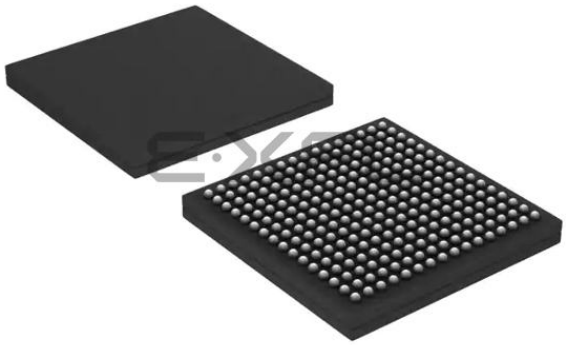

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Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	150
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
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Chapter 27
Chip Configuration Module (CCM)

- User’s manuals — These books provide details about individual ColdFire implementations and are intended to be used in conjunction with the *ColdFire Programmers Reference Manual.*
- Data sheets — Data sheets provide specific data regarding pin-out diagrams, bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations.
- Product briefs — Each device has a product brief that provides an overview of its features. This document is roughly equivalent to the overview (Chapter 1) of an device’s reference manual.
- Application notes — These short documents address specific design issues useful to programmers and engineers working with Freescale Semiconductor processors.

Additional literature is published as new processors become available. For a current list of ColdFire documentation, refer to http://www.freescale.com/coldfire.

Conventions

This document uses the following notational conventions:

MNEMONICS	In text, instruction mnemonics are shown in uppercase.
`mnemonics`	In code and tables, instruction mnemonics are shown in lowercase.
italics	Italics indicate variable command parameters. Book titles in text are set in italics.
0x0	Prefix to denote hexadecimal number
0b0	Prefix to denote binary number
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, RAMBAR[BA] identifies the base address field in the RAM base address register.
nibble	A 4-bit data unit
byte	An 8-bit data unit
word	A 16-bit data unit[1]
longword	A 32-bit data unit
x	In some contexts, such as signal encodings, x indicates a don’t care.
n	Used to express an undefined numerical value
~	NOT logical operator
&	AND logical operator
|	OR logical operator

[1]The only exceptions to this appear in the discussion of serial communication modules that support variable-length data transmission units. To simplify the discussion these units are referred to as words regardless of length.

	31	0
Field	SAR	
Reset	0000_0000_0000_0000_0000_0000_0000_0000	
R/W	R/W	
Address	IPSBAR + 0x100, 0x140, 0x180, 0x1C0	

Figure 16-4. Source Address Registers (SAR*n*)

NOTE

The backdoor enable bit must be set in both the core and SCM in order to enable backdoor accesses from the DMA to SRAM. See Section 8.4.2, “Memory Base Address Register (RAMBAR)” for more details.

NOTE

Flash accesses (reads/writes) by a bus master other than the core (DMA controller or Fast Ethernet Controller), or writes to Flash by the core during programming, must use the backdoor Flash address of IPSBAR plus an offset of 0x0400_0000. For example, for a DMA transfer from the first Flash location when IPSBAR is still at its default location of 0x4000_0000, the source register would be loaded with 0x4400_0000. Backdoor Flash read accesses can be made with the bus master, but it takes two cycles longer than a direct read of the Flash when using the FLASHBAR address.

16.4.2 Destination Address Registers (DAR0–DAR3)

DAR*n*, shown in Figure 16-5, holds the address to which the DMA controller sends data.

	31	0
Field	DAR	
Reset	0000_0000_0000_0000_0000_0000_0000_0000	
R/W	R/W	
Address	IPSBAR + 0x104, 0x144, 0x184, 0x1C4	

Figure 16-5. Destination Address Registers (DAR*n*)

NOTE

The DMA does not maintain coherency with the cache. Therefore, DMAs should not transfer data to cacheable memory unless software is used to maintain the cache coherency.

NOTE

The DMA should not be used to write data to the UART transmit FIFO in cycle steal mode. When the UART interrupt is used as a DMA request it does not negate fast enough to get a single transfer. The UART transmit FIFO only has one entry so the data from the second byte would be lost.

IPSBAR Offset: 0x1024 Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ETHER_EN	RESET
W																																
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-6. Ethernet Control Register (ECR)

Table 17-9. ECR Field Descriptions

Field	Description
31–2	Reserved, must be cleared.
1 ETHER_EN	When this bit is set, FEC is enabled, and reception and transmission are possible. When this bit is cleared, reception immediately stops and transmission stops after a bad CRC is appended to any currently transmitted frame. The buffer descriptor(s) for an aborted transmit frame are not updated after clearing this bit. When ETHER_EN is cleared, the DMA, buffer descriptor, and FIFO control logic are reset, including the buffer descriptor and FIFO pointers. Hardware alters the ETHER_EN bit under the following conditions: • ECR[RESET] is set by software, in which case ETHER_EN is cleared • An error condition causes the EIR[EBERR] bit to set, in which case ETHER_EN is cleared
0 RESET	When this bit is set, the equivalent of a hardware reset is performed but it is local to the FEC. ECR[ETHER_EN] is cleared and all other FEC registers take their reset values. Also, any transmission/reception currently in progress is abruptly aborted. This bit is automatically cleared by hardware during the reset sequence. The reset sequence takes approximately eight internal bus clock cycles after this bit is set.

17.4.7 MII Management Frame Register (MMFR)

The MMFR is user-accessible and does not reset to a defined value. The MMFR register is used to communicate with the attached MII compatible PHY device(s), providing read/write access to their MII registers. Performing a write to the MMFR causes a management frame to be sourced unless the MSCR is programmed to 0. If MSCR is cleared while MMFR is written and then MSCR is written with a non-zero value, an MII frame is generated with the data previously written to the MMFR. This allows MMFR and MSCR to be programmed in either order if MSCR is currently zero.

IPSBAR Offset: 0x1040 Access: User read/write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	ST				OP				PA					RA			TA				DATA												
Reset	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Figure 17-7. MII Management Frame Register (MMFR)

17.5.8 FEC Frame Reception

The FEC receiver works with almost no intervention from the host and can perform address recognition, CRC checking, short frame checking, and maximum frame length checking. The Ethernet controller receives serial data lsb first.

When the driver enables the FEC receiver by setting ECR[ETHER_EN], it immediately starts processing receive frames. When FEC_RXDV is asserted, the receiver first checks for a valid PA/SFD header. If the PA/SFD is valid, it is stripped and the receiver processes the frame. If a valid PA/SFD is not found, the frame is ignored.

In serial mode, the first 16 bit times of RX_D0 following assertion of FEC_RXDV are ignored. Following the first 16 bit times, the data sequence is checked for alternating 1/0s. If a 11 or 00 data sequence is detected during bit times 17 to 21, the remainder of the frame is ignored. After bit time 21, the data sequence is monitored for a valid SFD (11). If a 00 is detected, the frame is rejected. When a 11 is detected, the PA/SFD sequence is complete.

In MII mode, the receiver checks for at least one byte matching the SFD. Zero or more PA bytes may occur, but if a 00 bit sequence is detected prior to the SFD byte, the frame is ignored.

After the first 6 bytes of the frame are received, the FEC performs address recognition on the frame.

After a collision window (64 bytes) of data is received and if address recognition has not rejected the frame, the receive FIFO signals the frame is accepted and may be passed on to the DMA. If the frame is a runt (due to collision) or is rejected by address recognition, the receive FIFO is notified to reject the frame. Therefore, no collision fragments are presented to you except late collisions, which indicate serious LAN problems.

During reception, the Ethernet controller checks for various error conditions and after the entire frame is written into the FIFO, a 32-bit frame status word is written into the FIFO. This status word contains the M, BC, MC, LG, NO, CR, OV, and TR status bits, and the frame length. See Section 17.5.15.2, “Reception Errors,” for more details.

Receive buffer (RXB) and frame interrupts (RFINT) may be generated if enabled by the EIMR register. A receive error interrupt is a babbling receiver error (BABR). Receive frames are not truncated if they exceed the max frame length (MAX_FL); however, the BABR interrupt occurs and the LG bit in the receive buffer descriptor (RxBD) is set. See Section 17.5.1.2, “Ethernet Receive Buffer Descriptor (RxBD),” for more details.

When the receive frame is complete, the FEC sets the L-bit in the RxBD, writes the other frame status bits into the RxBD, and clears the E-bit. The Ethernet controller next generates a maskable interrupt (RFINT bit in EIR, maskable by RFIEN bit in EIMR), indicating that a frame is received and is in memory. The Ethernet controller then waits for a new frame.

17.5.9 Ethernet Address Recognition

The FEC filters the received frames based on destination address (DA) type — individual (unicast), group (multicast), or broadcast (all-ones group address). The difference between an individual address and a

20.3 Low-Power Mode Operation

This subsection describes the operation of the general purpose time module in low-power modes and halted mode of operation. Low-power modes are described in the Power Management Module. Table 3-1 shows the general purpose timer module operation in the low-power modes, and shows how this module may facilitate exit from each mode.

Table 20-1. Watchdog Module Operation in Low-power Modes

Low-power Mode	Watchdog Operation	Mode Exit
Wait	Normal	No
Doze	Normal	No
Stop	Stopped	No
Halted	Normal	No

General purpose timer operation stops in stop mode. When stop mode is exited, the general purpose timer continues to operate in its pre-stop mode state.

20.4 Signal Description

Table 20-2 provides an overview of the signal properties.

NOTE

Throughout this section, an "*n*" in the pin name, as in "GPT*n*0," designates GPTA or GPTB.

Table 20-2. Signal Properties

Pin Name	GPTPORT Register Bit	Function	Reset State	Pull-up
GPT*n*0	PORTT*n*0	GPT*n* channel 0 IC/OC pin	Input	Active
GPT*n*1	PORTT*n*1	GPT*n* channel 1 IC/OC pin	Input	Active
GPT*n*2	PORTT*n*2	GPT*n* channel 2 IC/OC pin	Input	Active
GPT*n*3	PORTT*n*3	GPT*n* channel 3 IC/OC or PA pin	Input	Active
SYNC*n*	PORTE[3:0][1]	GPT*n* counter synchronization	Input	Active

[1] SYNCA is available on either PORTE3 or PORTE1; SYNCB is available on either PORTE2 or PORTE0.

20.4.1 GPT*n*[2:0]

The GPT*n*[2:0] pins are for channel 2–0 input capture and output compare functions. These pins are available for general-purpose input/output (I/O) when not configured for timer functions.

20.4.2 GPT*n*3

The GPT*n*3 pin is for channel 3 input capture and output compare functions or for the pulse accumulator input. This pin is available for general-purpose I/O when not configured for timer functions.

Chapter 21
DMA Timers (DTIM0–DTIM3)

21.1 Introduction

This chapter describes the configuration and operation of the four direct memory access (DMA) timer modules (DTIM0, DTIM1, DTIM2, and DTIM3). These 32-bit timers provide input capture and reference compare capabilities with optional signaling of events using interrupts or DMA triggers. Additionally, programming examples are included.

NOTE

The designation *n* appears throughout this section to refer to registers or signals associated with one of the four identical timer modules: DTIM0, DTIM1, DTIM2, or DTIM3.

21.1.1 Overview

Each DMA timer module has a separate register set for configuration and control. The timers can be configured to operate from the internal bus clock or from an external clocking source using the DTIN*n* signal. If the internal bus clock is selected, it can be divided by 16 or 1. The selected clock source is routed to an 8-bit programmable prescaler that clocks the actual DMA timer counter register (DTCN*n*). Using the DTMR*n*, DTXMR*n*, DTCR*n*, and DTRR*n* registers, the DMA timer may be configured to assert an output signal, generate an interrupt, or request a DMA transfer on a particular event.

NOTE

The GPIO module must be configured to enable the peripheral function of the appropriate pins (refer to Chapter 26, “General Purpose I/O Module”) prior to configuring the DMA Timers.

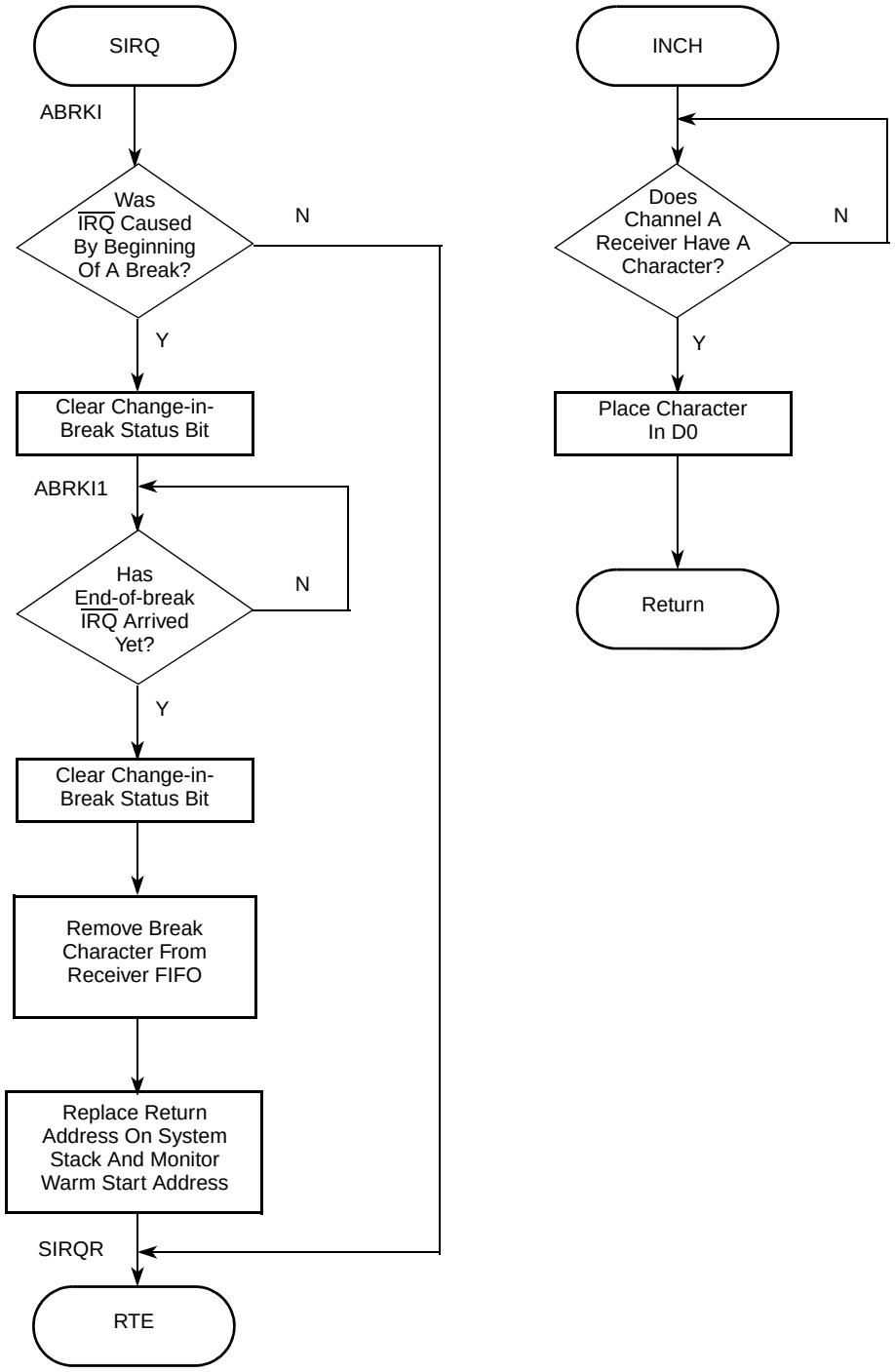


Figure 23-25. UART Mode Programming Flowchart (Sheet 4 of 5)

A received remote frame is not stored in a receive message buffer. It is only used to trigger the automatic transmission of a frame in response. The mask registers are not used in remote frame ID matching. All ID bits (except RTR) of the incoming received frame must match for the remote frame to trigger a response transmission.

25.4.5 Overload Frames

Overload frame transmissions are not initiated by the FlexCAN unless certain conditions are detected on the CAN bus. These conditions include:

- Detection of a dominant bit in the first or second bit of intermission.
- Detection of a dominant bit in the seventh (last) bit of the end-of-frame (EOF) field in receive frames.
- Detection of a dominant bit in the eighth (last) bit of the error frame delimiter or overload frame delimiter.

25.4.6 Time Stamp

The value of the free-running 16-bit timer is sampled at the beginning of the identifier field on the CAN bus. For a message being received, the time stamp will be stored in the time stamp entry of the receive message buffer at the time the message is written into that buffer. For a message being transmitted, the time stamp entry will be written into the transmit message buffer once the transmission has completed successfully.

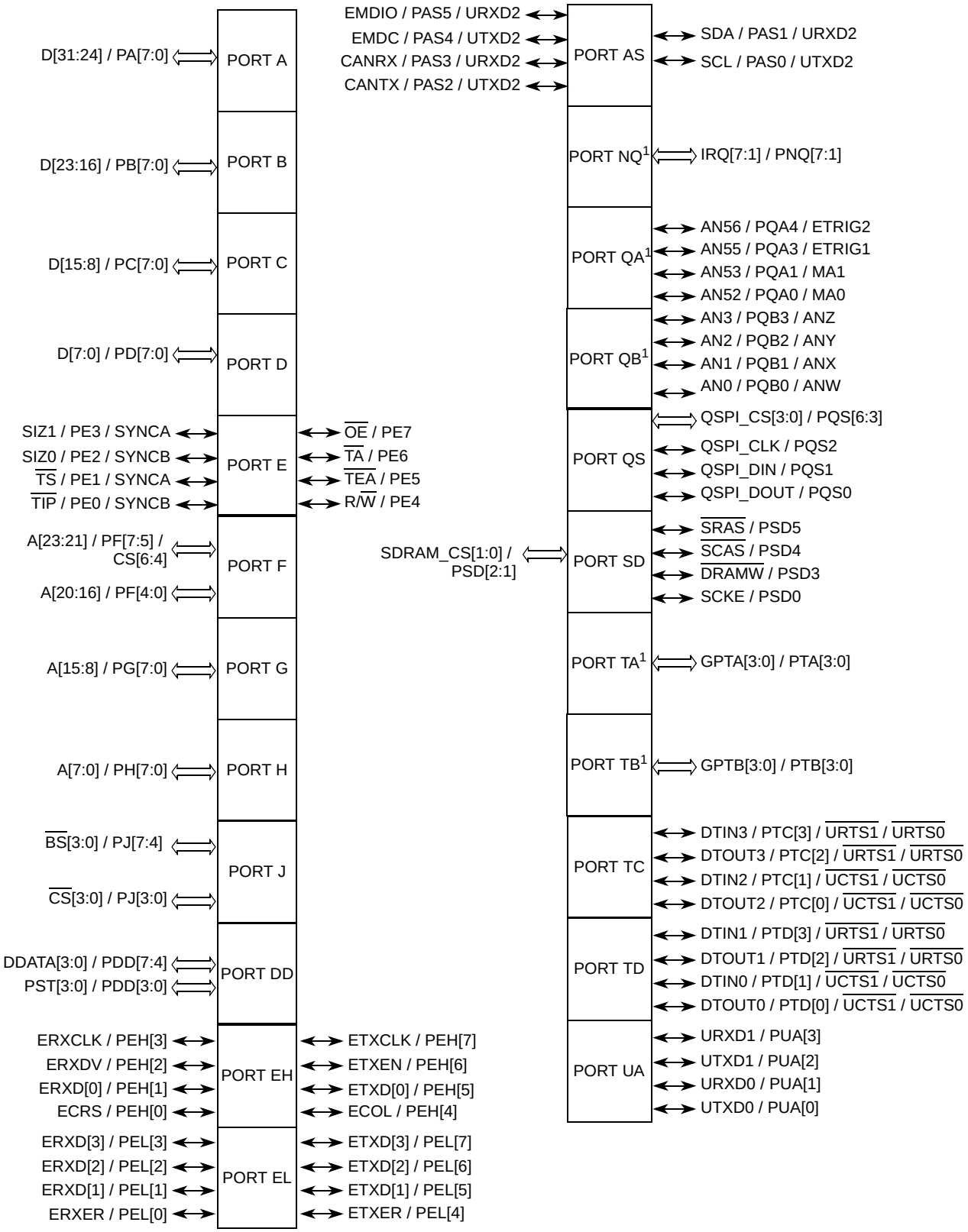
The free-running timer can optionally be reset upon the reception of a frame into message buffer 0. This feature allows network time synchronization to be performed.

25.4.7 Listen-Only Mode

In listen-only mode, the FlexCAN module is able to receive messages without giving an acknowledgment. Whenever the module enters this mode the status of the Error Counters is frozen and the FlexCAN module operates like in error passive mode. Since the module does not influence the CAN bus in this mode the host device is capable of functioning like a monitor or for automatic bit-rate detection.

25.4.8 Bit Timing

The FlexCAN module uses three 8-bit registers to set up the bit timing parameters required by the CAN protocol. Control registers 1 and 2 (CANCTRL1, CANCTRL2) contain the PROPSEG, PSEG1, PSEG2, and the RJW fields which allow the user to configure the bit timing parameters. The prescaler divide register (PRESDIV) allows the user to select the ratio used to derive the S-clock from the system clock. The time quanta clock operates at the S-clock frequency. Table 25-7 provides examples of system clock, CAN bit rate, and S-clock bit timing parameters.



1. Although ports NQ, QA, QB, TA, and TB are not part of the ports module, they are included here for comprehensiveness.

Figure 26-2. MCF5280, MCF5281, and MCF5282 Ports Module Block Diagram

Table 26-1. Ports External Signals (continued)

Primary Function (Pin Name)[1]	GPIO (Default Function)	Alternate Function 1	Alternate Function 2	Description
$\overline{\text{SCAS}}$	PSD[4]		—	SDRAM synchronous column address strobe / Port SD[4]
$\overline{\text{DRAMW}}$	PSD[3]	—	—	SDRAM write enable / Port SD[3]
$\overline{\text{SDRAM\_CS}}$[1:0]	PSD[2:1]	—	—	SDRAM row address strobes 1, 0 / Port SD[2:1]
SCKE	PSD[0]	—	—	SDRAM clock enable / Port SD[0]
GPTA[3:0] [2]	PTA[3:0]	—	—	General purpose timer A input/output / Port TA[3:0]
GPTB[3:0] [2]	PTB[3:0]	—	—	General purpose timer B input/output / Port TB[3:0]
DTIN3	PTC[3]	$\overline{\text{URTS1}}$	$\overline{\text{URTS0}}$	DMA timer 3 input / Port TC[3] / UART1 request to send / UART0 request to send
DTOUT3	PTC[2]	$\overline{\text{URTS1}}$	$\overline{\text{URTS0}}$	DMA timer 3 output / Port TC[2] / UART1 request to send / UART0 request to send
DTIN2	PTC[1]	$\overline{\text{UCTS1}}$	$\overline{\text{UCTS0}}$	DMA timer 2 input / Port TC[1] / UART1 clear to send / UART0 clear to send
DTOUT2	PTC[0]	$\overline{\text{UCTS1}}$	$\overline{\text{UCTS0}}$	DMA timer 2 output / Port TC[0] / UART1 clear to send / UART0 clear to send
DTIN1	PTD[3]	$\overline{\text{URTS1}}$	$\overline{\text{URTS0}}$	DMA timer 1 input / Port TD[3] / UART1 request to send / UART0 request to send
DTOUT1	PTD[2]	$\overline{\text{URTS1}}$	$\overline{\text{URTS0}}$	DMA timer 1 output / Port TD[2] / UART1 request to send / UART0 request to send
DTIN0	PTD[1]	$\overline{\text{UCTS1}}$	$\overline{\text{UCTS0}}$	DMA timer 0 input / Port TD[1] / UART1 clear to send / UART0 clear to send
DTOUT0	PTD[0]	$\overline{\text{UCTS1}}$	$\overline{\text{UCTS0}}$	DMA timer 0 output / Port TD[0] / UART1 clear to send / UART0 clear to send
URXD1	PUA[3]	—	—	UART1 receive serial data / Port UA[3]
UTXD1	PUA[2]	—	—	UART1 transmit serial data / Port UA[2]
URXD0	PUA[1]	—	—	UART0 receive serial data / Port UA[1]
UTXD0	PUA[0]	—	—	UART0 transmit serial data / Port UA[0]
The following signals apply to the MCF5280, MCF5281, and MCF5282				
ETXCLK	PEH[7]	—	—	Ethernet transmit clock / PEH[7]
ETXEN	PEH[6]	—	—	Ethernet transmit enable / PEH[6]
ETXD[0]	PEH[5]	—	—	Ethernet transmit data [0] / PEH[5]
ECOL	PEH[4]	—	—	Ethernet collision / PEH[4]
ERXCLK	PEH[3]	—	—	Ethernet receive clock / PEH[3]
ERXDV	PEH[2]	—	—	Ethernet receive data valid / PEH[2]
ERXD[0]	PEH[1]	—	—	Ethernet receive data [0] / PEH[1]

27.3 Block Diagram

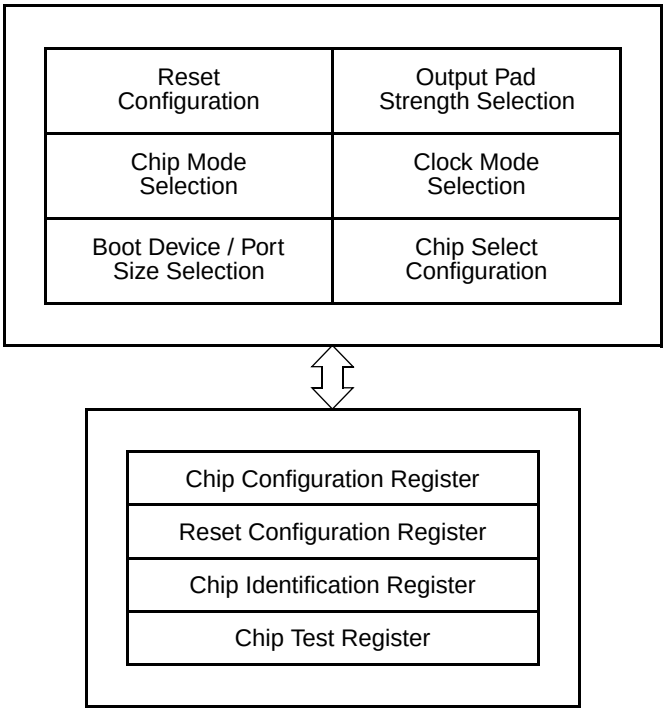


Figure 27-1. Chip Configuration Module Block Diagram

27.4 Signal Descriptions

Table 27-1 provides an overview of the CCM signals.

Table 27-1. Signal Properties

Name	Function	Reset State
$\overline{\text{RCON}}$	Reset configuration select	Internal weak pull-up device
CLKMOD[1:0]	Clock mode select	—
D[26:24, 21, 19:16]	Reset configuration override pins	—

27.4.1 $\overline{\text{RCON}}$

If the external $\overline{\text{RCON}}$ pin is asserted during reset, then various chip functions, including the reset configuration pin functions after reset, are configured according to the levels driven onto the external data pins. (see Section 27.6, “Functional Description”). The internal configuration signals are driven to reflect the levels on the external configuration pins to allow for module configuration.

27.4.2 CLKMOD[1:0]

The state of the CLKMOD[1:0] pins during reset determines the clock mode.

NOTE

When Flash security is enabled, the chip will boot in single chip mode regardless of the external reset configuration.

Table 27-9. Chip Configuration Mode Selection[1]

Chip Configuration Mode	CCR Register MODE Field		
	MODE2	MODE1	MODE0
Master mode	D26 driven high	D17 driven high	D16 driven high
Single-chip mode	D26 driven high	D17 driven high	D16 driven low
Reserved	D26 driven high	D17 driven low	D16 driven high
Reserved	D26 driven low	D17 don't care	D16 don't care

1 Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

During reset, certain module configurations depend on whether emulation mode is active as determined by the state of the internal emulation signal.

27.6.3 Boot Device Selection

During reset configuration, the $\overline{\text{CS0}}$ chip select pin is optionally configured to select an external boot device. In this case, the V (valid) bit in the CSMR0 register is ignored, and $\overline{\text{CS0}}$ is enabled after reset. $\overline{\text{CS0}}$ is asserted for the initial boot fetch accessed from address 0x0000_0000 for the Stack Pointer and address 0x0000_0004 for the program counter (PC). It is assumed that the reset vector loaded from address 0x0000_0004 causes the CPU to start executing from external memory space decoded by $\overline{\text{CS0}}$.

27.6.4 Output Pad Strength Configuration

Output pad strength is determined during reset configuration as shown in Table 27-10. Once reset is exited, the output pad strength configuration can be changed by programming the LOAD bit of the chip configuration register.

Table 27-10. Output Pad Driver Strength Selection[1]

Optional Pin Function Selection	CCR Register LOAD Bit
Output pads configured for partial strength	D21 driven low
Output pads configured for full strength	D21 driven high

1 Modifying the default configurations is possible only if the external $\overline{\text{RCON}}$ pin is asserted low.

27.6.5 Clock Mode Selection

The clock mode is selected during reset by the CLKMOD pins and reflected in the PLLMODE, PLLSEL, and PLLREF bits of SYNSR. After reset is exited, the clock mode cannot be changed.

Table 27-11 summarizes clock mode selection during reset configuration.

	7	6	5	4	3	2	1	0
Field	—				DDQB3	DDQB2	DDQB1	DDQB0
Reset	0000_0000							
R/W	R							
Address	IPSBAR + 0x19_0009							

Figure 28-7. Port QB Data Direction Register (DDRQB)

28.6.5 Control Registers

This subsection describes the QADC control registers.

28.6.5.1 QADC Control Register 0 (QACR0)

QACR0 establishes the QADC sampling clock (QCLK) with prescaler parameter fields and defines whether external multiplexing is enabled. Typically, these bits are written once when the QADC is initialized and not changed thereafter. The bits in this register are read anytime, write anytime (except during stop mode).

	15	14	13	12	11	8
Field	MUX	—		TRG	—	
Reset	0000_0000					
R/W:	R/W	R		R/W	R	

	7	6	5	4	3	2	1	0
Field	—	QPR6	QPR5	QPR4	QPR3	QPR2	QPR1	QPR0
Reset	0001_0011							
R/W:	R	R/W						
Address	IPSBAR + 0x19_000a, 0x19_000b							

Figure 28-8. QADC Control Register 0 (QACR0)

Table 28-4. QACR0 Field Descriptions

Bit(s)	Name	Description
15	MUX	Externally multiplexed mode. Configures the QADC for operation in externally multiplexed mode, which affects the interpretation of the channel numbers and forces the MA[1:0] signals to be outputs. 1 Externally multiplexed, up to 18 possible channels 0 Internally multiplexed, up to 8 possible channels
14–13	—	Reserved, should be cleared.
12	TRG	Trigger assignment. Determines the queue assignment of the ETRIG[2:1] signals. 1 ETRIG1 triggers queue 2; ETRIG2 triggers queue 1. 0 ETRIG1 triggers queue 1; ETRIG2 triggers queue 2.

NOTE

Although the result RAM can be written, some write operations, like bit manipulation, may not operate as expected because the hardware cannot access a true 16-bit value.

While there is only one result word table, the half-word (16-bit) data can be accessed in three different data formats:

- Right justified with 0s in the higher order unused bits
- Left justified with the most significant bit inverted to form a sign bit, and 0s in the unused lower order bits
- Left justified with 0s in the lower order unused bits

The left justified, signed format corresponds to a half-scale, offset binary, two's complement data format. The address used to read the result table determines the data alignment format. All write operations to the result word table are right justified.

28.9 Signal Connection Considerations

The QADC requires accurate, noise-free input signals for proper operation. This section discusses the design of external circuitry to maximize QADC performance.

28.9.1 Analog Reference Signals

No A/D converter can be more accurate than its analog reference. Any noise in the reference can result in at least that much error in a conversion. The reference for the QADC, supplied by signals V_{RH} and V_{RL}, should be low-pass filtered from its source to obtain a noise-free, clean signal. In many cases, simple capacitive bypassing may suffice. In extreme cases, inductors or ferrite beads may be necessary if noise or RF energy is present. External resistance may introduce error in this architecture under certain conditions. Any series devices in the filter network should contain a minimum amount of DC resistance.

For accurate conversion results, the analog reference voltages must be within the limits defined by V_{DDA} and V_{SSA}, as explained in this subsection.

28.9.2 Analog Power Signals

The analog supply signals (V_{DDA} and V_{SSA}) define the limits of the analog reference voltages (V_{RH} and V_{RL}) and of the analog multiplexer inputs. Figure 28-44 is a diagram of the analog input circuitry.

NOTE

DUMP does not check for a valid address; it is a valid command only when preceded by NOP, READ, or another DUMP command. Otherwise, an illegal command response is returned. NOP can be used for intercommand padding without corrupting the address pointer.

The size field is examined each time a DUMP command is processed, allowing the operand size to be dynamically altered.

Command/Result Formats:

		15 12				11 8				7 4	3 0
Byte	Command	0x1				0xD				0x0	0x0
	Result	X	X	X	X	X	X	X	X	D[7:0]	
Word	Command	0x1				0xD				0x4	0x0
	Result	D[15:0]									
Longword	Command	0x1				0xD				0x8	0x0
	Result	D[31:16]									
		D[15:0]									

Figure 30-25. DUMP Command/Result Formats

Table 31-4. IDCODE Register Field Descriptions

Bits	Name	Description
31–28	PRN	Part revision number. Indicate the revision number of the project.
27–22	DC	Design center.
21–12	PIN	Part identification number. Indicate the device number.
11–1	JEDEC	Joint electron device engineering council ID bits. Indicate the reduced JEDEC ID for Freescale.
0	ID	IDCODE register ID. This bit is set to 1 to identify the register as the IDCODE register and not the bypass register according to the IEEE standard 1149.1.

31.4.2.3 Bypass Register

The bypass register is a single-bit shift register path from TDI to TDO when the BYPASS instruction is selected.

31.4.2.4 JTAG_CFM_CLKDIV Register

The JTAG_CFM_CLKDIV register is a 7-bit clock divider for the CFM that is used with the LOCKOUT_RECOVERY instruction. It controls the period of the clock used for timed events in the CFM erase algorithm. The JTAG_CFM_CLKDIV register must be loaded before the lockout sequence can begin.

31.4.2.5 TEST_CTRL Register

The TEST_CTRL register is a 3-bit shift register path from TDI to TDO when the ENABLE_TEST_CTRL instruction is selected. The TEST_CTRL transfers its value to a parallel hold register on the rising edge of TCLK when the TAP state machine is in the update-DR state.

31.4.2.6 Boundary Scan Register

The boundary scan register is connected between TDI and TDO when the EXTEST or SAMPLE/PRELOAD instruction is selected. It captures input pin data, forces fixed values on output pins, and selects a logic value and direction for bidirectional pins or high impedance for tri-stated pins.

The boundary scan register contains bits for bonded-out and non bonded-out signals excluding JTAG signals, analog signals, power supplies, compliance enable pins, and clock signals.

31.5 Functional Description

31.5.1 JTAG Module

The JTAG module consists of a TAP controller state machine, which is responsible for generating all control signals that execute the JTAG instructions and read/write data registers.

31.5.2 TAP Controller

The TAP controller is a state machine that changes state based on the sequence of logical values on the TMS pin. Figure 31-3 shows the machine's states. The value shown next to each state is the value of the TMS signal sampled on the rising edge of the TCLK signal.

Asserting the $\overline{\text{TRST}}$ signal asynchronously resets the TAP controller to the test-logic-reset state. As Figure 31-3 shows, holding TMS at logic 1 while clocking TCLK through at least five rising edges also causes the state machine to enter the test-logic-reset state, whatever the initial state.

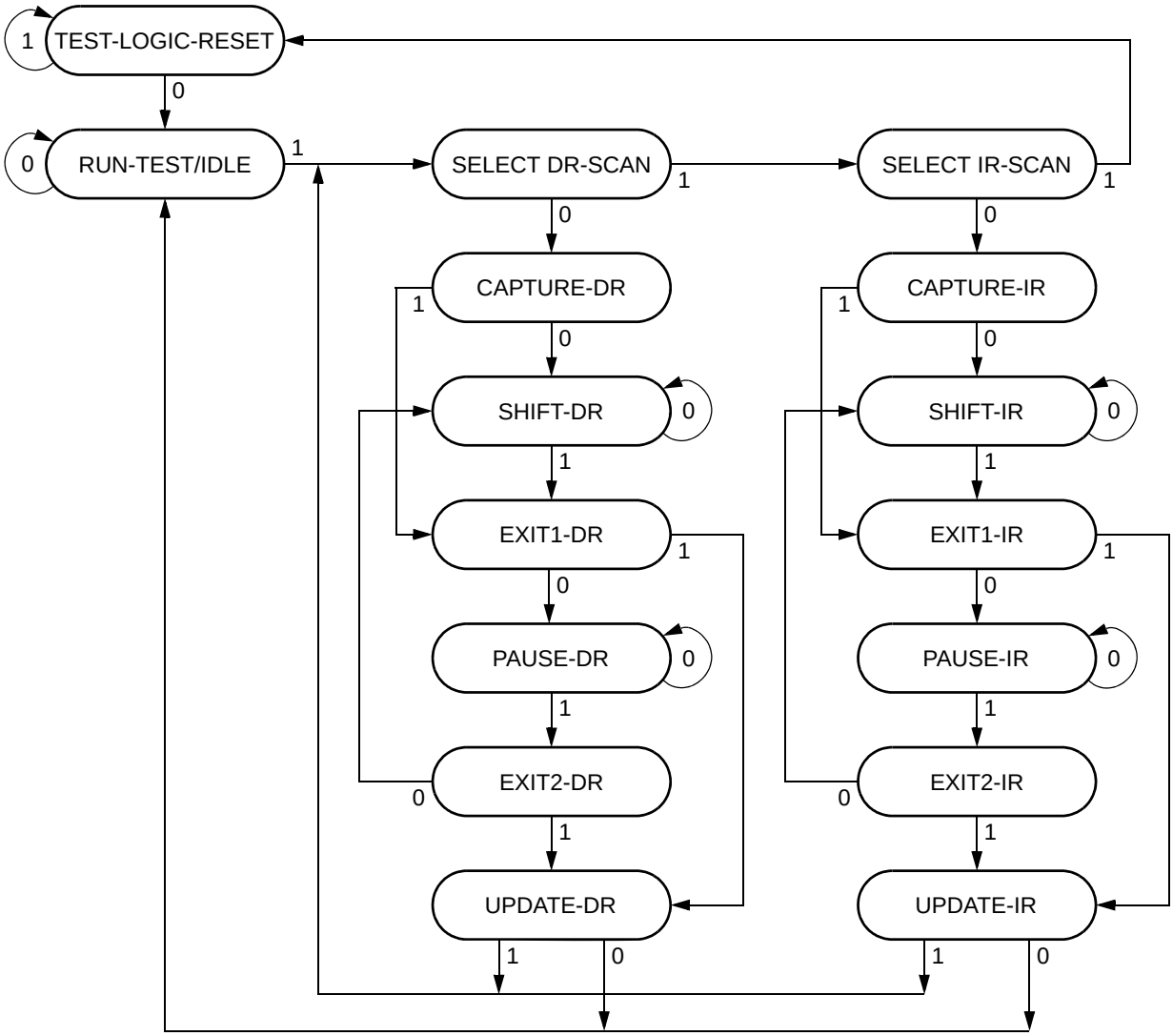


Figure 31-3. TAP Controller State Machine Flow

31.5.3 JTAG Instructions

Table 31-5 describes public and private instructions.

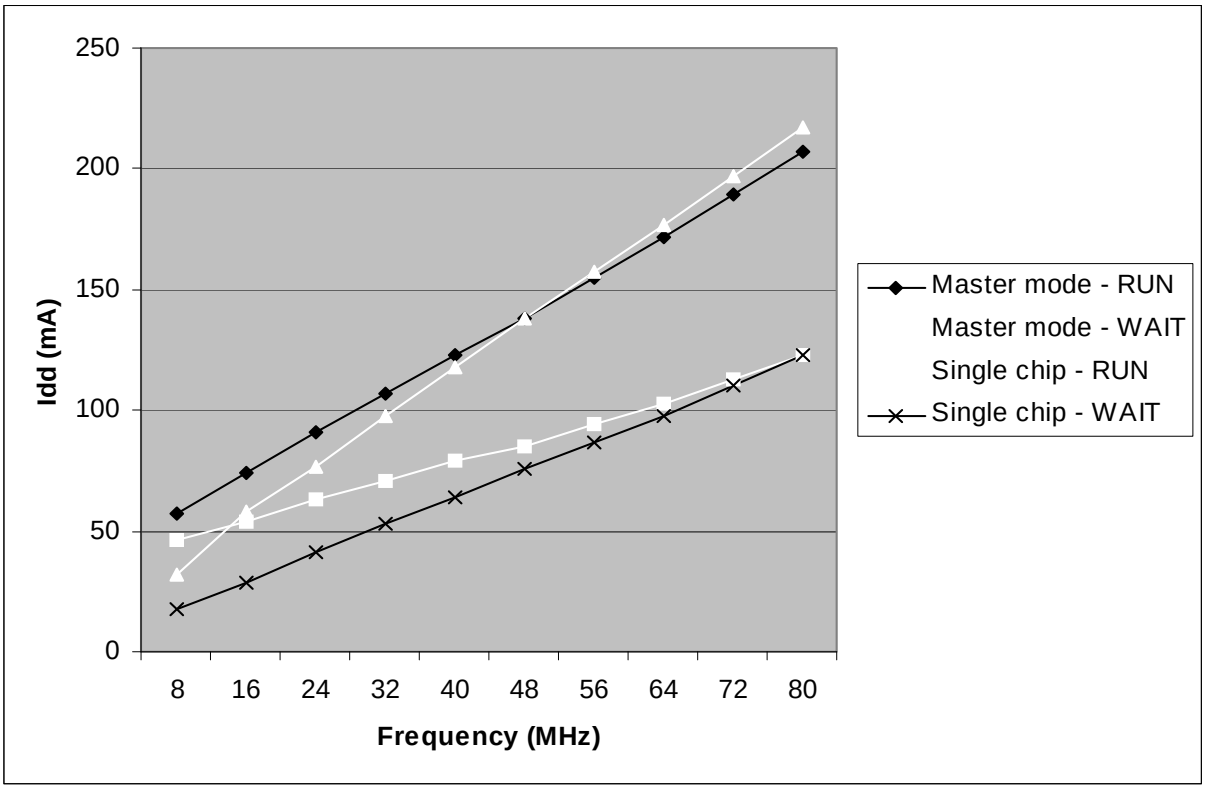


Figure 33-1. Typical WAIT/DOZE Mode Current Consumption

Table 33-5 lists the estimated power consumption for individual modules. The current consumption is for the module itself and does not include power for I/O.

Table 33-5. Estimated Module Power Consumption

Module	Estimated Power	Unit
EIM	20	µA/MHz
SDRAMC	30	µA/MHz
FEC	60	µA/MHz
Watchdog	1.5	µA/MHz
PIT	1	µA/MHz
FlexCAN	15	µA/MHz
QSPI, UART, I^2C, and Timers	75	µA/MHz

Table A-3. Register Memory Map (continued)

Address	Name	Mnemonic	Size
IPSBAR + 0xC18	Interrupt Level Request Register 0	ILRR0	8
IPSBAR + 0XC19	Interrupt Acknowledge Level and Priority Register 0	IACKLPR0	8
IPSBAR + 0xC41	Interrupt Control Register 0-01	ICR001	8
IPSBAR + 0xC42	Interrupt Control Register 0-02	ICR002	8
IPSBAR + 0xC43	Interrupt Control Register 0-03	ICR003	8
IPSBAR + 0xC44	Interrupt Control Register 0-04	ICR004	8
IPSBAR + 0xC45	Interrupt Control Register 0-05	ICR005	8
IPSBAR + 0xC46	Interrupt Control Register 0-06	ICR006	8
IPSBAR + 0xC47	Interrupt Control Register 0-07	ICR007	8
IPSBAR + 0xC48	Interrupt Control Register 0-08	ICR008	8
IPSBAR + 0xC49	Interrupt Control Register 0-09	ICR009	8
IPSBAR + 0xC4A	Interrupt Control Register 0-10	ICR010	8
IPSBAR + 0xC4B	Interrupt Control Register 0-11	ICR011	8
IPSBAR + 0xC4C	Interrupt Control Register 0-12	ICR012	8
IPSBAR + 0xC4D	Interrupt Control Register 0-13	ICR013	8
IPSBAR + 0xC4E	Interrupt Control Register 0-14	ICR014	8
IPSBAR + 0xC4F	Interrupt Control Register 0-15	ICR015	8
IPSBAR + 0xC51	Interrupt Control Register 0-17	ICR017	8
IPSBAR + 0xC52	Interrupt Control Register 0-18	ICR018	8
IPSBAR +0xC53	Interrupt Control Register 0-19	ICR019	8
IPSBAR + 0xC54	Interrupt Control Register 0-20	ICR020	8
IPSBAR + 0xC55	Interrupt Control Register 0-21	ICR021	8
IPSBAR + 0xC56	Interrupt Control Register 0-22	ICR022	8
IPSBAR + 0xC57	Interrupt Control Register 0-23	ICR023	8
IPSBAR + 0xC58	Interrupt Control Register 0-24	ICR024	8
IPSBAR + 0xC59	Interrupt Control Register 0-25	ICR025	8
IPSBAR + 0xC5A	Interrupt Control Register 0-26	ICR026	8
IPSBAR + 0xC5B	Interrupt Control Register 0-27	ICR027	8
IPSBAR + 0xC5C	Interrupt Control Register 0-28	ICR028	8
IPSBAR + 0xC5D	Interrupt Control Register 0-29	ICR029	8
IPSBAR + 0xC5E	Interrupt Control Register 0-30	ICR030	8
IPSBAR + 0xC5F	Interrupt Control Register 0-31	ICR031	8
IPSBAR + 0xC60	Interrupt Control Register 0-32	ICR032	8