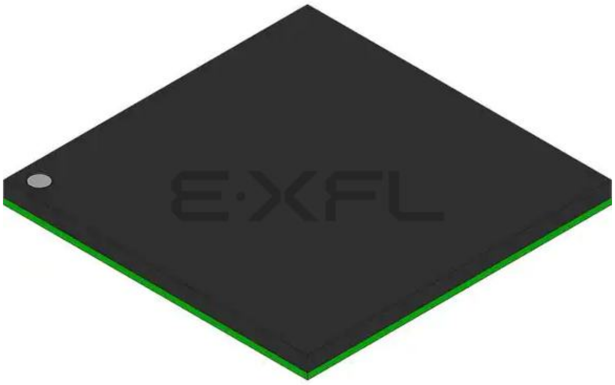
Freescale Semiconductor - MCF5281CVF66 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	142
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5281cvf66

The SRAM module is also accessible by non-core bus masters, for example the DMA and/or the FEC. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

1.1.1.3 Flash

This product incorporates SuperFlash® technology licensed from SST. The ColdFire Flash Module (CFM) is a non-volatile memory (NVM) module for integration with the processor core. The CFM is constructed with eight banks of 32K x 16-bit Flash arrays to generate 512 Kbytes of 32-bit Flash memory

NOTE

> The CFM on the MCF5281 and MCF5214 is constructed with four banks of 32K x 16-bit Flash arrays to generate 256 Kbytes of 32-bit Flash memory.
>
> The MCF5280 does not contain a CFM.

These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The Flash memory is ideal for program and data storage for single-chip applications allowing for field reprogramming without requiring an external programming voltage source. The CFM interfaces to the V2 ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle Flash arrays. A “backdoor” mapping of the Flash memory is used for all program, erase, and verify operations. It also provides a read datapath for non-core masters (for example, DMA).

1.1.1.4 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on Freescale’s 683xx family of parts.

The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor’s supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the CLKOUT output provide execution status, captured operand data, and branch target addresses defining the dynamic execution path of the processor at the CPU’s clock rate.

1.1.2 System Control Module

This section details the functionality of the System Control Module (SCM) which provides the programming model for the System Access Control Unit (SACU), the system bus arbiter, a 32-bit Core Watchdog Timer (CWT), and the system control registers and logic. Specifically, the system control includes the internal peripheral system base address register (IPSBAR), the processor’s dual-port RAM base address register (RAMBAR), and system control registers that include low-power and core watchdog timer control.

1.1.3 External Interface Module (EIM)

The external interface module handles the transfer of information between the internal core and memory, peripherals, or other processing elements in the external address space.

Programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

1.1.4 Chip Select

Programmable chip select outputs provide a glueless connection to external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

1.1.5 Power Management

The MCF5282 incorporates several low-power modes of operation which are entered under program control and exited by several external trigger events. An integrated Power-On Reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The Low Voltage Detect (LVD) section monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage is higher than the standby voltage. If the supply voltage to chip falls below the standby battery voltage, the RAM is switched over to the standby supply.

1.1.6 General Input/Output Ports

All of the pins associated with the external bus interface may be used for several different functions. Their primary function is to provide an external memory interface to access off-chip resources. When not used for this function, all of the pins may be used as general-purpose digital I/O pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

The digital I/O pins on the MCF5282 are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

1.1.7 Interrupt Controllers (INTC0/INTC1)

There are two interrupt controllers on the MCF5282, each of which can support up to 63 interrupt sources for a total of 126. Each interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 56 of the 63 sources of a given controller provide a programmable level [1-7] and priority within the level.

Table 8-14. GPACR Address Space

Register	Space Protected (IPSBAR Offset)	Modules Protected
GPACR0	0x0000_0000–0x03FF_FFFF	Ports, CCM, PMM, Reset controller, Clock, EPORT, WDOG, PIT0–PIT3, QADC, GPTA, GPTB, FlexCAN, CFM (Control)
GPACR1	0x0400_0000–0x07FF_FFFF	CFM (Flash module's backdoor access for programming or access by a bus master other than the core) **Note:** Reserved for the MCF5280

Table 9-10. Stop Mode Operation (Sheet 5 of 5)

MODE In	LOCEN	LOCRE	LOLRE	PLL	OSC	FWKUP	Expected PLL Action at Stop	PLL Action During Stop	MODE Out	LOCKSS	LOCK	LOCS	Comments
SCM	1	0	0	On	On	1	—	—	SCM	0	0	1	
								Lose reference clock	SCM				

Note:

PLL = PLL enabled during STOP mode. PLL = On when STPMD[1:0] = 00 or 01

OSC = Oscillator enabled during STOP mode. Oscillator is on when STPMD[1:0] = 00, 01, or 10

MODES

NRM = normal PLL crystal clock reference or normal PLL external reference or PLL 1:1 mode. During PLL 1:1 or normal external reference mode, the oscillator is never enabled. Therefore, during these modes, refer to the OSC = On case regardless of STPMD values.

EXT=external clock mode

REF=PLL reference mode due to losing PLL clock or lock from NRM mode

SCM=PLL self-clocked mode due to losing reference clock from NRM mode

RESET= immediate reset

LOCKS

‘LK= expecting previous value of LOCKS before entering stop

0–>‘LK= current value is 0 until lock is regained which then will be the previous value before entering stop

0–> = current value is 0 until lock is regained but lock is never expected to regain

LOCS

‘LC=expecting previous value of LOCS before entering stop

1–>‘LC= current value is 1 until clock is regained which then will be the previous value before entering stop

1–> =current value is 1 until clock is regained but CLK is never expected to regain

14.2.14.7 Debug Data (DDATA[3:0])

Debug data signals (DDATA[3:0]) display captured processor addresses, data and breakpoint status.

These pins can also be configured as GPIO PDD[7:4].

14.2.14.8 Processor Status Outputs (PST[3:0])

PST[3:0] outputs indicate core status, as shown below in Table 14-7. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer.

These pins can also be configured as GPIO PDD[3:0].

Table 14-7. Processor Status Encoding

PST[3:0]	Definition
0000	Continue execution
0001	Begin execution of an instruction
0010	Reserved
0011	Entry into user mode
0100	Begin execution of PULSE and WDDATA instruction
0101	Begin execution of taken branch
0110	Reserved
0111	Begin execution of RTE instruction
1000	Begin one-byte transfer on DDATA
1001	Begin two-byte transfer on DDATA
1010	Begin three-byte transfer on DDATA
1011	Begin four-byte transfer on DDATA
1100	Exception Processing
1101	Emulator-Mode Exception Processing
1110	Processor is stopped
1111	Processor is halted

14.2.15 Test Signals

14.2.15.1 Test (TEST)

This input signal is reserved for factory testing only and should be connected to VSS to prevent unintentional activation of test functions.

14.2.16 Power and Reference Signals

These signals provide system power, ground and references to the device. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

14.2.16.1 QADC Analog Reference (VRH, VRL)

These signals serve as the high (VRH) and low (VRL) reference potentials for the analog converter in the QADC.

14.2.16.2 QADC Analog Supply (VDDA, VSSA)

These are dedicated power supply signals to isolate the sensitive QADC analog circuitry from the normal levels of noise present on the digital power supply.

14.2.16.3 PLL Analog Supply (VDDPLL, VSSPLL)

These are dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.

14.2.16.4 QADC Positive Supply (VDDH)

This pin supplies positive power to the ESD structures in the QADC pads.

14.2.16.5 Power for Flash Erase/Program (VPP)

This pin is used for Flash stress testing and can be left unconnected in normal device operation.

14.2.16.6 Power and Ground for Flash Array (VDDF, VSSF)

These signals supply a power and ground to the Flash array.

14.2.16.7 Standby Power (VSTBY)

This pin is used to provide standby voltage to the RAM array if VDD is lost.

14.2.16.8 Positive Supply (VDD)

This pin supplies positive power to the core logic and I/O pads.

14.2.16.9 Ground (VSS)

This pin is the negative supply (ground) to the chip.

Table 15-25. SDRAM Example Specifications

Parameter	Specification
Speed grade (-8E)	40 MHz (25-ns period)
10 rows, 8 columns	
Two bank-select lines to access four internal banks	
ACTV-to-read/write delay (t_{RCD})	20 ns (min.)
Period between auto-refresh and ACTV command (t_{RC})	70 ns
ACTV command to precharge command (t_{RAS})	48 ns (min.)
Precharge command to ACTV command (t_{RP})	20 ns (min.)
Last data input to PALL command (t_{RWL})	1 bus clock (25 ns)
Auto-refresh period for 4096 rows (t_{REF})	64 mS

NOTE

Throughout this chapter “external request” and DREQ are used to refer to a DMA request from one of the on-chip UARTS or DMA timers. For details on the connections associated with DMA request inputs, see Section 16.2, “DMA Request Control (DMAREQC).”

16.1.1 DMA Module Features

The DMA controller module features are as follows:

- Four independently programmable DMA controller channels
- Auto-alignment feature for source or destination accesses
- Dual-address transfers
- Channel arbitration on transfer boundaries
- Data transfers in 8-, 16-, 32-, or 128-bit blocks using a 16-byte buffer
- Continuous-mode or cycle-steal transfers
- Independent transfer widths for source and destination
- Independent source and destination address registers

16.2 DMA Request Control (DMAREQC)

The DMAREQC register provides a software-controlled connection matrix for DMA requests. It logically routes DMA requests from the DMA timers and UARTs to the four channels of the DMA controller. Writing to this register determines the exact routing of the DMA request to the four channels of the DMA modules. If DCR*n*[EEXT] is set and the channel is idle, the assertion of the appropriate DREQ*n* activates channel *n*.

	31 … 20	19 … 16
Field	—	—
Reset	0000_0000_0000_0000	
R/W	R/W	

	15 … 12	11 … 8	7 … 4	3 … 0
Field	DMAC3	DMAC2	DMAC1	DMAC0
Reset	0000_0000_0000_0000			
R/W	R/W			
	IPSBAR + 0x014			

Figure 16-2. DMA Request Control Register (DMAREQC)

Table 16-1. DMAREQC Field Description

Bits	Name	Description

Table 17-35. MII Mode (continued)

Signal Description	EMAC pin
Collision	FEC_COL
Carrier Sense	FEC_CRS
Receive Clock	FEC_RXCLK
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[3:0]
Receive Error	FEC_RXER
Management Data Clock	FEC_MDC
Management Data Input/Output	FEC_MDIO

The 7-wire serial mode interface (RCR[MII_MODE] cleared) is generally referred to as AMD mode. Table 17-36 shows the 7-wire mode connections to the external transceiver.

Table 17-36. 7-Wire Mode Configuration

Signal description	EMAC Pin
Transmit Clock	FEC_TXCLK
Transmit Enable	FEC_TXEN
Transmit Data	FEC_TXD[0]
Collision	FEC_COL
Receive Clock	FEC_RXCLK
Receive Data Valid	FEC_RXDV
Receive Data	FEC_RXD[0]

17.5.7 FEC Frame Transmission

The Ethernet transmitter is designed to work with almost no intervention from software. After ECR[ETHER_EN] is set and data appears in the transmit FIFO, the Ethernet MAC can transmit onto the network. The Ethernet controller transmits bytes least significant bit (lsb) first.

When the transmit FIFO fills to the watermark (defined by TFWR), MAC transmit logic asserts FEC_TXEN and starts transmitting the preamble (PA) sequence, the start frame delimiter (SFD), and then the frame information from the FIFO. However, the controller defers the transmission if the network is busy (FEC_CRS is asserted). Before transmitting, the controller waits for carrier sense to become inactive, then determines if carrier sense stays inactive for 60 bit times. If so, transmission begins after waiting an additional 36 bit times (96 bit times after carrier sense originally became inactive). See Section 17.5.15.1, “Transmission Errors,” for more details.

Table 18-3. WCR Field Descriptions

Bit(s)	Name	Description
15–4	—	Reserved, should be cleared.
3	WAIT	Wait mode bit. Controls the function of the watchdog timer in wait mode. Once written, the WAIT bit is not affected by further writes except in halted mode. Reset sets WAIT. 1 Watchdog timer stopped in wait mode 0 Watchdog timer not affected in wait mode
2	DOZE	Doze mode bit. Controls the function of the watchdog timer in doze mode. Once written, the DOZE bit is not affected by further writes except in halted mode. Reset sets DOZE. 1 Watchdog timer stopped in doze mode 0 Watchdog timer not affected in doze mode
1	HALTED	Halted mode bit. Controls the function of the watchdog timer in halted mode. Once written, the HALTED bit is not affected by further writes except in halted mode. During halted mode, watchdog timer registers can be written and read normally. When halted mode is exited, timer operation continues from the state it was in before entering halted mode, but any updates made in halted mode remain. If a write-once register is written for the first time in halted mode, the register is still writable when halted mode is exited. 1 Watchdog timer stopped in halted mode 0 Watchdog timer not affected in halted mode Note: Changing the HALTED bit from 1 to 0 during halted mode starts the watchdog timer. Changing the HALTED bit from 0 to 1 during halted mode stops the watchdog timer.
0	EN	Watchdog enable bit. Enables the watchdog timer. Once written, the EN bit is not affected by further writes except in halted mode. When the watchdog timer is disabled, the watchdog counter and prescaler counter are held in a stopped state. 1 Watchdog timer enabled 0 Watchdog timer disabled

18.5.2.2 Watchdog Modulus Register (WMR)

	15	14	13	12	11	10	9	8
Field	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8
Reset	1111_1111							
R/W	R/W							

	7	6	5	4	3	2	1	0
Field	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
Reset	1111_1111							
R/W	R/W							
Address	IPSBAR + 0x0014_0002, 0x0014_0003							

Figure 18-3. Watchdog Modulus Register (WMR)

Table 18-4. WMR Field Descriptions

Bit(s)	Name	Description
15–0	WM	Watchdog modulus. Contains the modulus that is reloaded into the watchdog counter by a service sequence. Once written, the WM[15:0] field is not affected by further writes except in halted mode. Writing to WMR immediately loads the new modulus value into the watchdog counter. The new value is also used at the next and all subsequent reloads. Reading WMR returns the value in the modulus register. Reset initializes the WM[15:0] field to 0xFFFF. Note: The prescaler counter is reset anytime a new value is loaded into the watchdog counter and also during reset.

18.5.2.3 Watchdog Count Register (WCNTR)

	15	14	13	12	11	10	9	8
Field	WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
Reset	1111_1111							
R/W	R							

	7	6	5	4	3	2	1	0
Field	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
Reset	1111_1111							
R/W	R							
Address	IPSBAR + x0014_0004, 0x0014_0005							

Figure 18-4. Watchdog Count Register (WCNTR)

Table 18-5. WCNTR Field Descriptions

Bit(s)	Name	Description
15–0	WC	Watchdog count field. Reflects the current value in the watchdog counter. Reading the 16-bit WCNTR with two 8-bit reads is not guaranteed to return a coherent value. Writing to WCNTR has no effect, and write cycles are terminated normally.

18.5.2.4 Watchdog Service Register (WSR)

When the watchdog timer is enabled, writing 0x5555 and then 0xAAAA to WSR before the watchdog counter times out prevents a reset. If WSR is not serviced before the timeout, the watchdog timer sends a signal to the reset controller module that sets the RSR[WDR] bit and asserts a system reset.

Both writes must occur in the order listed before the timeout, but any number of instructions can be executed between the two writes. However, writing any value other than 0x5555 or 0xAAAA to WSR resets the servicing sequence, requiring both values to be written to keep the watchdog timer from causing a reset.

When the PCSR*n*[OVW] bit is set, counter can be directly initialized by writing to PMR*n* without having to wait for the count to reach 0x0000.

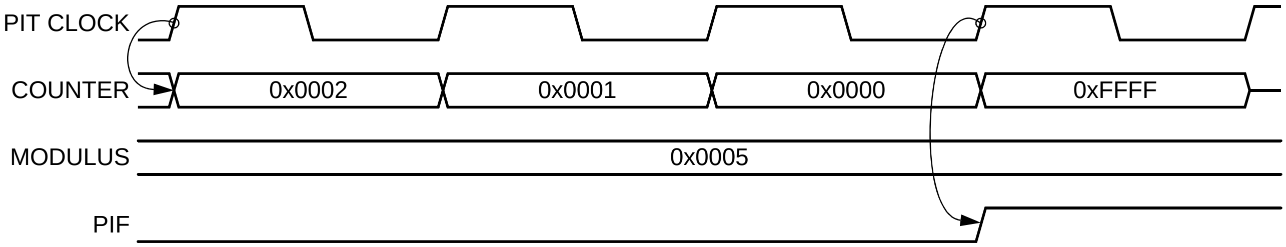

Figure 19-6. Counter in Free-Running Mode

19.3.3 Timeout Specifications

The 16-bit PIT counter and prescaler supports different timeout periods. The prescaler divides the internal bus clock period as selected by the PCSR*n*[PRE] bits. The PMR*n*[PM] bits select the timeout period.

$$\text{Timeout period} = \frac{2^{\text{PCSRn[PRE]}} \times (\text{PMRn[PM]} + 1)}{f_{sys}} \qquad \textit{Eqn. 19-1}$$

19.3.4 Interrupt Operation

Table 19-6 shows the interrupt request generated by the PIT.

Table 19-6. PIT Interrupt Requests

Interrupt Request	Flag	Enable Bit
Timeout	PIF	PIE

The PIF flag is set when the PIT counter reaches 0x0000. The PIE bit enables the PIF flag to generate interrupt requests. Clear PIF by writing a 1 to it or by writing to the PMR.

21.2.2 DMA Timer Extended Mode Registers (DTXMR*n*)

The DTXMR*n* registers program DMA request and increment modes for the timers.

IPSBAR Offset: 0x00_0402 (DTXMR0)
0x00_0442 (DTXMR1)
0x00_0482 (DTXMR2)
0x00_04C2 (DTXMR3)

Access: User read/write

	7	6	5	4	3	2	1	0
R	DMAEN	0	0	0	0	0	0	MODE16
W								
Reset:	0	0	0	0	0	0	0	0

Figure 21-3. DTXMR*n* Registers

Table 21-3. DTXMR*n* Field Descriptions

Field	Description
7 DMAEN	DMA request. Enables DMA request output on counter reference match or capture edge event. 0 DMA request disabled 1 DMA request enabled
6–1	Reserved, must be cleared.
0 MODE16	Selects the increment mode for the timer. Setting MODE16 is intended to exercise the upper bits of the 32-bit timer in diagnostic software without requiring the timer to count through its entire dynamic range. When set, the counter's upper 16 bits mirror its lower 16 bits. All 32 bits of the counter remain compared to the reference value. 0 Increment timer by 1 1 Increment timer by 65,537

21.2.3 DMA Timer Event Registers (DTER*n*)

DTER*n*, shown in Figure 21-4, reports capture or reference events by setting DTER*n*[CAP] or DTER*n*[REF]. This reporting happens regardless of the corresponding DMA request or interrupt enable values, DTXMR*n*[DMAEN] and DTMR*n*[ORRI,CE].

Writing a 1 to DTER*n*[REF] or DTER*n*[CAP] clears it (writing a 0 does not affect bit value); both bits can be cleared at the same time. If configured to generate an interrupt request, clear REF and CAP early in the interrupt service routine so the timer module can negate the interrupt request signal to the interrupt controller. If configured to generate a DMA request, processing of the DMA data transfer automatically clears the REF and CAP flags via the internal DMA ACK signal.

IPSBAR Offset: 0x00_0304 (I2FDR)

Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	IC					
W								
Reset:	0	0	0	0	0	0	0	0

Figure 24-3. I^2C Frequency Divider Register (I2FDR)

Table 24-3. I2FDR Field Descriptions

Field	Description
7–6	Reserved, must be cleared.
5–0 IC	I^2C clock rate. Prescales the clock for bit-rate selection. The serial bit clock frequency is equal to the internal bus clock divided by the divider shown below. Due to potentially slow I2C_SCL and I2C_SDA rise and fall times, bus signals are sampled at the prescaler frequency.

IC	Divider	IC	Divider	IC	Divider	IC	Divider
0x00	28	0x10	288	0x20	20	0x30	160
0x01	30	0x11	320	0x21	22	0x31	192
0x02	34	0x12	384	0x22	24	0x32	224
0x03	40	0x13	480	0x23	26	0x33	256
0x04	44	0x14	576	0x24	28	0x34	320
0x05	48	0x15	640	0x25	32	0x35	384
0x06	56	0x16	768	0x26	36	0x36	448
0x07	68	0x17	960	0x27	40	0x37	512
0x08	80	0x18	1152	0x28	48	0x38	640
0x09	88	0x19	1280	0x29	56	0x39	768
0x0A	104	0x1A	1536	0x2A	64	0x3A	896
0x0B	128	0x1B	1920	0x2B	72	0x3B	1024
0x0C	144	0x1C	2304	0x2C	80	0x3C	1280
0x0D	160	0x1D	2560	0x2D	96	0x3D	1536
0x0E	192	0x1E	3072	0x2E	112	0x3E	1792
0x0F	240	0x1F	3840	0x2F	128	0x3F	2048

24.2.3 I^2C Control Register (I2CR)

I2CR enables the I^2C module and the I^2C interrupt. It also contains bits that govern operation as a slave or a master.

24.3.8 Handshaking and Clock Stretching

The clock synchronization mechanism can acts as a handshake in data transfers. Slave devices can hold I2C_SCL low after completing one byte transfer. In such a case, the clock mechanism halts the bus clock and forces the master clock into wait states until the slave releases I2C_SCL.

Slaves may also slow down the transfer bit rate. After the master has driven I2C_SCL low, the slave can drive I2C_SCL low for the required period and then release it. If the slave I2C_SCL low period is longer than the master I2C_SCL low period, the resulting I2C_SCL bus signal low period is stretched.

24.4 Initialization/Application Information

The following examples show programming for initialization, signaling START, post-transfer software response, signaling STOP, and generating a repeated START.

24.4.1 Initialization Sequence

Before the interface can transfer serial data, registers must be initialized:

1. Set I2FDR[IC] to obtain I2C_SCL frequency from the system bus clock. See Section 24.2.2, “I^{2}C Frequency Divider Register (I2FDR).”
2. Update the I2ADR to define its slave address.
3. Set I2CR[IEN] to enable the I^{2}C bus interface system.
4. Modify the I2CR to select or deselect master/slave mode, transmit/receive mode, and interrupt-enable or not.

NOTE

If I2SR[IBB] is set when the I^{2}C bus module is enabled, execute the following pseudocode sequence before proceeding with normal initialization code. This issues a STOP command to the slave device, placing it in idle state as if it were power-cycled on.

```
I2CR = 0x0
I2CR = 0xA0
dummy read of I2DR
I2SR = 0x0
I2CR = 0x0
I2CR = 0x80       ; re-enable
```

24.4.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the master transmitter mode. On a multiple-master bus system, I2SR[IBB] must be tested to determine whether the serial bus is free. If the bus is free (IBB is cleared), the START signal and the first byte (the slave address) can be sent. The data written to the data register comprises the address of the desired slave and the lsb indicates the transfer direction.

The free time between a STOP and the next START condition is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system clock and the I2C_SCL period, the

28.4.1.1 Port QA Analog Input Signals

When used as analog inputs, the four port QA signals are referred to as AN[56:55, 53:52].

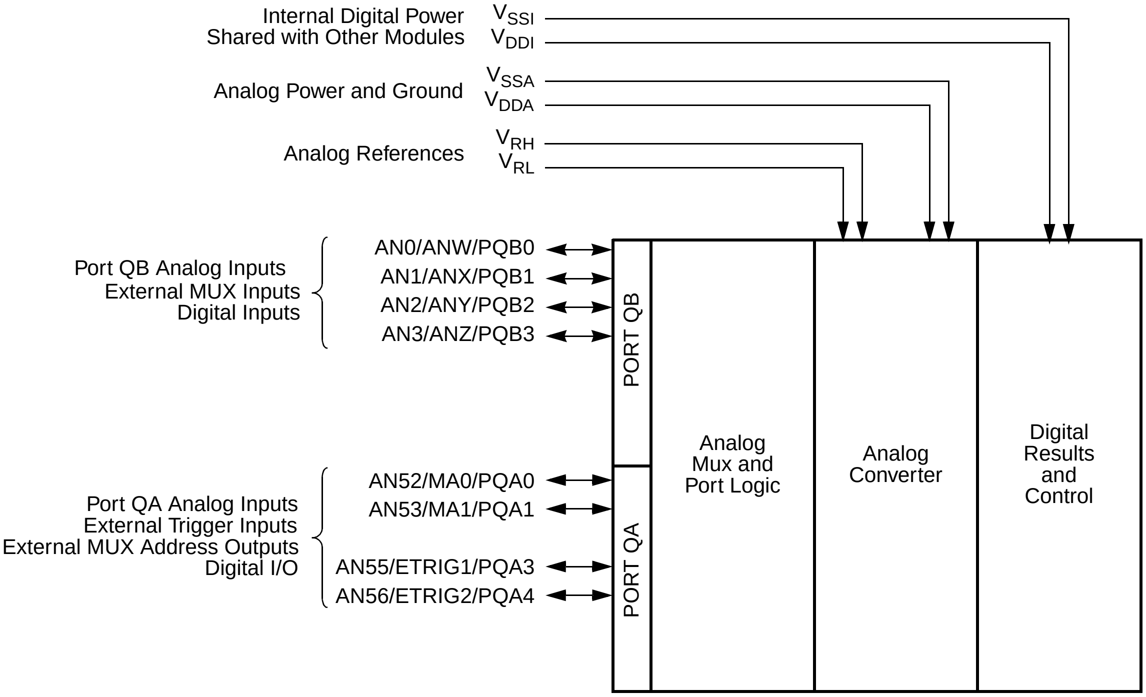

Figure 28-2. QADC Input and Output Signals

28.4.1.2 Port QA Digital Input/Output Signals

Port QA signals are referred to as PQA[4:3, 1:0] when used as a bidirectional 4-bit digital input/output port. These four signals may be used for general-purpose digital input or digital output.

Port QA signals are connected to a digital input synchronizer during reads and may be used as general-purpose digital inputs when the applied voltages meet high-voltage input (V_{IH}) and low-voltage input (V_{IL}) requirements.

Each port QA signal is configured as an input or output by programming the port data direction register (DDRQA). The digital input signal states are read from the port QA data register (PORTQA) when DDRQA specifies that the signals are inputs. The digital data in PORTQA is driven onto the port QA signals when the corresponding bits in DDRQA specify output. See Section 28.6.4, “Port QA and QB Data Direction Register (DDRQA & DDRQB).

28.4.2 Port QB Signal Functions

The four port QB signals can be used as analog inputs or as a 4-bit digital I/O port.

28.4.2.1 Port QB Analog Input Signals

When used as analog inputs, the four port QB signals are referred to as AN[3:0].

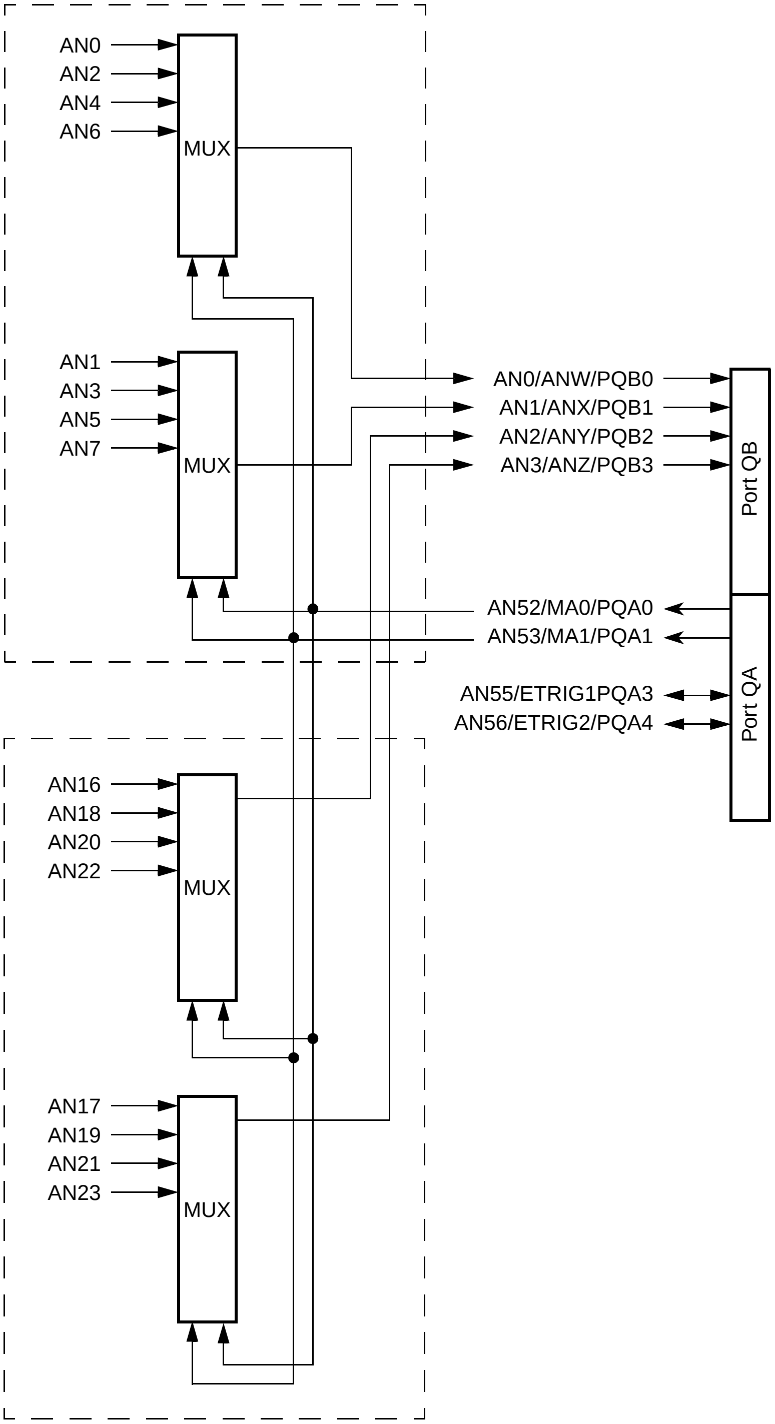

Figure 28-18. External Multiplexing Configuration

When externally multiplexed mode is selected, the QADC automatically drives the MA output signals from the channel number in each CCW. The QADC also converts the proper input channel (ANW, ANX, ANY, and ANZ) by interpreting the CCW channel number. As a result, up to 16 externally multiplexed channels appear to the conversion queues as directly connected signals. User software simply puts the channel number of externally multiplexed channels into CCWs.

NOTE

> The debug module has no hardware interlocks, so to prevent spurious breakpoint triggers while the breakpoint registers are being loaded, disable TDR (by clearing TDR[29,13]) before defining triggers.

A write to TDR clears the CSR trigger status bits, CSR[BSTAT].

Second-Level Trigger

	31 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	TRC	EBL	EDLW	EDWL	EDWU	EDLL	EDLM	EDUM	EDUU	DI	EAI	EAR	EAL	EPC	PCI
Reset	0000_0000_0000_0000														

First-Level Trigger

	15 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	LxT	EBL	EDLW	EDWL	EDWU	EDLL	EDLM	EDUM	EDUU	DI	EAI	EAR	EAL	EPC	PCI
Reset	0000_0000_0000_0000														
R/W	Write only. Accessible in supervisor mode as debug control register 0x07 using the WDEBUG instruction and through the BDM port using the WDMREG command.														
DRc[4–0]	0x07														

Figure 30-11. Trigger Definition Register (TDR)

Table 30-14 describes TDR fields.

Table 30-14. TDR Field Descriptions

Bits	Name	Description
31–30	TRC	Trigger response control. Determines how the processor responds to a completed trigger condition. The trigger response is always displayed on DDATA. 00 Display on DDATA only 01 Processor halt 10 Debug interrupt 11 Reserved
15–14	LxT	Level-x trigger. This is a Rev. B function only. The Level-x Trigger bit determines the logic operation for the trigger between the PC_condition and the (Address_range & Data_condition) where the inclusion of a Data condition is optional. The ColdFire debug architecture supports the creation of single or double-level triggers. TDR[15] 0 Level-2 trigger = PC_condition & Address_range & Data_condition 1 Level-2 trigger = PC_condition | (Address_range & Data_condition) TDR[14] 0 Level-1 trigger = PC_condition & Address_range & Data_condition 1 Level-1 trigger = PC_condition | (Address_range & Data_condition)
29/13	EBL	Enable breakpoint. Global enable for the breakpoint trigger. Setting TDR[EBL] enables a breakpoint trigger. Clearing it disables all breakpoints at that level.

Table 32-1. Signal Description by Pin Number (continued)

MAPBGA Pin	Pin Functions			MAPBGA Pin	Pin Functions		
	Primary	Secondary	Tertiary		Primary	Secondary	Tertiary
G12	VDD	—	—	R12	GPTB2	PTB2	—
G13	QSPI_CS2	PQS5	—	R13	GPTA2	PTA2	—
G14	QSPI_CS3	PQS6	—	R14	CLKMOD0	—	—
G15	$\overline{\mathrm{DRAMW}}$	PSD3	—	R15	$\overline{\mathrm{BS1}}$	PJ5	—
G16	$\overline{\mathrm{SDRAM\_CS0}}$	PSD1	—	R16	$\overline{\mathrm{BS0}}$	PJ4	—
H1	D26	PA2	—	T1	VSSA	—	—
H2	D25	PA1	—	T2	AN2	PQB2	ANY
H3	D24	PA0	—	T3	AN0	PQB0	ANW
H4	D23	PB7	—	T4	AN53	PQA1	MA1
H5	VDD	—	—	T5	VRL	—	—
H6	VDD	—	—	T6	D2	PD2	—
H7	VSS	—	—	T7	UTXD0	PUA0	—
H8	VSS	—	—	T8	EXTAL	—	—
H9	VSS	—	—	T9	TCLK	—	—
H10	VSS	—	—	T10	DSO	TDO	—
H11	VDD	—	—	T11	$\overline{\mathrm{RCON}}$	—	—
H12	VDD	—	—	T12	GPTB3	PTB3	—
H13	$\overline{\mathrm{SDRAM\_CS1}}$	PSD2	—	T13	GPTA3	PTA3	—
H14	SCKE	PSD0	—	T14	CLKMOD1	—	—
H15	$\overline{\mathrm{SRAS}}$	PSD5	—	T15	$\overline{\mathrm{BS2}}$	PJ6	—
H16	$\overline{\mathrm{SCAS}}$	PSD4	—	T16	VSS	—	—

[1] NC = no connect