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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c31b0agn20000

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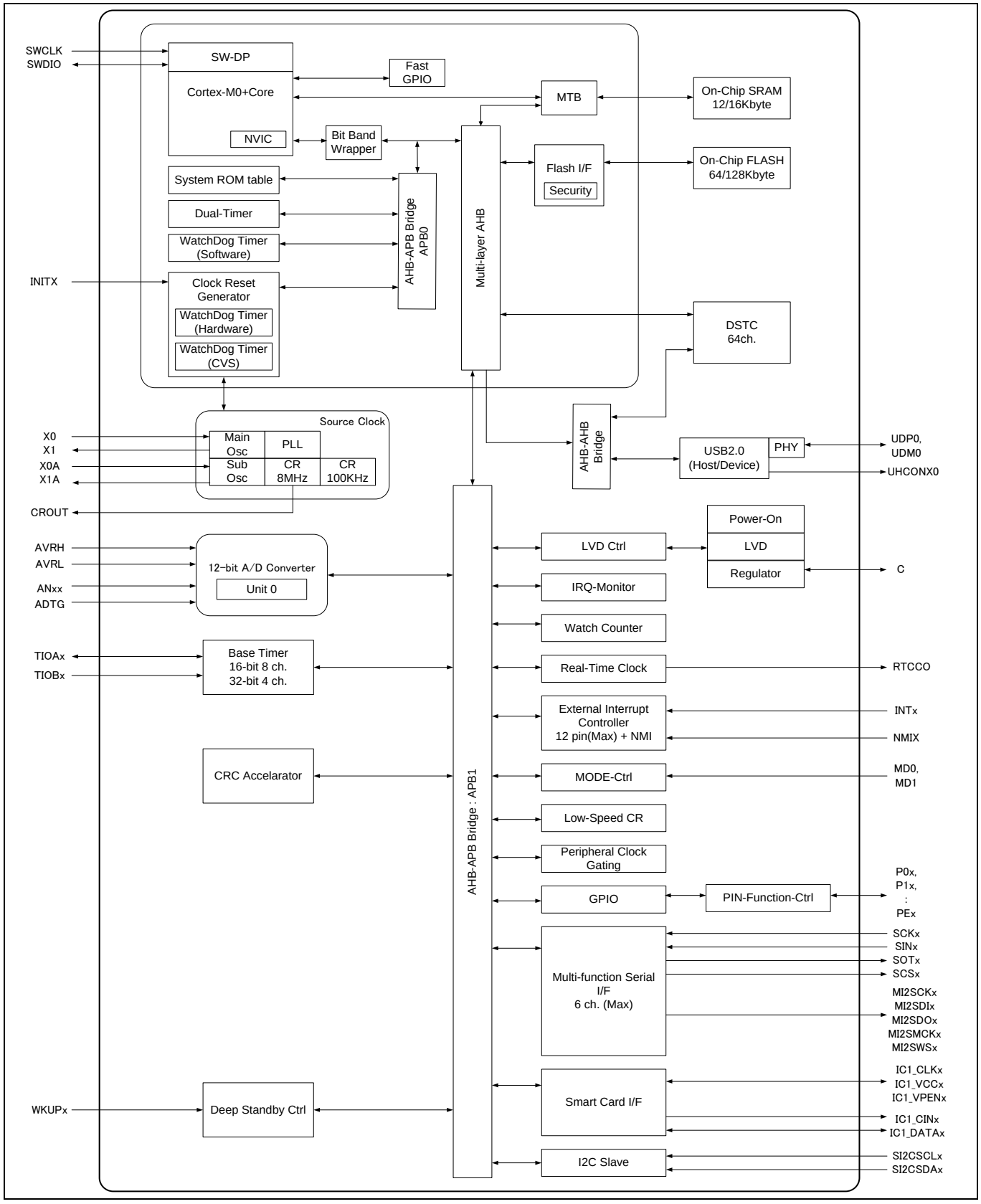
1. Block Diagram



5. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	Alternate Functions					I/O Circuit Type	Pin State Type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32								
1	1	2	P50	SIN3_1	INT00_0				D	K
2	2	3	P51	SOT3_1	INT01_0				D	K
3	3	4	P52	SCK3_1	INT02_0				D	K
4	4	-	P53	TIOA1_2	INT07_2				D	K
5	5	-	P30	SCS60_1	TIOB0_1	INT03_2	MI2SWS6_1		D	K
6	6	-	P31	SCK6_1	SI2CSCL6_1	INT04_2	MI2SCK6_1		H	K
-	-	5	P31	SCK6_1	SI2CSCL6_1	INT04_2			H	K
7	7	-	P32	SOT6_1	SI2CSDA6_1	TIOB2_1	INT05_2	MI2SDO6_1	H	K
-	-	6	P32	SOT6_1	SI2CSDA6_1	TIOB2_1	INT05_2		H	K
8	8	-	P33	ADTG_6	SIN6_1	INT04_0	MI2SDI6_1		H	K
-	-	7	P33	ADTG_6	SIN6_1	INT04_0			H	K
9	-	-	P34	SCS61_1	TIOB4_1	MI2SMCK6_1			D	K
-	9	-	P34	SCS61_1	MI2SMCK6_1				D	K
10	-	-	P35	SCS62_1	TIOB5_1	INT08_1			D	K
11	-	-	P3A	TIOA0_1	INT03_0	RTCCO_2	SUBOUT_2	IC1_CIN_0	D	K
-	10	-	P3A	TIOA0_1	INT03_0	RTCCO_2	SUBOUT_2		D	K
12	-	-	P3B	TIOA1_1	IC1_DATA_0				D	K
-	11	-	P3B	TIOA1_1					D	K
13	-	-	P3C	TIOA2_1	IC1_RST_0				D	K
-	12	-	P3C	TIOA2_1					D	K
14	-	-	P3D	TIOA3_1	IC1_VPEN_0				D	K
15	-	-	P3E	TIOA4_1	IC1_VCC_0				D	K
16	-	-	P3F	TIOA5_1	IC1_CLK_0				D	K
17	13	8	MD0						I	F
18	14	9	PE2	X0					A	A
19	15	10	PE3	X1					A	B
20	-	-	P40	TIOA0_0	INT12_1				D	K
21	-	-	P41	TIOA1_0	INT13_1				D	K
22	-	-	P42	TIOA2_0					D	K
23	-	-	P43	ADTG_7	TIOA3_0				D	K
24	-	-	P4C	SCK7_1	TIOB3_0				D	K
-	16	-	P4C	SCK7_1					D	K
25	17	-	P4D	SOT7_1					D	K
26	18	-	P4E	SIN7_1	INT06_2				D	K
27	19	11	VCC						-	-
28	20	12	C						-	-
29	21	13	VSS						-	-
30	22	14	P46	X0A					C	C
31	23	15	P47	X1A					C	D

Pin No.			Pin Name	Alternate Functions					I/O Circuit Type	Pin State Type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32								
32	24	16	INITX						B	E
33	25	17	P60	TIOA2_2	INT15_1	CEC1_0			H	K
34	-	-	P1E	RTS4_1	MI2SMCK4_1				D	K
35	-	-	P1D	CTS4_1	MI2SWS4_1				D	K
36	-	-	P1C	SCK4_1	MI2SCK4_1				D	K
37	-	-	P1B	SOT4_1	MI2SDO4_1				D	K
-	26	-	P1B	SOT4_1					D	K
38	-	-	P1A	SIN4_1	INT05_1	CEC0_0	MI2SDI4_1		H	K
-	27	-	P1A	SIN4_1	INT05_1	CEC0_0			H	K
39	-	-	P1F	ADTG_5					D	K
40	28	18	P10	AN00					F	J
41	29	19	P11	AN01	SIN1_1	INT02_1	WKUP1		G	J
42	30	20	P12	AN02	SOT1_1				F	J
43	31	21	P13	AN03	SCK1_1	RTCCO_1	SUBOUT_1		F	J
44	32	-	P14	AN04	SIN0_1	SCS10_1	INT03_1		F	J
45	33	-	P15	AN05	SOT0_1	SCS11_1			F	J
46	34	22	P23	AN06	SCK0_0	TIOA7_1			F	J
47	35	23	P22	AN07	TIOB7_1				F	J
48	36	24	VCC						-	-
49	37	-	AVRH[1]						-	-
50	38	25	AVRL						-	-
51	39	26	P21	INT06_1	WKUP2				E	K
52	-	-	P00	WKUP4					E	K
53	40	27	P01	SWCLK	SOT0_0				D	K
54	-	-	P02	WKUP5					E	K
55	41	28	P03	SWDIO	SIN0_0	TIOB7_0			D	K
56	42	29	P05	MD1	TIOA5_2	INT00_1	WKUP3		E	K
57	43	-	VCC						-	-
58	44	30	P80	UDM0					J	G
59	45	31	P81	UDP0					J	G
60	46	32	VSS						-	-
61	47	-	P61	UHCONX0	TIOB2_2				H	K
62	-	-	P0B	TIOB6_1	WKUP6				E	K
63	-	-	P0C	TIOA6_1	WKUP7				E	K
64	48	1	P0F	NMIX	WKUP0	RTCCO_0	SUBOUT_0	CROUT_1	E	I

[1] In a 32-pin package, the AVRH pin is internally connected to the V_{CC} pin.

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	41	29	19
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I^2C pin (operation mode 4).	42	30	20
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I^2C pin (operation mode 4).	43	31	21
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 input/output pin.	44	32	-
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	45	33	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	1	1	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I^2C pin (operation mode 4).	2	2	3
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I^2C pin (operation mode 4).	3	3	4
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I^2C pin (operation mode 4).	37	26	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I^2C pin (operation mode 4).	36	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should mount only under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VCC →AVRH
Turning off : AVRH →VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

Type	Selected Pin Function		CPU State							
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS
K	Digital I/O selected	CEC pin selected	-	-	CP	CP	CP	CP	CP	CP
		WKUP enable and input selected	-	-	IP	IP	IP	IP	IP	IP
		I2CSLAVE enable selected	-	-	PC	HC	IP	GS	IS	GS
		External interrupt enable and input selected	-	-	PC	HC	IP	GS	IS	GS
		GPIO selected	IS	IE	PC	HC	IS	HS	IS	HS
		Resource other than above selected	-	-	PC	HC	IS	GS	IS	GS

Terms in the table above have the following meanings.

Type
This indicates a pin status type that is shown in “pin list table” in “5. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1) Reset state. CPU is initialized by Power-on reset or a reset due to low Power voltage supply.

(2) Reset state. CPU is initialized by INITX input signal or system initialization after power on reset.

(3) Run mode or SLEEP mode state.

(4) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

(5) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

(6) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"

(7) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"

(8) Run mode state after returning from Deep Standby mode.
(I/O state hold function(CONTX) is fixed at 1)

11.3 DC Characteristics

11.3.1 Current Rating

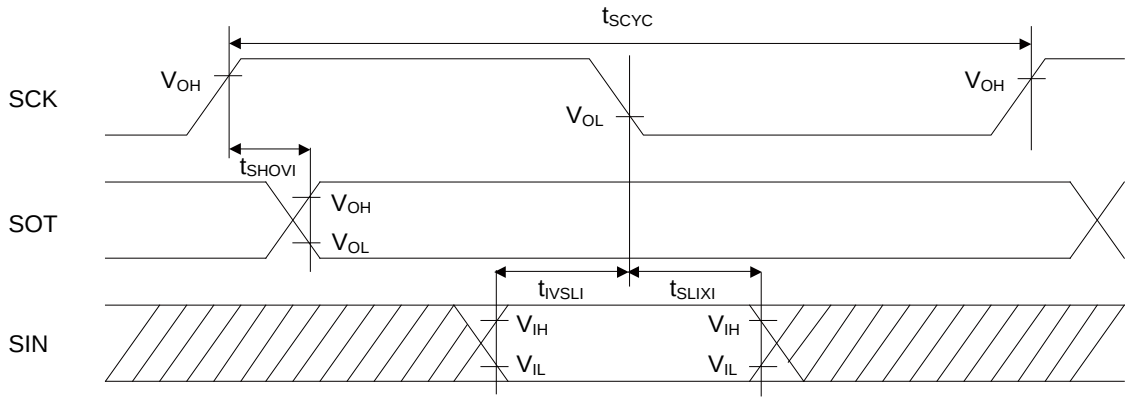
Symbol (Pin Name)	Conditions		HCLK Frequency[19]	Value Typ[20]	Value Max[21]	Unit	Remarks
Icc (VCC)	Run mode, code executed from Flash	8 MHz external clock input, PLL ON[22] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	8 MHz	1.4	2.7	mA	[23]
			20 MHz	2.6	4.1		
			40 MHz	3.9	5.6		
		8 MHz external clock input, PLL ON[22] Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	8 MHz	1.3	2.6	mA	[23]
			20 MHz	2.3	3.8		
			40 MHz	3.4	5.1		
		8 MHz crystal oscillation, PLL ON[22] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	8 MHz	1.6	3.0	mA	[23], [24],
			20 MHz	2.8	4.4		
			40 MHz	4.1	5.9		
	Run mode, code executed from RAM	8 MHz external clock input, PLL ON[22] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	8 MHz	1.0	2.1	mA	[23]
			20 MHz	1.7	2.9		
			40 MHz	2.7	4.0		
	Run mode, code executed from Flash	8 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHz	1.6	3.1	mA	[23], [25], [26]
	Run mode, code executed from Flash	Built-in high speed CR[27] NOP code executed All peripheral clock stopped by CKENx	8 MHz	1.1	2.4	mA	[23]
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHz	240	1264	µA	[23]
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHz	246	1271	µA	[23]
Iccs (VCC)	Sleep operation	8 MHz external clock input, PLL ON[22] All peripheral clock stopped by CKENx	8 MHz	0.8	1.9	mA	[23]
			20 MHz	1.3	2.4		
			40 MHz	1.8	3.0		
		Built-in high speed CR[27] All peripheral clock stopped by CKENx	8 MHz	0.6	1.7	mA	[23]
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	237	1261	µA	[23]
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	238	1262	µA	[23]

[19] PCLK0 is set to divided rate 8.
[20] T_A=+25°C,V_{CC}=3.3 V
[21] T_A=+105°C,V_{CC}=3.6 V
[22] When HCLK=8, PLL is off.
[23] All ports are fixed
[24] When IMAINSEL bit (MOSC_CTL:IMAINSEL) is “10” (default).
[25] Flash sync down is set to FRWTR.RWT=111 and FSYNDN.SD=1111
[26] VCC=1.65 V
[27] The frequency is set to 8 MHz by trimming

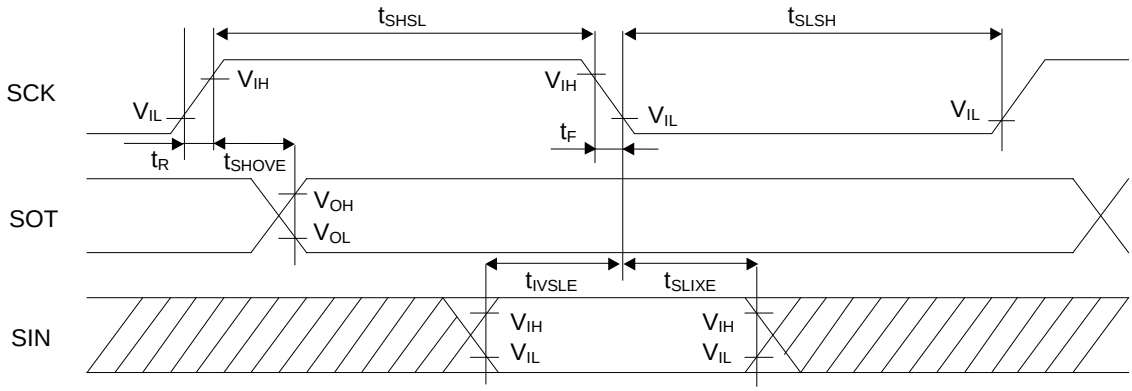
11.3.3 Pin Characteristics

(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{CC} +0.3	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	V_{SS} +5.5	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V		-	$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 2.7$ V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL}=2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	48	kΩ	
			$V_{CC} < 2.7$ V	-	-	88		
Input capacitance	C_{IN}	Other than VCC, VSS, AVRH	-	-	5	15	pF	



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

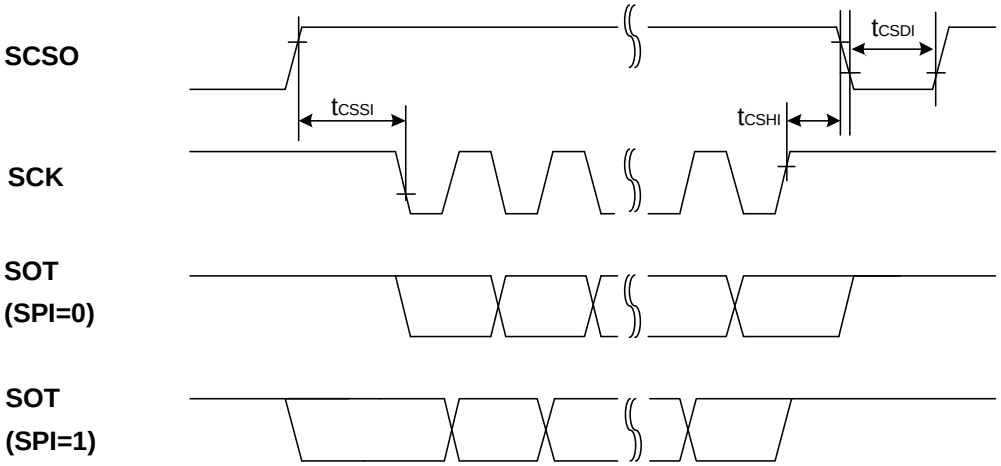
(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	-50[46]	+0[46]	-50[46]	+0[46]	ns
SCK↓→SCS↑ hold time	t_{CSHI}		+0[47]	+50[47]	+0[47]	+50[47]	ns
SCS deselect time	t_{CSDI}		-50[48]	+50[48]	-50[48]	+50[48]	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

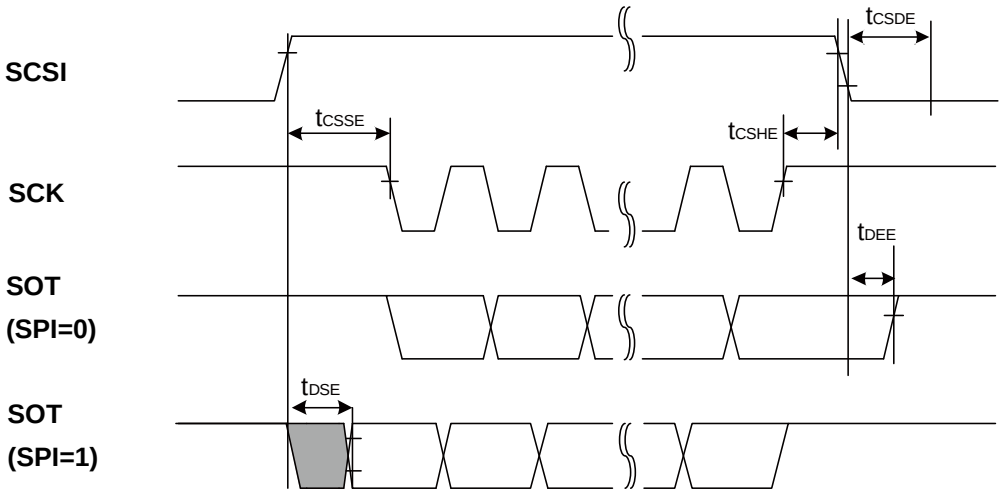
Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see the Peripheral Address Map.
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics guarantee only the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

[46] CSSU bit value × serial chip select timing operating clock cycle.
[47] CSHD bit value × serial chip select timing operating clock cycle.
[48] CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.



Master mode

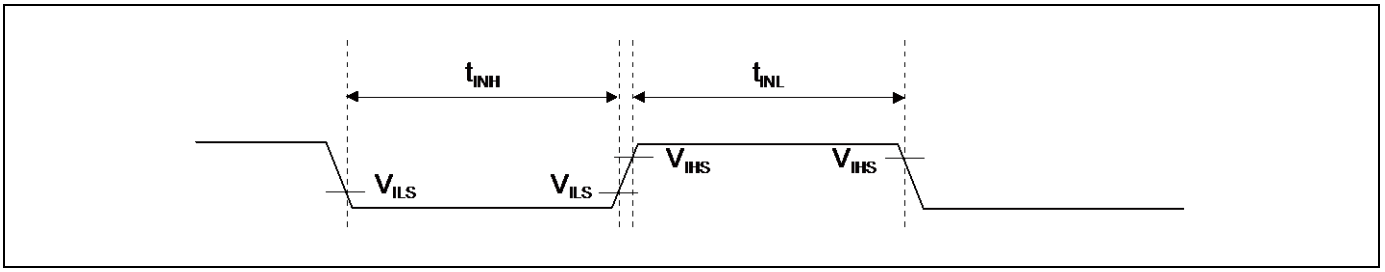


Slave mode

11.4.10 External Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}[55]	-	ns	A/D converter trigger input
		INT00 to INT08, INT12, INT13, INT15, NMIX	[56]	2 t_{CYCP} +100[55]	-	ns	External interrupt, NMI
			[57]	500	-	ns	
		WKUPx	[58]	500	-	ns	Deep standby wake up

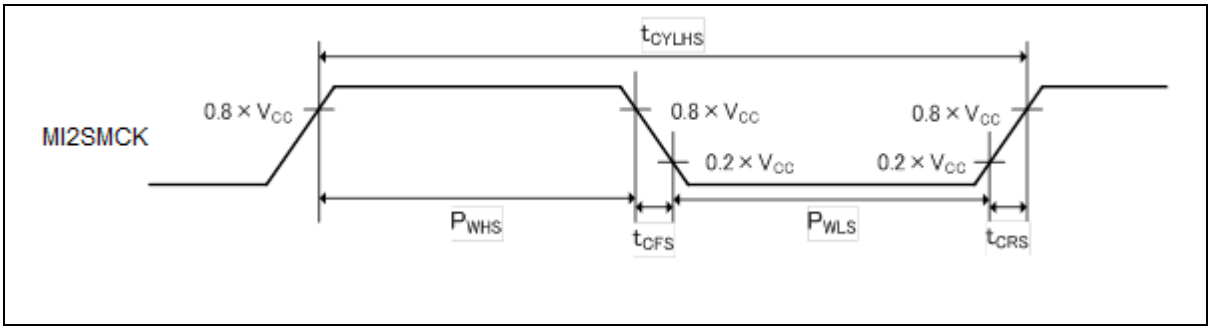


[55] t_{CYCP} indicates the APB bus clock cycle time. For the number of the APB bus to which the Base Timer has been connected, see the Peripheral Address Map.
[56] In Run mode and Sleep mode
[57] In Timer mode, RTC mode and Stop mode
[58] In Deep Standby RTC mode and Deep Standby Stop mode

MI2SMCK Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	MI2SMCK	-	-	12.288	MHz	
Input clock cycle	t_{CYLHS}	-	-	81.3	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



MI2SMCK Output Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	MI2SMCK	-	-	25	MHz	$V_{CC} \geq 2.7$ V
				-	20	MHz	$V_{CC} < 2.7$ V

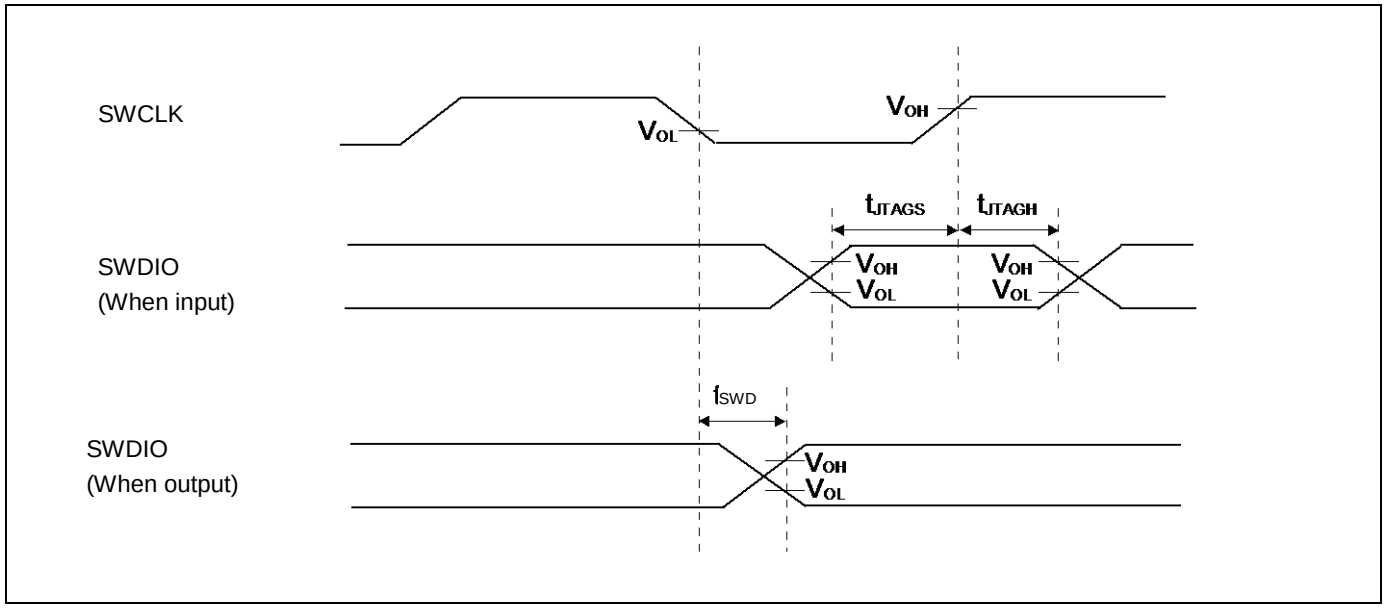
11.4.14 SW-DP Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

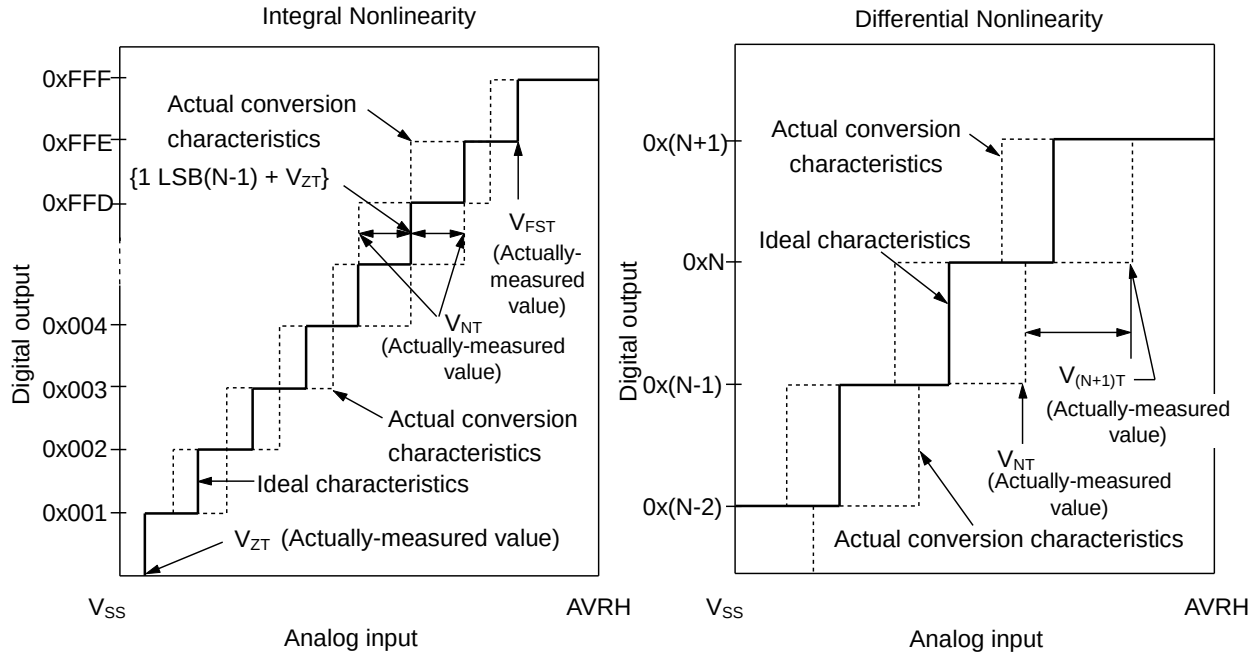
Note:

- *External load capacitance C_L=30 pF*



Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

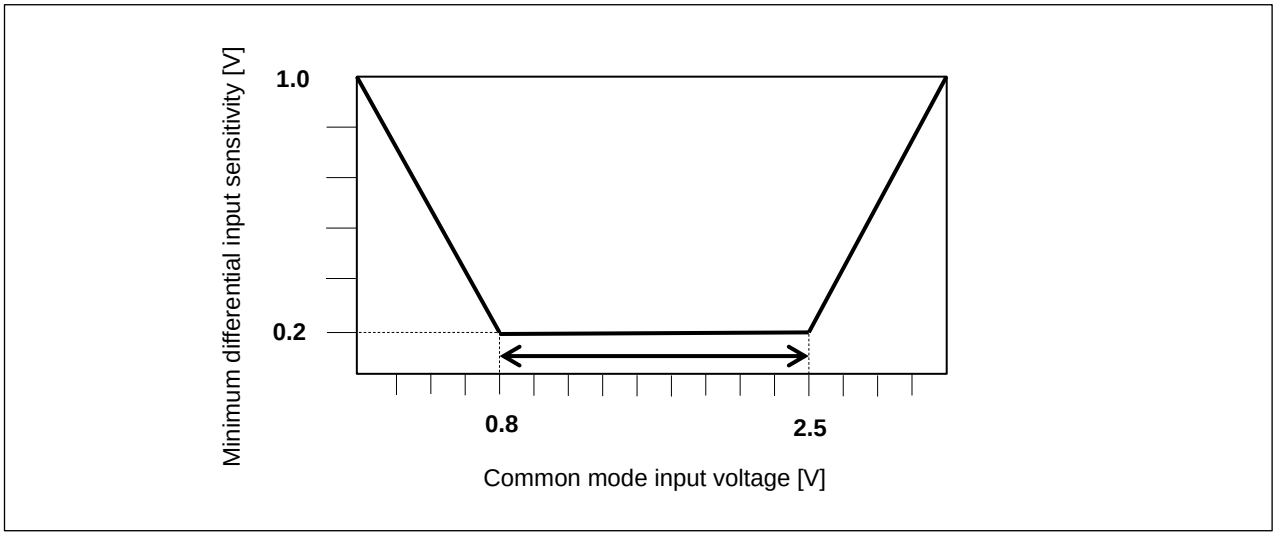
N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

11.6 USB Characteristics

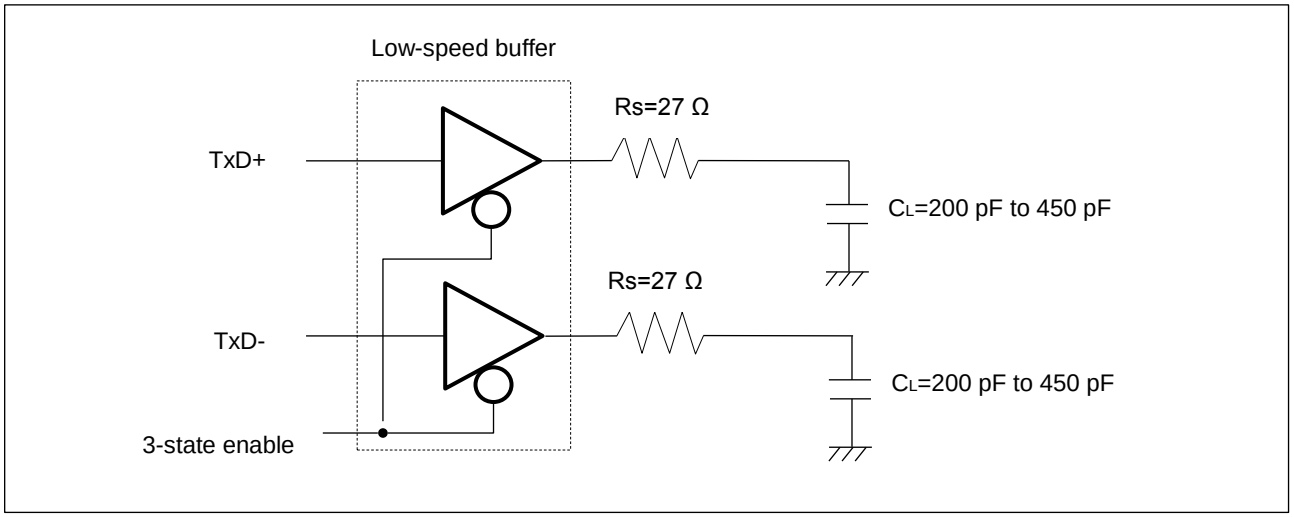
(V_{CC}=3.0 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Schematic Reference
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	V_{CC} + 0.3	V	1
	Input L level voltage	V_{IL}		-	V_{SS} – 0.3	0.8	V	1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	2
	Differential common mode range	V_{CM}		-	0.8	2.5	V	2
Output characteristic	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	4
	Rising time	t_{FR}		Full-speed	4	20	ns	5
	Falling time	t_{FF}		Full-speed	4	20	ns	5
	Rising/Falling time matching	t_{FRFM}		Full-speed	90	111.11	%	5
	Output impedance	Z_{DRV}		Full-speed	28	44	Ω	6
	Rising time	t_{LR}		Low-speed	75	300	ns	7
	Falling time	t_{LF}		Low-speed	75	300	ns	7
	Rising/Falling time matching	t_{LRFM}		Low-speed	80	125	%	7

1. The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V_{IL}(Max)=0.8 V, VIH(Min)=2.0 V (TTL input standard).
   There is some hysteresis to lower noise sensitivity.
2. Use differential-receiver to receive USB differential data signal.
   Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
   Above voltage range is the common mode input voltage range.



・Low-Speed Load (Compliance Load)



15. Errata

This chapter describes the errata for S6E1C product family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

15.1 Part Numbers Affected

Part Number
S6E1C32D0AGV20000, S6E1C32C0AGV20000, S6E1C32B0AGP20000, S6E1C32D0AGN20000, S6E1C32C0AGN20000, S6E1C32B0AGN20000
S6E1C31D0AGV20000, S6E1C31C0AGV20000, S6E1C31B0AGP20000, S6E1C31D0AGN20000, S6E1C31C0AGN20000, S6E1C31B0AGN20000
S6E1C12D0AGV20000, S6E1C12C0AGV20000, S6E1C12B0AGP20000, S6E1C12D0AGN20000, S6E1C12C0AGN20000, S6E1C12B0AGN20000
S6E1C11D0AGV20000, S6E1C11C0AGV20000, S6E1C11B0AGP20000, S6E1C11D0AGN20000, S6E1C11C0AGN20000, S6E1C11B0AGN20000

15.2 Qualification Status

Product Status: In Production − Qual.

15.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
[1] AHB Bus Matrix issue	Refer to 15.1	Rev B	Will be fixed in the next silicon

1. AHB Bus Matrix issue

■PROBLEM DEFINITION
The AHB Bus Matrix logic has two master interfaces (CPU and DSTC) and four slave interfaces (RAM, FLASH, AHB and APB). When two master interfaces (CPU and DSTC) access the same slave interface at the same time, and when the CPU is in wait cycle, an unnecessary access occurs during the wait cycle and the expected access occurs again after the unnecessary access.

■PARAMETERS AFFECTED
N/A

■TRIGGER CONDITION(S)
CPU and DSTC access the same slave interface at the same time.

■SCOPE OF IMPACT
DSTC cannot be used.

■WORKAROUND
DSTC must not use.

■FIX STATUS
This issue will be fixed in the next silicon revision.