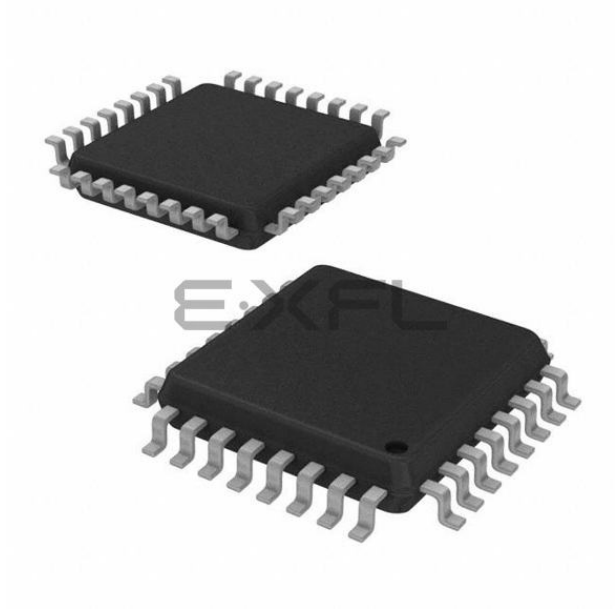

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What is "Embedded - Microcontrollers"?

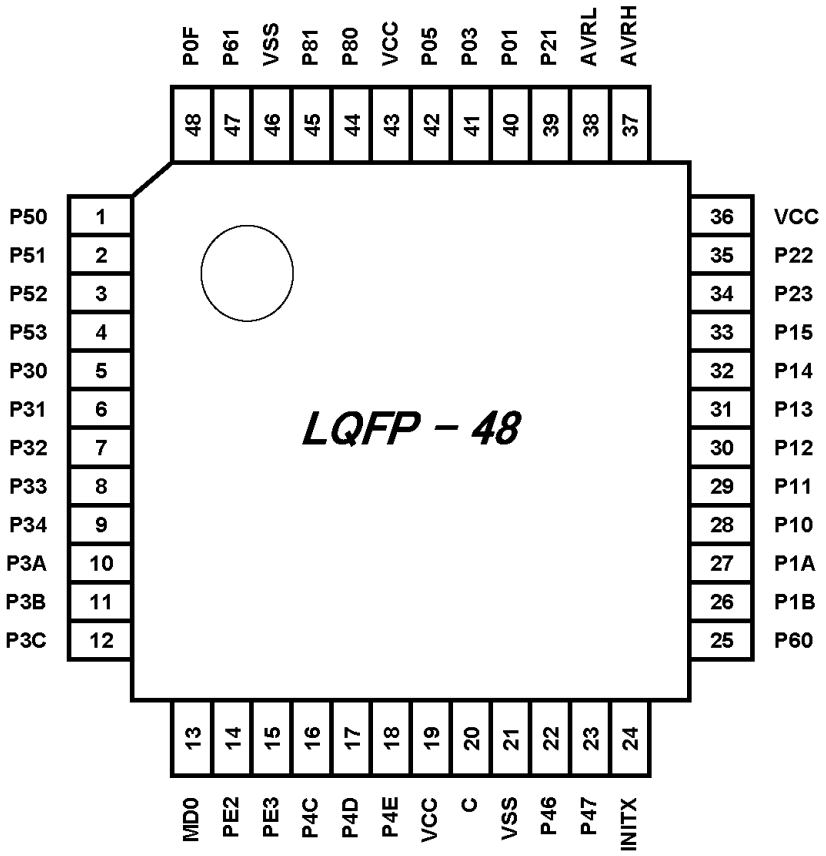
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c32b0agn20000

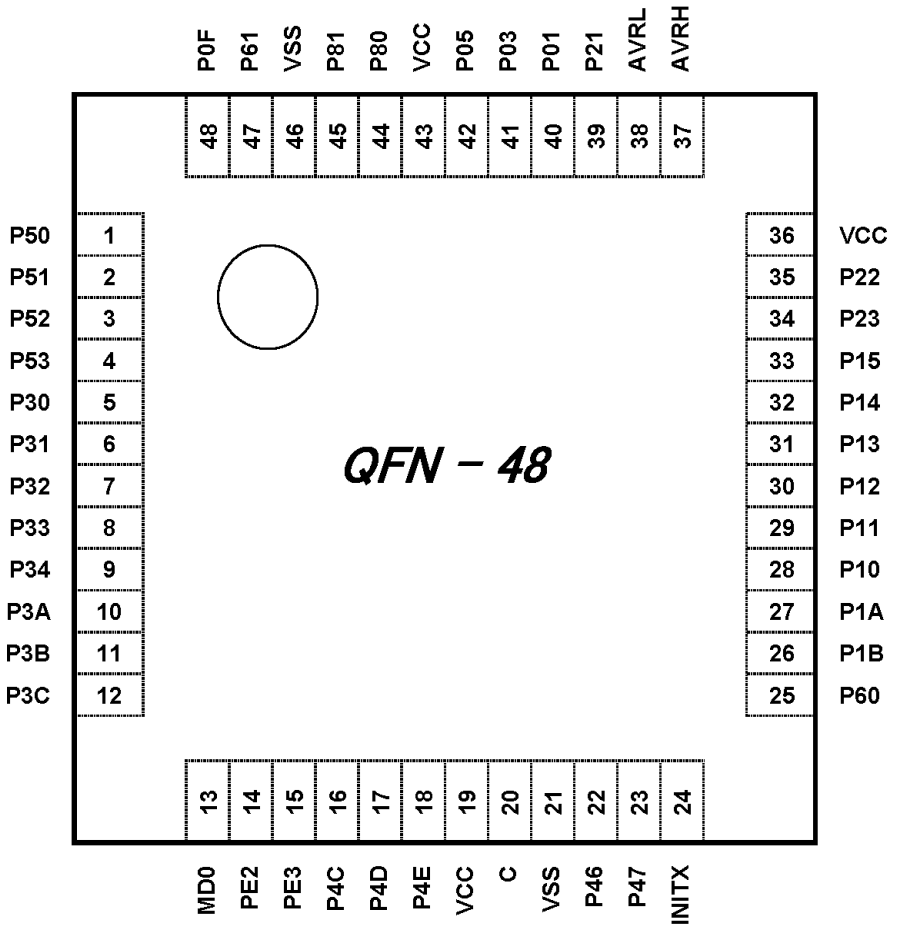
LQA048-02

(TOP VIEW)



WNY048

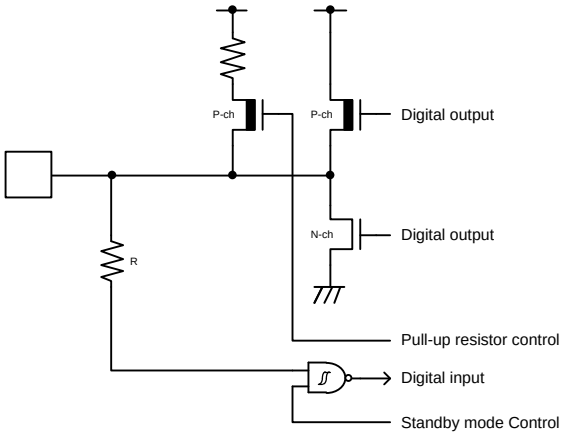
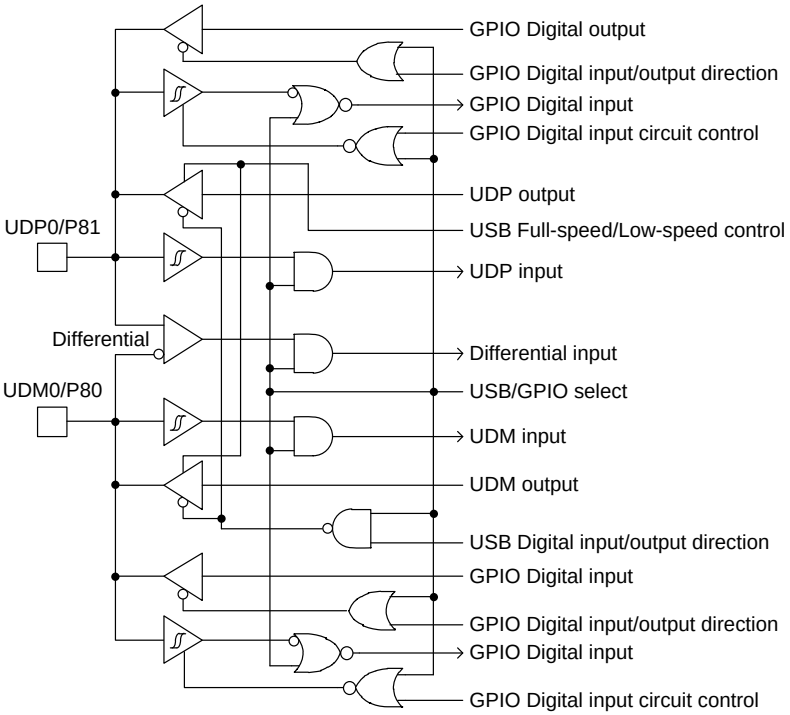
(TOP VIEW)



Pin No.			Pin Name	Alternate Functions					I/O Circuit Type	Pin State Type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32								
32	24	16	INITX						B	E
33	25	17	P60	TIOA2_2	INT15_1	CEC1_0			H	K
34	-	-	P1E	RTS4_1	MI2SMCK4_1				D	K
35	-	-	P1D	CTS4_1	MI2SWS4_1				D	K
36	-	-	P1C	SCK4_1	MI2SCK4_1				D	K
37	-	-	P1B	SOT4_1	MI2SDO4_1				D	K
-	26	-	P1B	SOT4_1					D	K
38	-	-	P1A	SIN4_1	INT05_1	CEC0_0	MI2SDI4_1		H	K
-	27	-	P1A	SIN4_1	INT05_1	CEC0_0			H	K
39	-	-	P1F	ADTG_5					D	K
40	28	18	P10	AN00					F	J
41	29	19	P11	AN01	SIN1_1	INT02_1	WKUP1		G	J
42	30	20	P12	AN02	SOT1_1				F	J
43	31	21	P13	AN03	SCK1_1	RTCCO_1	SUBOUT_1		F	J
44	32	-	P14	AN04	SIN0_1	SCS10_1	INT03_1		F	J
45	33	-	P15	AN05	SOT0_1	SCS11_1			F	J
46	34	22	P23	AN06	SCK0_0	TIOA7_1			F	J
47	35	23	P22	AN07	TIOB7_1				F	J
48	36	24	VCC						-	-
49	37	-	AVRH[1]						-	-
50	38	25	AVRL						-	-
51	39	26	P21	INT06_1	WKUP2				E	K
52	-	-	P00	WKUP4					E	K
53	40	27	P01	SWCLK	SOT0_0				D	K
54	-	-	P02	WKUP5					E	K
55	41	28	P03	SWDIO	SIN0_0	TIOB7_0			D	K
56	42	29	P05	MD1	TIOA5_2	INT00_1	WKUP3		E	K
57	43	-	VCC						-	-
58	44	30	P80	UDM0					J	G
59	45	31	P81	UDP0					J	G
60	46	32	VSS						-	-
61	47	-	P61	UHCONX0	TIOB2_2				H	K
62	-	-	P0B	TIOB6_1	WKUP6				E	K
63	-	-	P0C	TIOA6_1	WKUP7				E	K
64	48	1	P0F	NMIX	WKUP0	RTCCO_0	SUBOUT_0	CROUT_1	E	I

[1] In a 32-pin package, the AVRH pin is internally connected to the V_{CC} pin.

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	41	29	19
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I^2C pin (operation mode 4).	42	30	20
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I^2C pin (operation mode 4).	43	31	21
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 input/output pin.	44	32	-
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	45	33	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	1	1	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I^2C pin (operation mode 4).	2	2	3
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I^2C pin (operation mode 4).	3	3	4
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I^2C pin (operation mode 4).	37	26	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I^2C pin (operation mode 4).	36	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-

Type	Circuit	Remarks
H		・CMOS level output ・CMOS level hysteresis input ・5V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor Approximately 33 kΩ ・IOH= -4 mA, IOL= 4 mA ・Available to control PZR registers ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
I		・CMOS level hysteresis input
J		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should mount only under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

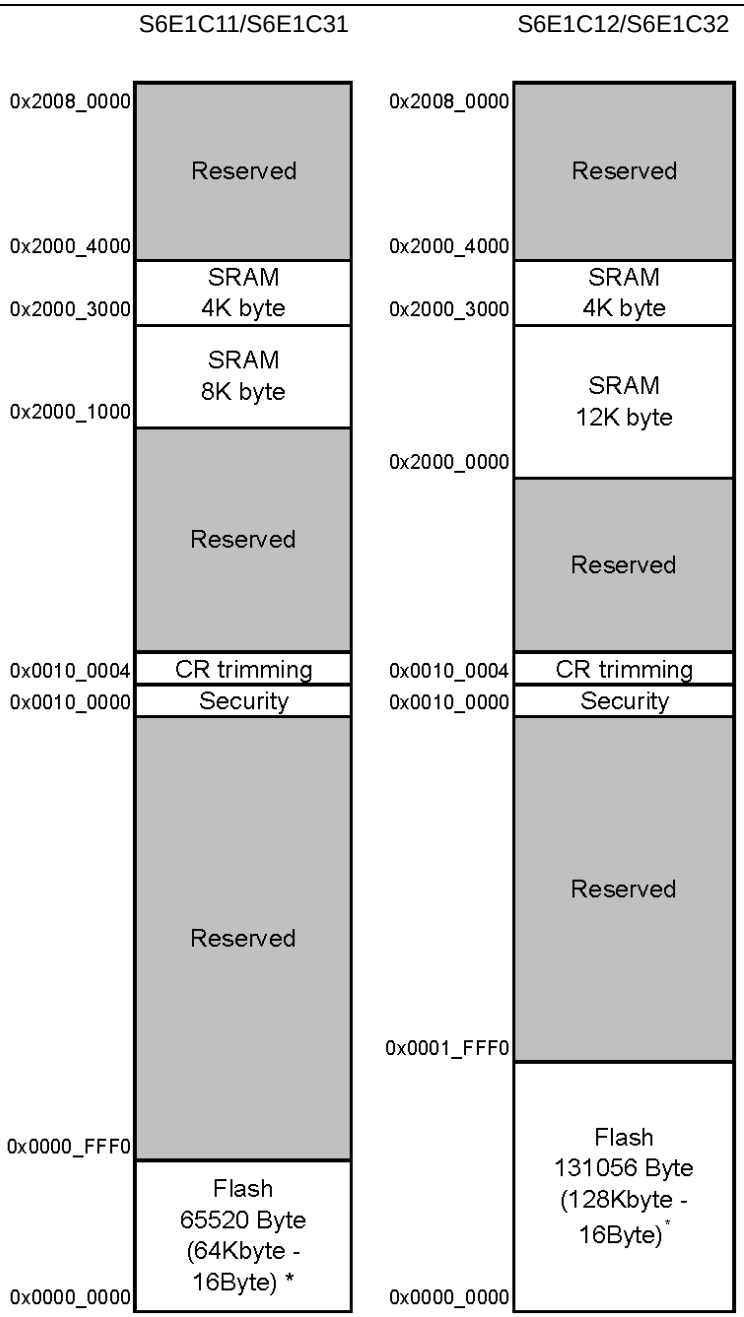
Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the flash memory.

LVD Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.15	0.3	µA	For occurrence of reset
				0.10	0.3	µA	For occurrence of interrupt

Bipolar Vref Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Bipolar Vref Current	I_{CCBGR}	VCC	At operation	100	200	µA	

Flash Memory Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	4.4	5.6	mA	

A/D converter Current

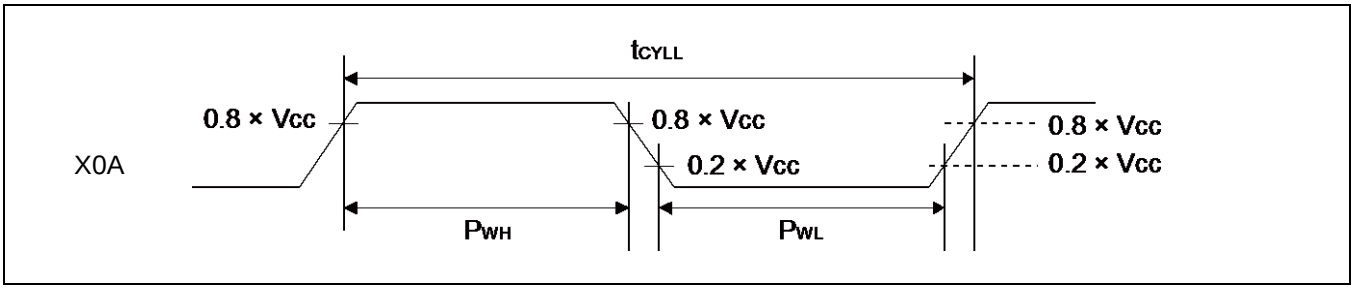
(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	VCC	At operation	0.5	0.75	mA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	0.69	1.3	mA	AVRH=3.6 V
			At stop	0.1	1.3	µA	

11.4.2 Sub Clock Input Characteristics[35]

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used



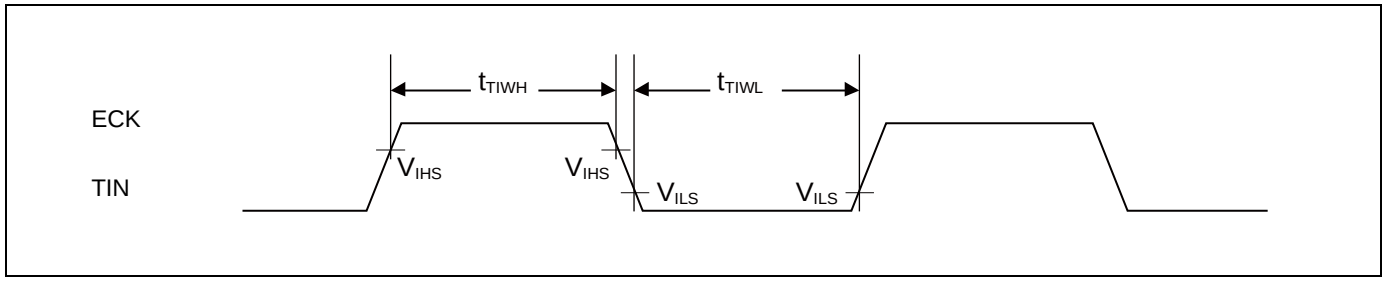
[35] See "Sub crystal oscillator" in "11. Handling Devices" for the crystal oscillator used.

11.4.8 Base Timer Input Timing

Timer Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

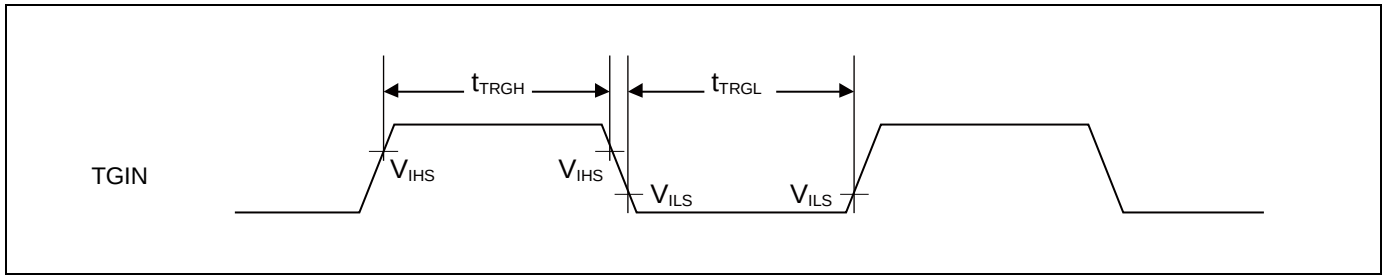
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see the Peripheral Address Map
- *".*

11.4.9 CSIO/SPI/UART Timing

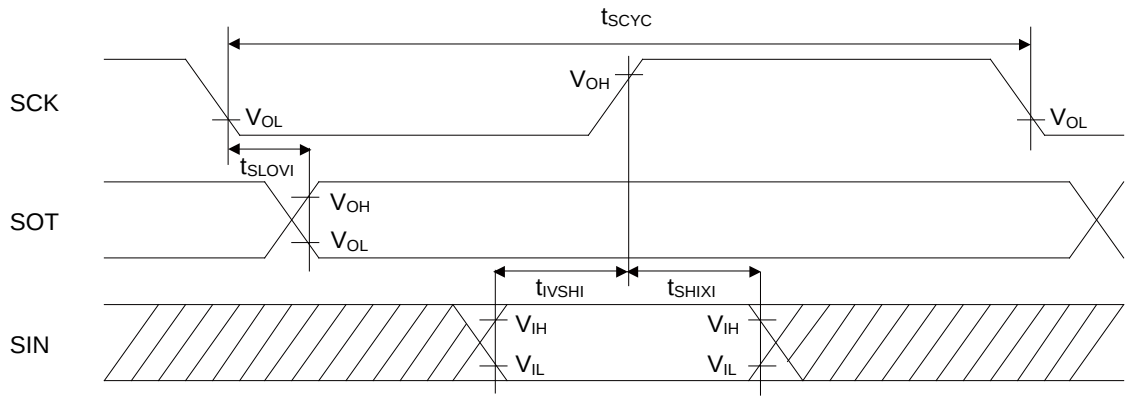
CSIO (SPI=0, SCINV=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

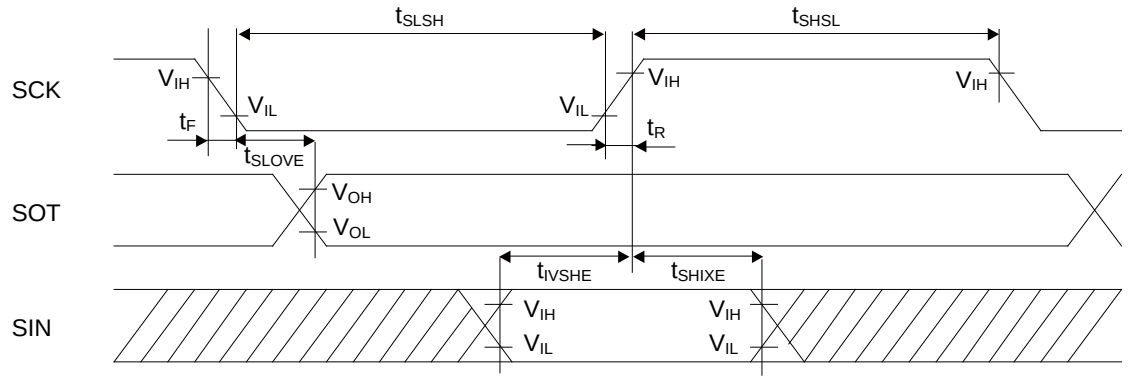
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

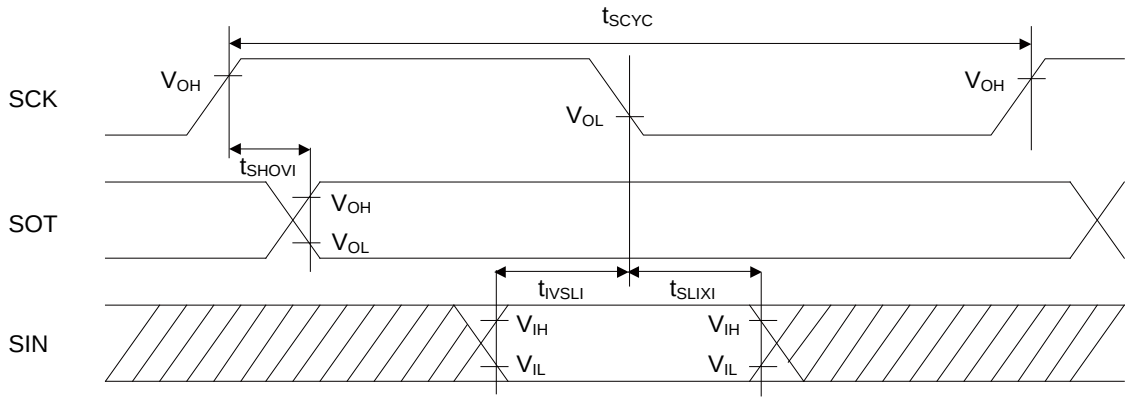
- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see the Peripheral Address Map.
- *The characteristics are applicable only when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



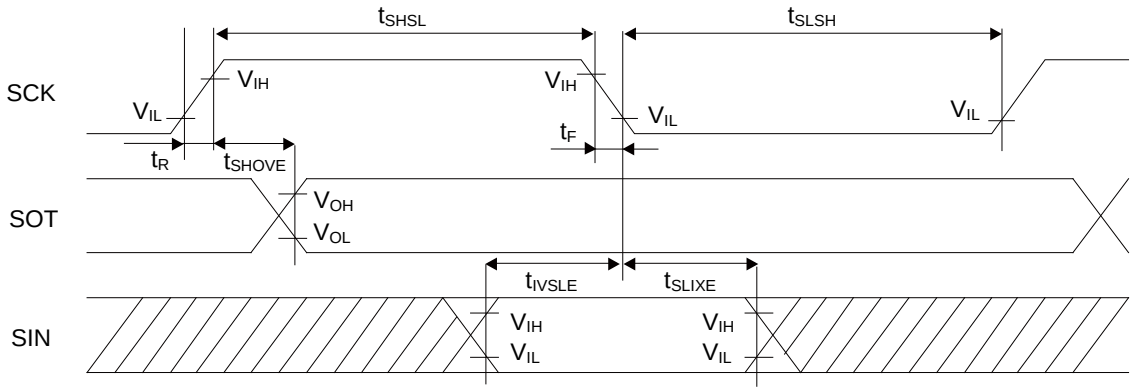
Master mode



Slave mode



Master mode



Slave mode

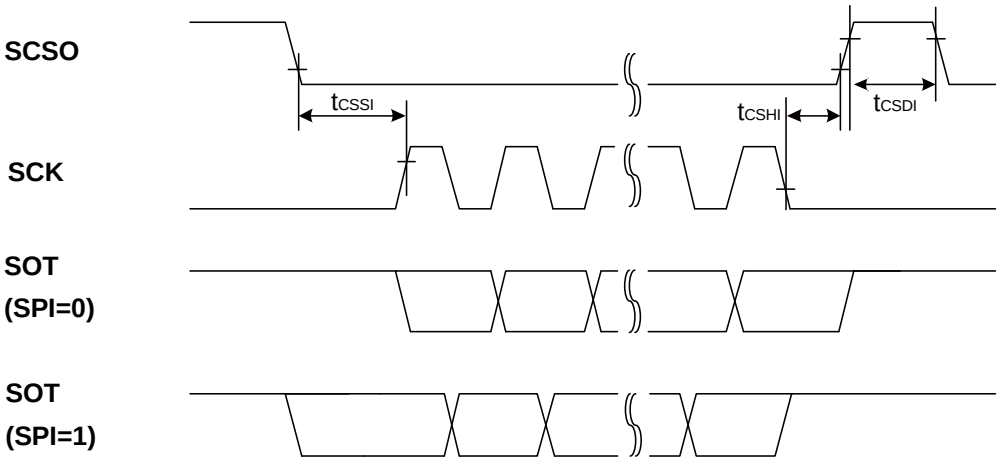
SPI (SPI=1, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

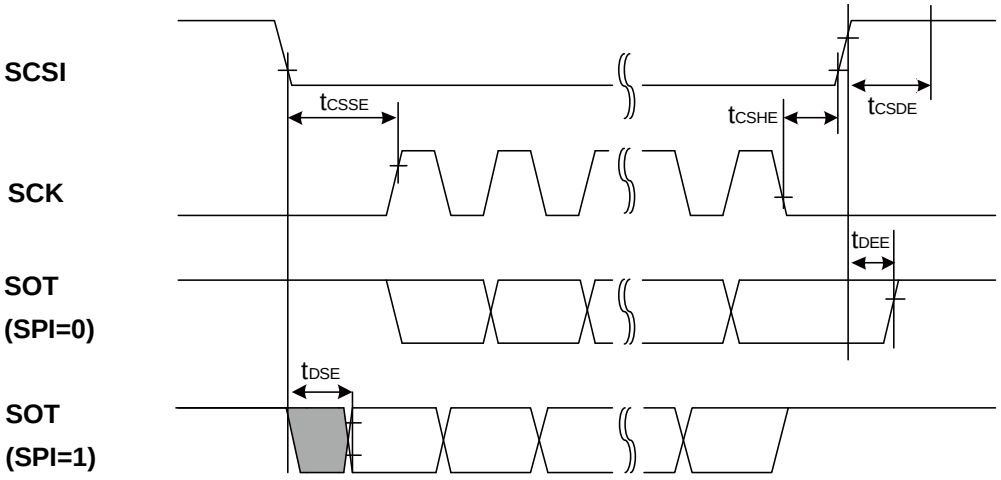
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see the Peripheral Address Map.
- *The characteristics are applicable only when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

11.5 12-bit A/D Converter

Electrical Characteristics of A/D Converter (Preliminary Values)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time[64]	-	-	1.0	-	-	µs	$V_{CC} \geq 2.7$ V
			4.0	-	-		1.8 ≤ V_{CC} < 2.7 V
			10	-	-		1.65 ≤ V_{CC} < 1.8 V
Sampling time[65]	Ts	-	0.3	-	10	µs	$V_{CC} \geq 2.7$ V
			1.2	-			1.8 ≤ V_{CC} < 2.7 V
			3.0	-			1.65 ≤ V_{CC} < 1.8 V
Compare clock cycle[66]	Tcck	-	50	-	1000	ns	$V_{CC} \geq 2.7$ V
			200	-			1.8 ≤ V_{CC} < 2.7 V
			500	-			1.65 ≤ V_{CC} < 1.8 V
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	7.5	pF	
Analog input resistance	R_{AIN}	-	-	-	2.2	kΩ	$V_{CC} \geq 2.7$ V
					5.5		1.8 ≤ V_{CC} < 2.7 V
					10.5		1.65 ≤ V_{CC} < 1.8 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	V_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	V_{CC}	V	VCC ≥ 2.7V
			V_{CC}				VCC < 2.7V
	-	AVRL	V_{SS}	-	V_{SS}	V	

[64] The conversion time is the value of sampling time (t_s) + compare time (t_c).
The minimum conversion time is computed according to the following conditions:
- $V_{CC} \geq 2.7$ V sampling time=0.3 µs, compare time=0.7 µs
- 1.8 ≤ V_{CC} < 2.7 V sampling time=1.2 µs, compare time=2.8 µs
- 1.65 ≤ V_{CC} < 1.8 V sampling time=3.0 µs, compare time=7.0 µs

Ensure that the conversion time satisfies the specifications of the sampling time (t_s) and compare clock cycle (t_{CCK}).
For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see the Peripheral Address Map.
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

[65] The required sampling time varies according to the external impedance. Set a sampling time that satisfies (Equation 1).

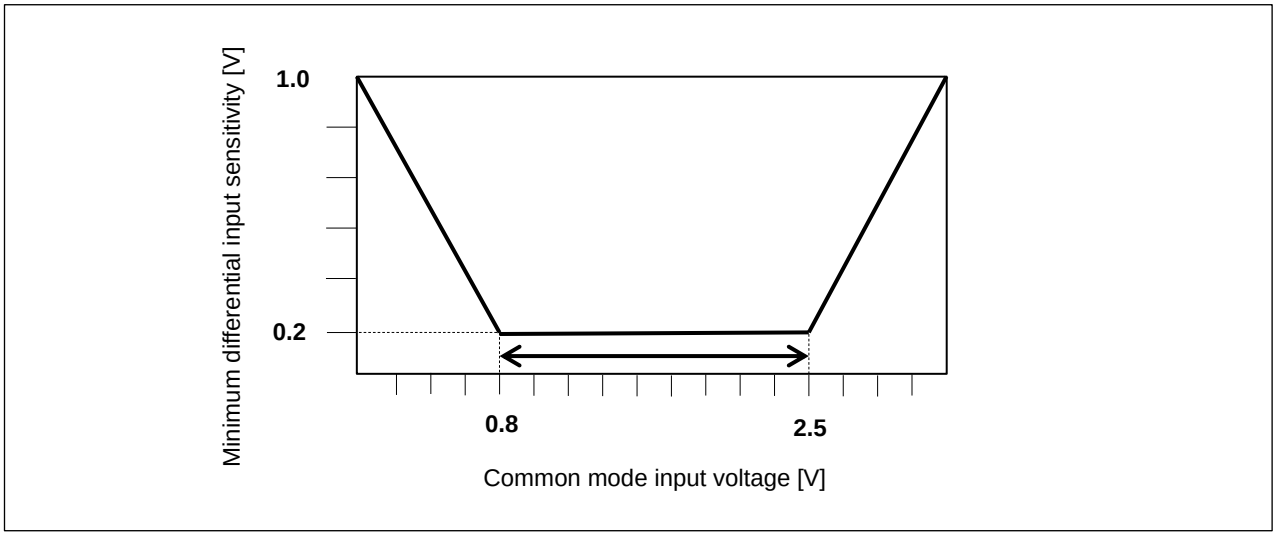
[66] The compare time (t_c) is the result of (Equation 2).

11.6 USB Characteristics

(V_{CC}=3.0 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Schematic Reference
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	V_{CC} + 0.3	V	1
	Input L level voltage	V_{IL}		-	V_{SS} – 0.3	0.8	V	1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	2
	Differential common mode range	V_{CM}		-	0.8	2.5	V	2
Output characteristic	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	4
	Rising time	t_{FR}		Full-speed	4	20	ns	5
	Falling time	t_{FF}		Full-speed	4	20	ns	5
	Rising/Falling time matching	t_{FRFM}		Full-speed	90	111.11	%	5
	Output impedance	Z_{DRV}		Full-speed	28	44	Ω	6
	Rising time	t_{LR}		Low-speed	75	300	ns	7
	Falling time	t_{LF}		Low-speed	75	300	ns	7
	Rising/Falling time matching	t_{LRFM}		Low-speed	80	125	%	7

1. The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V_{IL}(Max)=0.8 V, VIH(Min)=2.0 V (TTL input standard).
   There is some hysteresis to lower noise sensitivity.
2. Use differential-receiver to receive USB differential data signal.
   Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
   Above voltage range is the common mode input voltage range.



11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

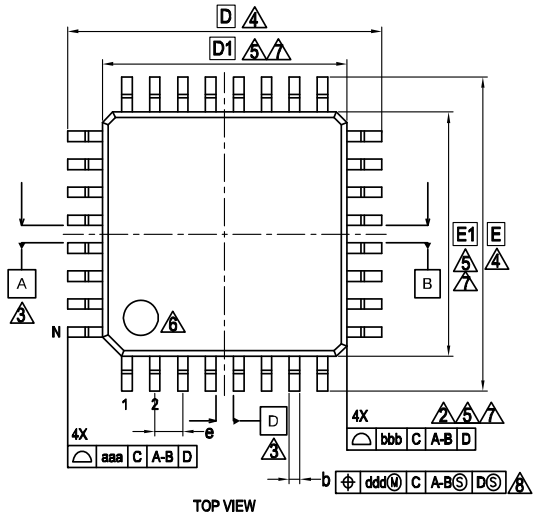
(T_A=-40°C to +105°C)

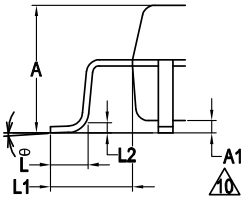
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed[67]	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}[68]	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

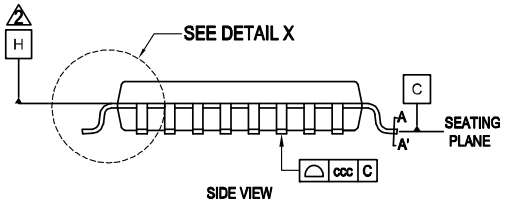
[67] The value of low voltage detection reset is always fixed.
[68] t_{CYCP} indicates the APB1 bus clock cycle time.

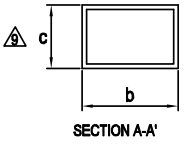
14. Package Dimensions

LQB032 032 LEAD PLASTIC LOW PROFILE QUAD FLAT PACKAGE









PACKAGE	LQB032		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
b	0.32	0.35	0.42
c	0.13	—	0.18
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
θ	0°	—	7°
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		

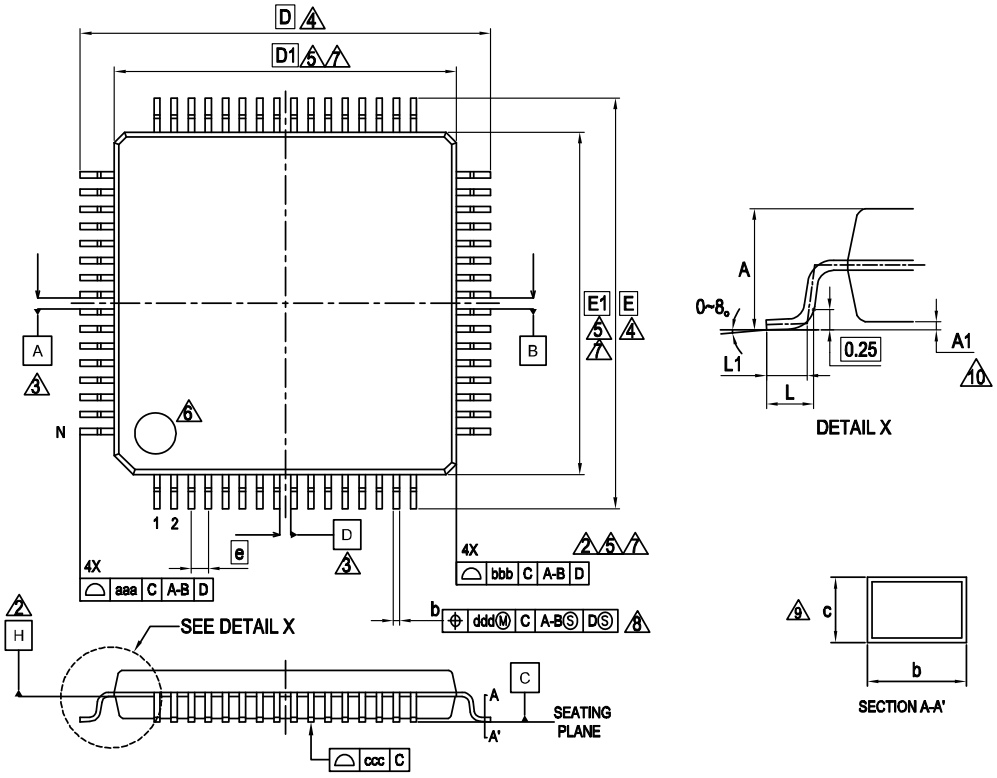
SYMBOL	TOLERANCES OF FORM AND POSITION
N	32
aaa	0.20
bbb	0.10
ccc	0.10
ddd	0.20

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev.0B

LQD064-02 , 64 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQD64-02		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	64		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A