SHARP/Socle Technology - LH75400N0Q100C0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, EBI/EMI, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75400n0q100c0

LH75410 BLOCK DIAGRAM

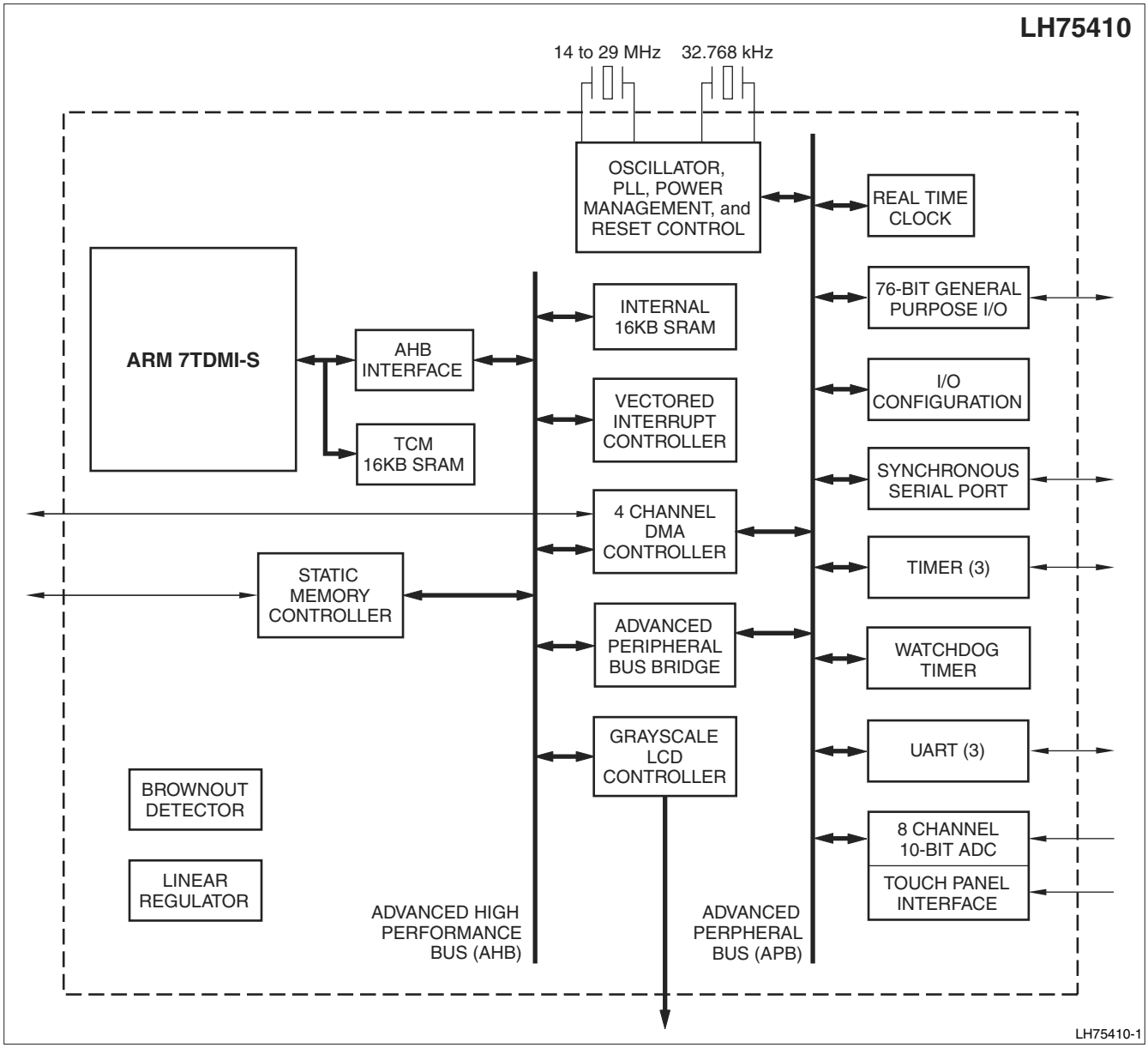


Figure 4. LH75410 Block Diagram

LH75401 Signal Descriptions

Table 2. LH75401 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1

THE LH75411

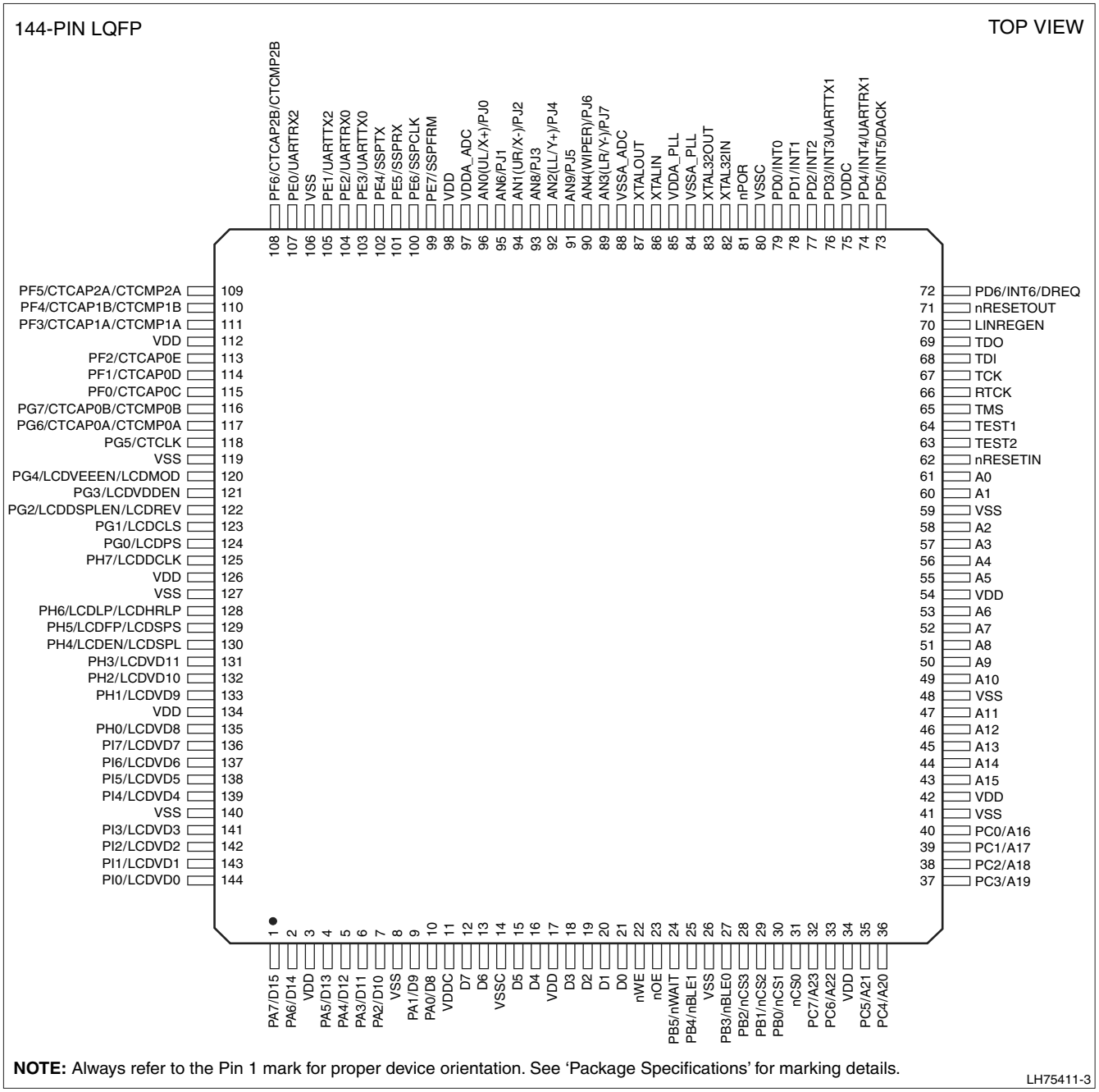


Figure 6. LH75411 Pin Diagram

LH75411 Numerical Pin Listing

Table 3. LH75411 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

LH75400 Numerical Pin Listing

Table 5. LH75400 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1

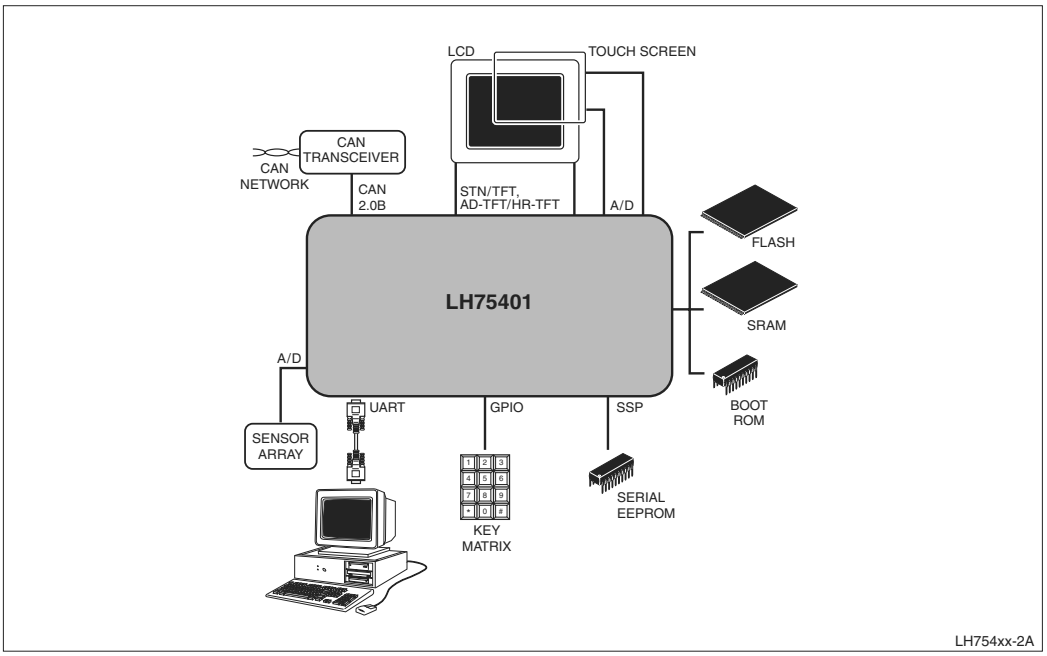


Figure 9. LH75401 System Application Example

FUNCTIONAL OVERVIEW

ARM7TDMI-S Processor

The LH75400/01/10/11 microcontrollers feature the ARM7TDMI-S core with an Advanced High-Performance Bus (AHB) 2.0 interface. The ARM7TDMI-S is a 16/32-bit embedded RISC processor and a member of the ARM7 Thumb family of processors. For more information, visit the ARM Web site at www.arm.com.

Bus Architecture

The LH75400/01/10/11 microcontrollers use the ARM Advanced Microcontroller Bus Architecture (AMBA) 2.0 internal bus protocol. Three AHB masters control access to external memory and on-chip peripherals:

- The ARM processor fetches instructions and transfers data
- The Direct Memory Access Controller (DMAC) transfers from memory to memory, from peripheral to memory, and from memory to peripheral
- The LCDC refreshes an LCD panel with data from the external memory or from internal memory if the frame buffer is 16KB or less.

The ARM7TDMI-S processor is the default bus master. An Advanced Peripheral Bus (APB) bridge is provided to access to the various APB peripherals. Generally, APB peripherals are serviced by the ARM core. However, if they are DMA-enabled, they are also serviced by the DMAC to increase system performance while the ARM core runs from local internal memory.

Power Supplies

Five-Volt-tolerant 3.3 V I/Os are employed. The LH75400/01/10/11 microcontrollers require a single 3.3 V supply. The core logic requires 1.8 V, supplied by an on-chip linear regulator. Core logic power may also be supplied externally to achieve higher system speeds. See the Electrical Specifications.

Clock Sources

The LH75400/01/10/11 microcontrollers may use two crystal oscillators, or an externally supplied clock. There are two clock trees:

- One clock tree drives an internal Phase Lock Loop (PLL) and the three UARTs. It supports a crystal oscillator frequency range from 14 MHz to 20 MHz.
- The other is a 32.768 kHz oscillator that generates a 1 Hz clock for the RTC. (Use of the 32.768 kHz crystal for the Real Time Clock is optional. If not using the crystal, tie XTAL32IN to VSS and allow XTAL32OUT to float.)

The 14-to-20 MHz crystal oscillator drives the UART clocks, so an oscillator frequency of 14.7456 MHz is recommended to achieve modem baud rates.

The PLL may be bypassed and an external clock supplied at XTALIN; the SoC will operate to DC with the PLL disabled. When doing so, allow XTALOUT to float. The input clock with the PLL bypassed will be twice the desired system operating frequency, and care must be taken not to exceed the maximum input clock voltage. Maximum values for system speeds and input voltages are given in the Electrical Specifications.

UART 2 FEATURES

- Similar functionality to the industry-standard 82510
- Supported baud rates up to 3,225,600 baud (given a system clock of 51.6096 MHz)
- 5, 6, 7, 8, or 9 data bits per character
- Even, odd, HIGH, LOW, software, or no parity-bit generation and detection
- 3/4, 1, 1-1/4, 1-1/2, 1-3/4, or 2 stop-bit generation
- µLAN address flag
- Full-duplex operation
- Separate transmit and receive FIFOs, with programmable depth (1 or 4). Each FIFO has overrun protection and:
  - Programmable receive trigger levels: 1/4, 1/2, 3/4, or full
  - Programmable transmit trigger levels: empty, 1/4, 1/2, 3/4.
- Two 16-bit baud-rate generators.
- One interrupt that can be triggered by transmit and receive FIFO thresholds, receive errors, control character or address marker reception, or timer timeout
- Generation and detection of breaks during UART transactions
- Support for local loopback, remote loopback, and auto-echo modes
- µLAN Address Mode.

Timers

The LH75400/01/10/11 microcontrollers have three 16-bit timers. The timers are clocked by the system clock, but have an internal scaled-down system clock that is used for the Pulse Width Modulator (PWM) and compare functions.

All counters are incremented by an internal prescaled counter clock or external clock and can generate an overflow interrupt. All three timers have separate internal prescaled counter clocks, with either a common external clock or a prescaled version of the system clock.

- Timer 0 has five Capture Registers and two Compare Registers.
- Timer 1 and Timer 2 have two Capture and two Compare Registers each.

The Capture Registers have edge-selectable inputs and can generate an interrupt. The Compare Registers can force the compare output pin either HIGH or LOW upon a match.

The timers support a PWM Mode that uses the two Timer Compare Registers associated with a timer to create a PWM. Each timer can generate a separate interrupt. The interrupt becomes active if any enabled compare, capture, or overflow interrupt condition occurs. The interrupt remains active until all compare, capture, and overflow interrupts are cleared.

Real Time Clock (RTC)

The RTC is an AMBA slave module that connects to the APB. The RTC provides basic alarm functions or acts as a long-time base counter by generating an interrupt signal after counting for a programmed number of cycles of an RTC input. Counting in 1-second intervals is achieved using a 1 Hz clock input to the RTC.

RTC FEATURES

- 32-bit up-counter with programmable load
- Programmable 32-bit match Compare Register
- Software-maskable interrupt that is set when the Counter and Compare Registers have identical values.

Controller Area Network (CAN)

The CAN 2.0B Controller is an AMBA-compliant peripheral that connects as a slave to the APB. The CAN Controller is located between the processor core and a CAN Transceiver, and is accessed through the AMBA port.

CAN communications are performed serially, at a maximum frequency of 1MB/s, using the TX (transmit) and RX (receive) lines. The TX and RX signals for data transmission and reception provide the communications interface between the CAN Controller and the CAN bus. All peripherals share the TX and RX lines, and always see the common incoming and outgoing data.

Bus arbitration follows the CAN 2.0A and CAN 2.0B specifications. The bus is always controlled by the node with the highest priority (lowest ID). Only after the bus has been released can the next highest priority node control it. Transmit and receive errors are handled according to the CAN protocol.

Bus timing is critical to the CAN protocol. Therefore, the CAN Controller has two programmable Bus Timing Registers that define timing parameters.

NOTE: The CAN Controller pertains to the LH75401 and LH75400 microcontrollers.

Table 13. SSP Modes

MODE	DESCRIPTION	DATA TRANSFERS
Motorola SPI	For communications with Motorola SPI-compatible devices. Clock polarity and phase are programmable.	Full-duplex, 4-wire synchronous
SSI	For communications with Texas Instruments DSP-compatible Serial Synchronous Interface devices.	Full-duplex, 4-wire synchronous
National Semiconductor Microwire	For communications with National Semiconductor Microwire-compatible devices.	Half-duplex synchronous, using 8-bit control messages

Watchdog Timer (WDT)

The WDT consists of a 32-bit down-counter that allows a selectable time-out interval to detect malfunctions. The timer must be reset by software periodically. Otherwise, a time-out occurs, interrupting the system. If the interrupt is not serviced within the timeout period, the WDT triggers the RCPC to generate a System Reset. If the WDT times out, it sets a bit in the RCPC Reset Status Register.

The WDT supports 16 selectable time intervals, for a time-out of 216 through 231 system clock cycles. All Control and Status Registers for the Watchdog Timer are accessed through the APB.

WDT FEATURES

- Counter generates an interrupt at a set interval and the count reloads from the pre-set value after reaching zero.
- Default timeout period is set to the minimum timeout of 216 system clock cycles.
- WDT is driven by the APB.
- Built-in protection mechanism guards against interrupt-service failure.
- WDT can be programmed to trigger a System Reset on a timeout.
- WDT can be programmed to trigger an interrupt on the first timeout; then, if the service routine fails to clear the interrupt, the next WDT timeout triggers a System Reset.

Reset, Clock, and Power Controller (RCPC)

The RCPC lets users control System Reset, clocks, power management, and external interrupt conditioning via the AMBA APB interface. This control includes:

- Enabling and disabling various clocks
- Managing power-down sequencing
- Selecting the sources for various clocks.

The RCPC provides for an orderly start-up until the crystal oscillator stabilizes and the PLL acquires lock. If users want to change the system clock frequency during normal operation, the RCPC ensures a seamless transition between the old and new frequencies.

RCPC FEATURES

- Manages five Power Modes for minimizing power consumption: Active, Standby, Sleep, Stop1, and Stop2
- Generates the system clock (HCLK) from either the PLL clock or the PLL-bypassed (oscillator) clock, divided by 2, 4, 6, 8, … 30
- Generates three UART clocks from oscillator clock
- Generates the 1 Hz RTC clock
- Generates the SSP and LCD clocks from HCLK, divided by 1, 2, 4, 8, 16, 32, or 64
- Provides a selectable external clock output
- Generates system and RTC Resets based on an external reset, Watchdog Timer reset, or soft reset
- Configures seven HIGH/LOW-level or rising/falling edge-trigger external interrupts and converts them to HIGH-level trigger interrupt outputs required by the VIC
- Generates remap outputs used by the memory map decoder
- Provides an identification register
- Supports external or watchdog reset status.

Operating Modes

The LH75400/01/10/11 microcontrollers support three operating modes:

- Normal Mode
- PLL Bypass Mode, where the internal PLL is bypassed and an external clock source is used; otherwise the chip operates normally
- EmbeddedICE Mode, where the JTAG port accesses the TAP Controller in the core and the core is placed in Debug Mode.

The state of the TEST1, TEST2, and nRESETIN signals determines the operating mode entered at Power-on Reset (see Table 15).

Table 15. Device Operating Modes

OPERATING MODE	TEST2	TEST1	nRESETIN
Reserved	0	0	0
PLL Bypass	0	0	1
Reserved	0	1	x
Reserved	1	0	0
EmbeddedICE	1	0	1
Normal	1	1	x

NOTE: TEST1, TEST2, and nRESETIN are latched on the rising edge of nPOR. The microcontroller stays in that operating mode until power is removed or nPOR transitions from LOW to HIGH.

General Purpose Input/Output (GPIO)

The LH75400/01/10/11 microcontrollers have 10 GPIO ports:

- Seven 8-bit ports
- Two 7-bit ports
- One 6-bit port.

The GPIO ports are designated A through J and provide 76 bits of programmable input/output (see Table 16). Pins of all ports, except Port J, can be configured as inputs or outputs. Port J is input only. Upon System Reset, all ports default to inputs.

Table 16. GPIO Ports

PORT	PROGRAMMABLE PINS
A	8 Input/Output Pins
B	6 Input/Output Pins
C	8 Input/Output Pins
D	7 Input/Output Pins
E	8 Input/Output Pins
F	7 Input/Output Pins
G	8 Input/Output Pins
H	8 Input/Output Pins
I	8 Input/Output Pins
J	8 Input Pins

DC Characteristics

All characteristics are specified over an operating temperature of -40°C to +85°C, and at minimum and maximum supply voltages.

Table 23. DC Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS	NOTES
VIH	CMOS Input HIGH Voltage	2.0			V		
VIL	CMOS Input LOW Voltage			0.8	V		1
VT+	Schmitt Trigger Positive Going Threshold	2.0			V		
VT-	Schmitt Trigger Negative Going Threshold			0.8	V		
Vhst	Schmitt Trigger Hysteresis	0.35			V		
VOH	Output Drive 1	2.6			V	IOH = -2 mA	
	Output Drive 2	2.6			V	IOH = -4 mA	
	Output Drive 3	2.6			V	IOH = -6 mA	
	Output Drive 4	2.6			V	IOH = -8 mA	
VOL	Output Drive 1			0.4	V	IOL = 2 mA	
	Output Drive 2			0.4	V	IOL = 4 mA	
	Output Drive 3			0.4	V	IOL = 6 mA	
	Output Drive 4			0.4	V	IOL = 8 mA	
XTAL32IN	External Clock Input	1.62	1.8	1.98	V	Externally supplied	
XTALIN	External Clock Input	1.62	1.8	1.98	V	Externally supplied	
IIN	Input Leakage Current	-10		10	µA	VIN = VDD or GND	
IACTIVE	Active Current		50	70	mA		2
ISTANDBY	Standby Current		45		mA		2
ISLEEP	Sleep Current		4.0		mA		
ISTOP1	Stop1 Current		3.0		mA		
ISTOP2	Stop2 Current (RTC ON)		35		µA		3
			120		µA		4
ISTOP2	Stop2 Current (RTC OFF)		23		µA		3
			100		µA		4

NOTES:
1. VIL MAX. = 0.5 V for pin TCK with 50 pF load.
2. Running a Typical Application at 51.6 MHz.
3. Using external 1.8 V supply, internal regulator disabled.
4. Using Internal linear regulator.

Table 24. Linear Regulator DC Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		µA
ISLEEPLR	Current when Regulator is Disabled		8		µA
IOLR	Output Current Range	0.0		100	mA
VOLR	Output Voltage		1.84		V
RPULL	Pull-up Resistor			0	Ω

Synchronous Serial Port Waveform

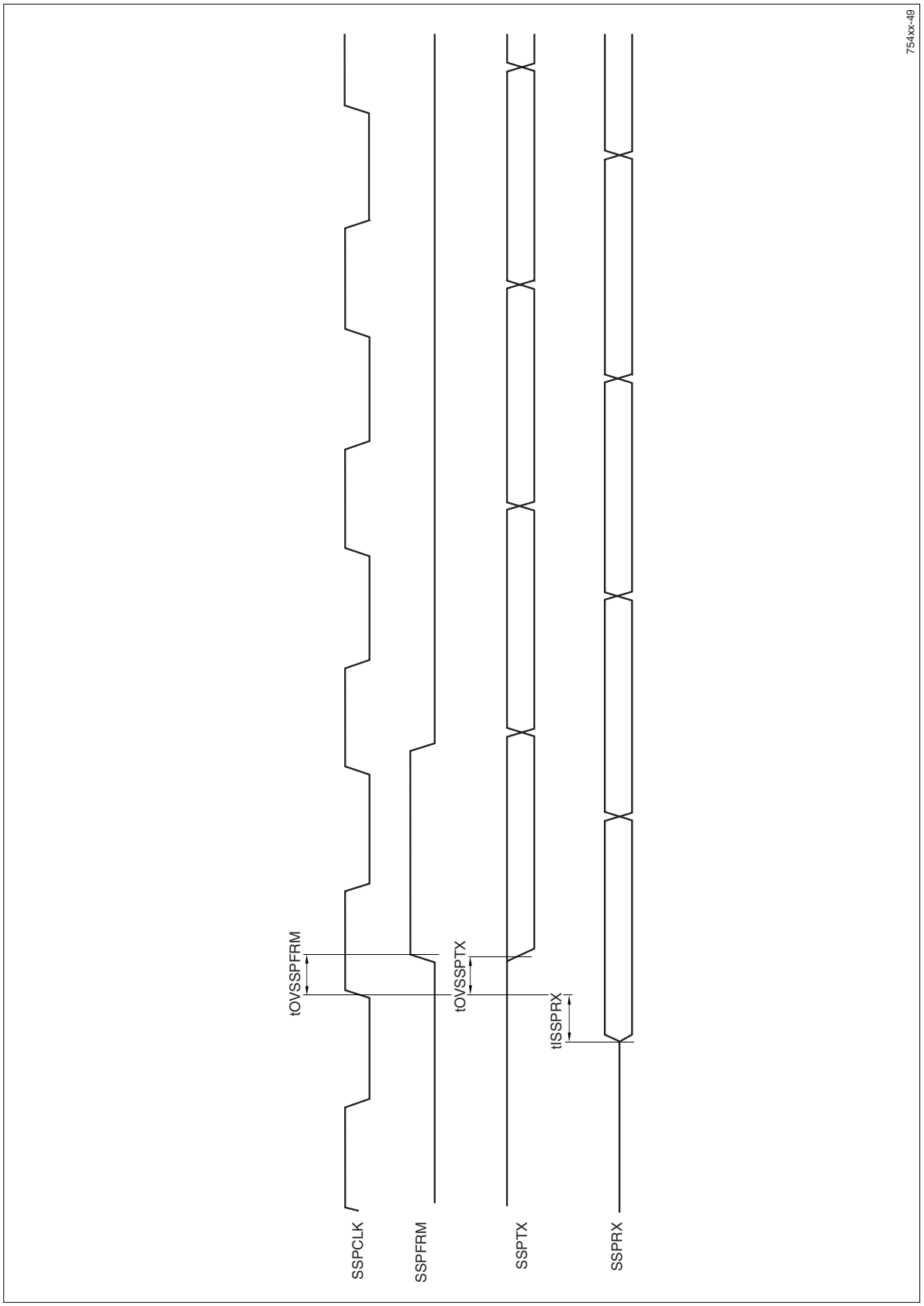


Figure 17. Synchronous Serial Port Waveform

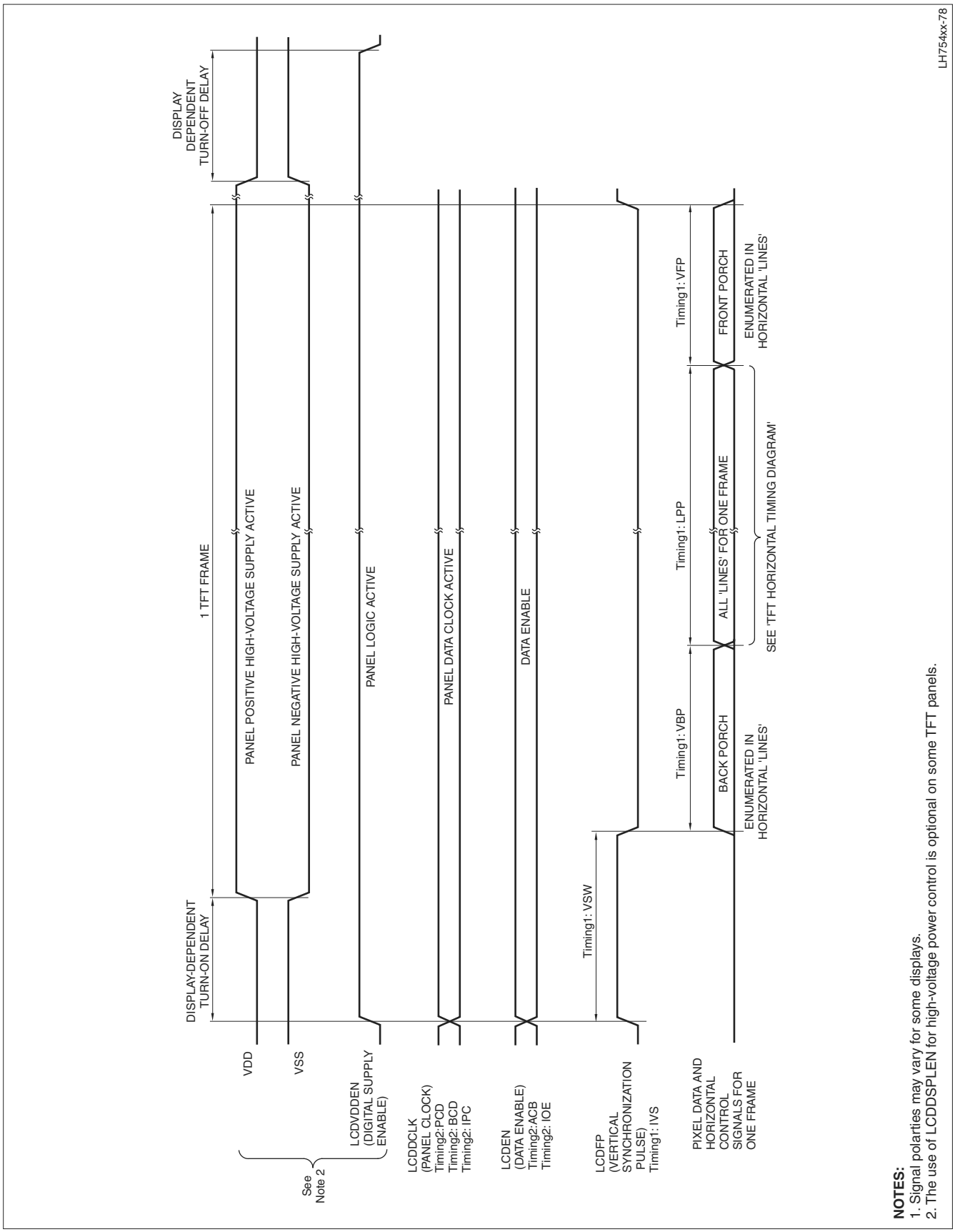
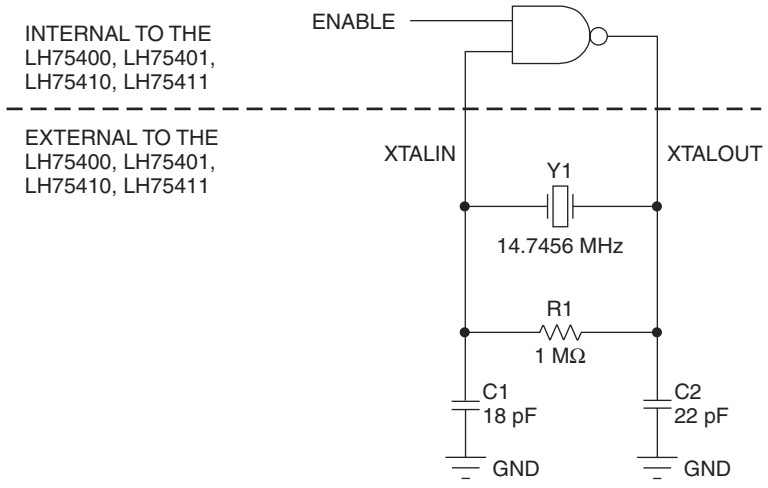


Figure 23. TFT Vertical Timing Diagram



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

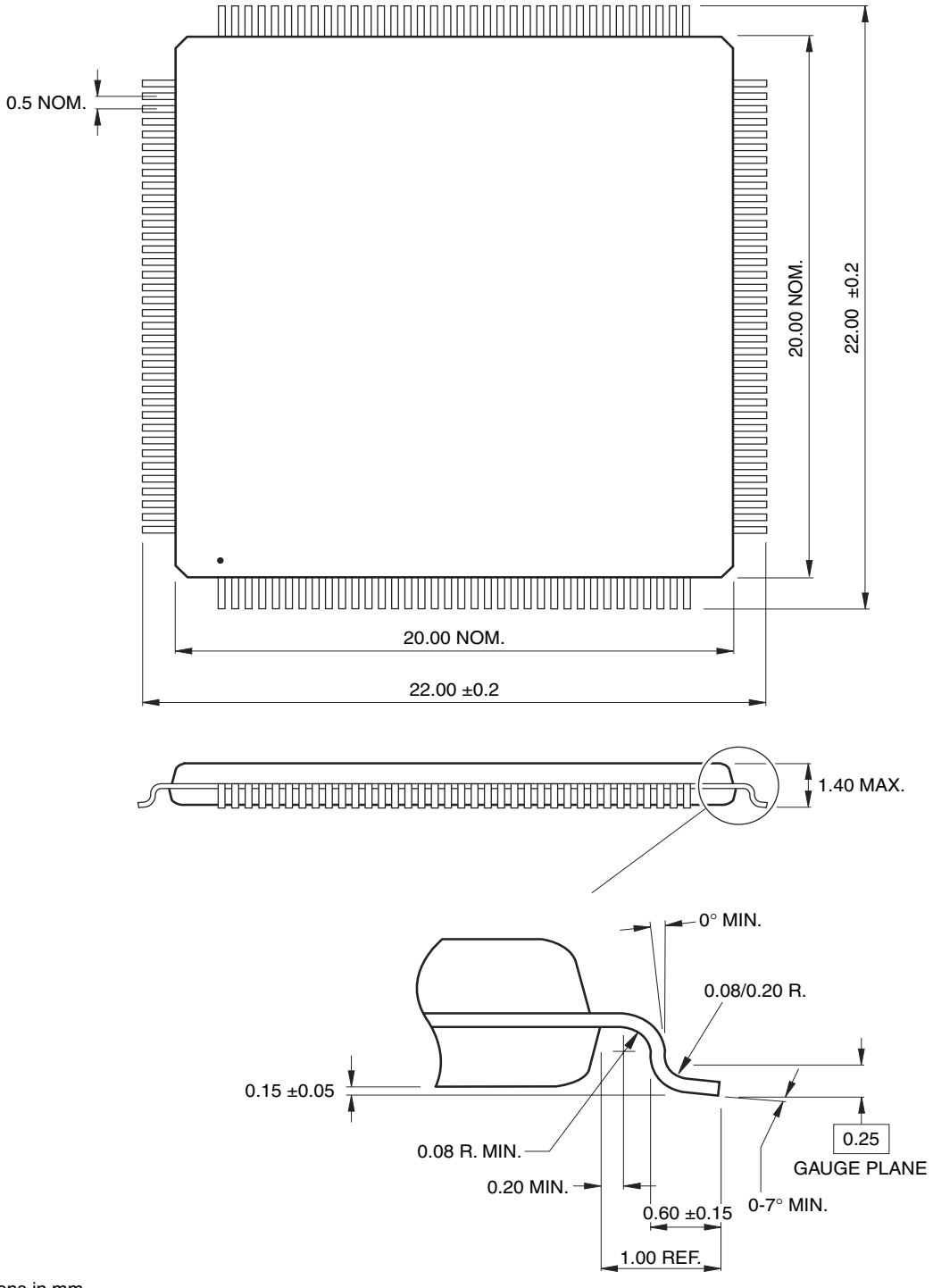
PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

LH754xx-102

Figure 27. Suggested External Components, 14.7456 MHz Oscillator

PACKAGE SPECIFICATIONS

144LQFP (JEDEC MS-026) **TOP VIEW**

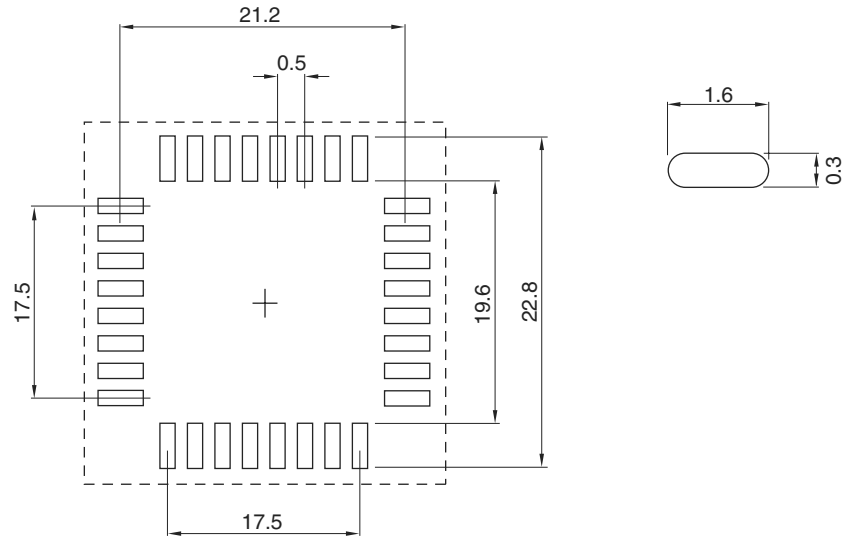


NOTE: Dimensions in mm.

144LQFP-JEDEC

Figure 28. 144-pin LQFP

144LQFP



NOTE: Dimensions in mm.

144LQFP

Figure 29. Recommended PCB Footprint