SHARP/Socle Technology - LH75401N0M100C0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, EBI/EMI, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75401n0m100c0

LH75401 BLOCK DIAGRAM

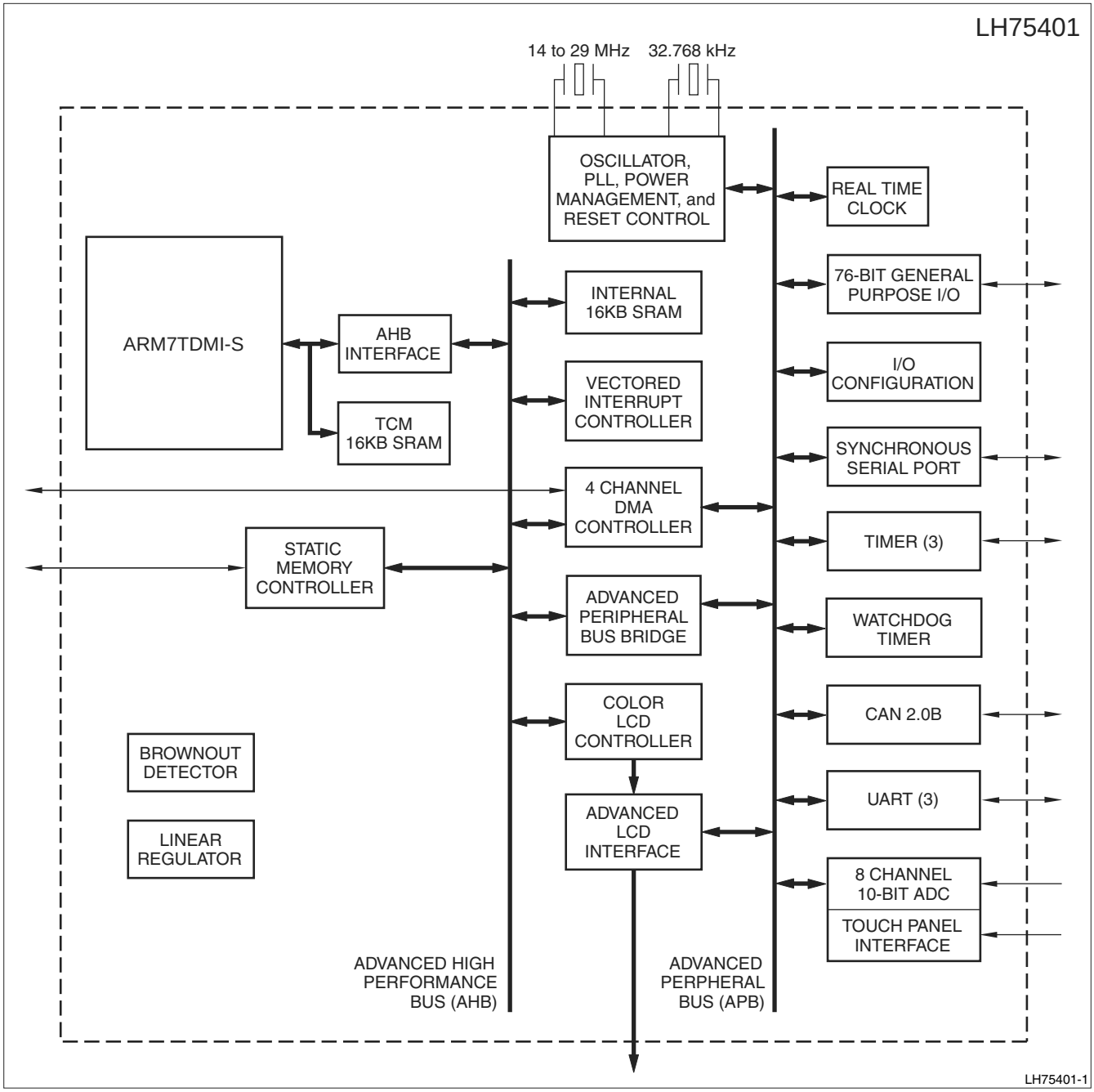


Figure 1. LH75401 Block Diagram

LH75411 BLOCK DIAGRAM

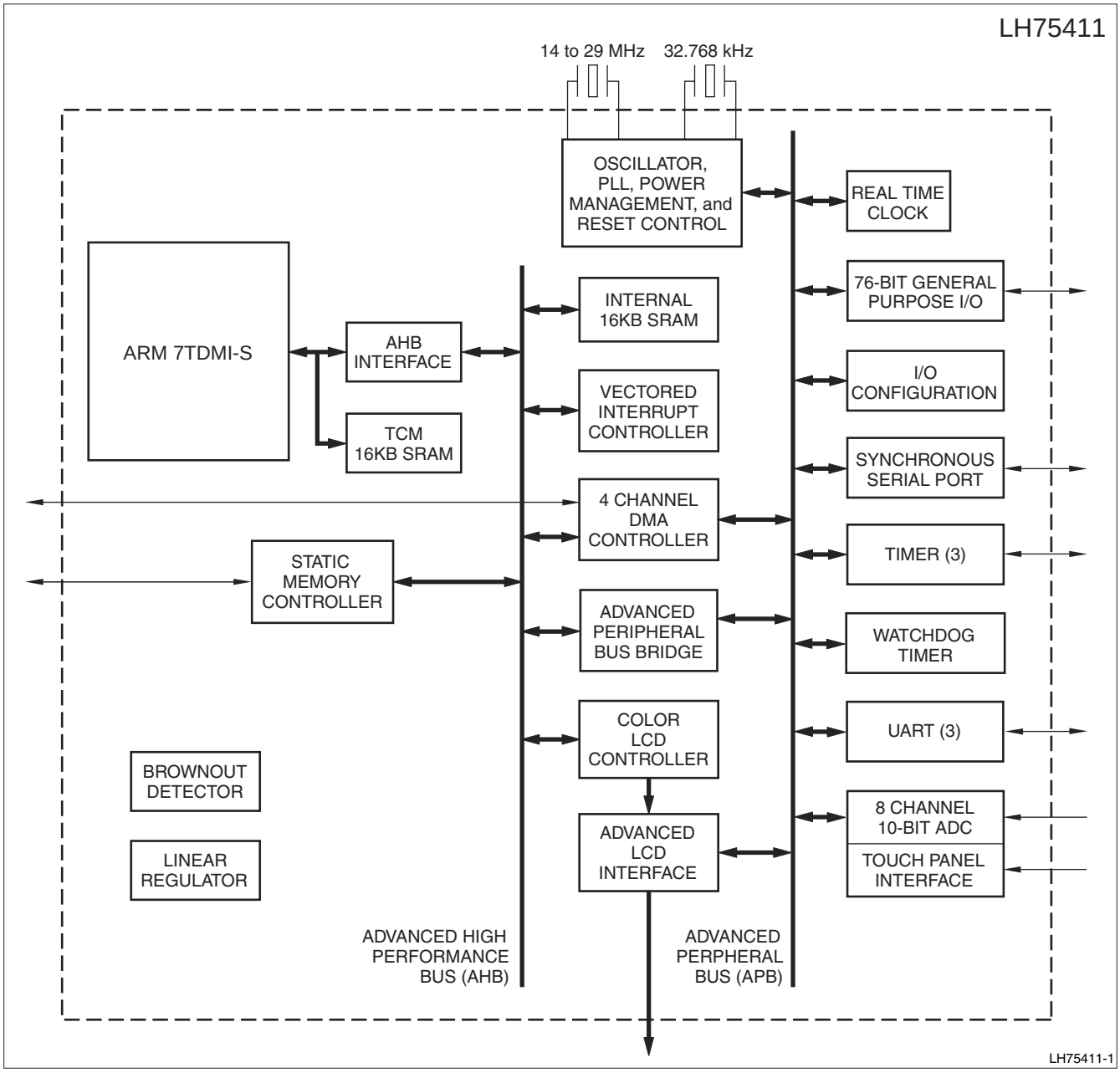


Figure 2. LH75411 Block Diagram

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP	LCDHRLP		8 mA	Bidirectional		
129	PH5	LCDFP	LCDSPS		8 mA	Bidirectional		
130	PH4	LCDEN	LCDSPL		8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:
1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP			8 mA	Bidirectional		
129	PH5	LCDFP			8 mA	Bidirectional		
130	PH4	LCDEN			8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:
1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V ±10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWE R CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWE R CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pins have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

Reset Generation

EXTERNAL RESETS

Two external signals generate resets to the ARM7TDMI-S core:

- nPOR sets all internal registers to their default state when asserted. It is used as a Power-On Reset.
- nRESETIN sets all internal registers, except the JTAG circuitry, to their default state when asserted.

When nPOR is asserted, nRESETIN defines the microcontroller Test Mode. When nPOR is released, nRESETIN behaves during Reset as described previously.

INTERNAL RESETS

There are two types of Internal Resets generated:

- System Reset
- RTC Reset.

System and RTC Resets are asserted by:

- An External Reset (a logic LOW signal on the external nRESETIN or nPOR input pin)
- A signal from the internal Watchdog Timer
- A Soft Reset.

The reset latency depends on the PLL lock state.

AHB Master Priority and Arbitration

The LH75400/01/10/11 microcontrollers have three AHB masters:

- ARM processor
- DMAC
- LCD Controller.

Each AHB master has a priority level that is permanent and cannot change.

Table 9. Bus Master Priority

PRIORITY	BUS MASTER PRIORITY
1 (Highest)	Color LCDC (LH75401 and LH75411) LCDC (LH75400 and LH75410)
2	DMAC
3 (Lowest)	ARM7TDMI-S Core (Default)

Memory Interface Architecture

The LH75400/01/10/11 microcontrollers provide the following data-path management resources on chip:

- AHB and APB data buses
- 16KB of zero-wait-state TCM SRAM accessible via processor
- 16KB of internal SRAM accessible via processor, DMAC, and LCDC
- A Static Memory Controller (SMC) that controls access to external memory
- A 4-stream general-purpose DMAC.

All external and internal system resources are memory-mapped. This memory map partition has three views, based on the setting of the REMAP bits in the Reset, Clock, and Power Controller (RCPC).

The second partitioning of memory space is the dividing of the segments into sections. The external memory segment is divided into eight 64MB sections, of which the first four are used, each having a chip select associated with it. Access to any of the last four sections does not result in an external bus access and does not cause a memory abort. The peripheral register segment is divided into 4KB peripheral sections, 21 of which are assigned to peripherals.

Table 10. Memory Mapping

ADDRESS	REMAP = 00 (DEFAULT)	REMAP = 01	REMAP = 10
0x00000000	External Memory	Internal SRAM	TCM SRAM
0x20000000	Reserved	Reserved	Reserved
0x40000000	External Memory	External Memory	External Memory
0x60000000	Internal SRAM	Internal SRAM	Internal SRAM
0x80000000	TCM SRAM	TCM SRAM	TCM SRAM
0xA0000000	Reserved	Reserved	Reserved
0xC0000000	Reserved	Reserved	Reserved
0xE0000000 - 0xFFFBFFFF	Reserved	Reserved	Reserved

Vectored Interrupt Controller (VIC)

All internal and external interrupts are routed to the VIC, where hardware determines the interrupt priority (see Table 14). The VIC is also where the appropriate signal to the processor (IRQ or FIQ) is generated. The processor services the interrupt as either a vectored interrupt or a default-vectored interrupt.

The VIC accepts inputs from 32 interrupt source lines:

- Seven external
- Twenty-three internal
- Two used as software interrupts.

All 32 interrupt source lines can be enabled, disabled, and cleared individually, and individual status can be determined. On reset, all interrupts are disabled.

The VIC also accepts software-generated interrupts. Software-generated interrupts use the same enabling control as hardware-generated interrupts.

The VIC provides 32 interrupts:

- 16 vectored interrupts
- 16 or more default-vectored interrupts.

Any of the 32 interrupt source lines can be assigned to any of the 16 interrupt vectors. Any line not explicitly assigned to an interrupt vector is processed as a default-vectored interrupt. At reset, all 32 lines become default-vectored interrupts.

Each interrupt line can be explicitly identified as an IRQ (default) or FIQ interrupt. Vectored-interrupt servicing is only available for IRQ interrupts.

Table 14. Interrupt Channels

POSITION	DESCRIPTION	SOURCE
0	WDT	Watchdog Timer
1	Not Used	Available as a software interrupt
2	ARM7 DBGCOMMRX	Sourced by the ARM7TDMI-S Core
3	ARM7 DBGCOMMTX	Sourced by the ARM7TDMI-S Core
4	Timer0 Combined	Timer0
5	Timer1 Combined	Timer1
6	Timer2 Combined	Timer2
7	External Interrupt 0	Sourced by the GPIO Block
8	External Interrupt 1	Sourced by the GPIO Block
9	External Interrupt 2	Sourced by the GPIO Block
10	External Interrupt 3	Sourced by the GPIO Block
11	External Interrupt 4	Sourced by the GPIO Block
12	External Interrupt 5	Sourced by the GPIO Block
13	External Interrupt 6	Sourced by the GPIO Block
14	Not Used	Available as a software interrupt
15	RTC_ALARM	Real Time Clock
16	ADC TSCIRQ (combined)	Analog-to-Digital Converter
17	ADC BrownOutINTR	Brown Out Detector
18	ADC PenIRQ	Analog-to-Digital Converter
19	LCD	LCD Controller
20	SSPTXINTR	Synchronous Serial Port
21	SSPRXINTR	Synchronous Serial Port
22	SSPRORINTR	Synchronous Serial Port
23	SSPRXTOINTR	Synchronous Serial Port
24	SSPINTR	Synchronous Serial Port
25	UART1 UARTRXINTR	UART1
26	UART1 UARTTXINTR	UART1
27	UART1 UARTINTR	UART1
28	UART0 UARTINTR	UART0
29	UART2 Interrupt	UART2
30	DMA	DMA
31	CAN	CAN (LH75401/LH75400) Reserved (LH75411/LH75410)

Device Pin Multiplexing

Table 17. LCD Panel Signal Multiplexing

EXTERNAL PIN	4-BIT STN (MONOCHROME)		8-BIT STN SINGLE PANEL (MONOCHROME)
	SINGLE PANEL	DUAL PANEL	
LVCVD11	Reserved	MLSTN3	Reserved
LVCVD10	Reserved	MLSTN2	Reserved
LVCVD9	Reserved	MLSTN1	Reserved
LVCVD8	Reserved	MLSTN0	Reserved
LVCVD7	Reserved	Reserved	MUSTN7
LVCVD6	Reserved	Reserved	MUSTN6
LVCVD5	Reserved	Reserved	MUSTN5
LVCVD4	Reserved	Reserved	MUSTN4
LVCVD3	MUSTN3	MUSTN3	MUSTN3
LVCVD2	MUSTN2	MUSTN2	MUSTN2
LVCVD1	MUSTN1	MUSTN1	MUSTN1
LVCVD0	MUSTN0	MUSTN0	MUSTN0

NOTES:
1. MUSTN = Mono upper panel STN, dual and/or single panel.
2. MLSTN = Mono lower panel STN, dual panel only.

Table 18. LCD External Pin Multiplexing (LH75401 and LH75411)

EXTERNAL PIN	DEFAULT MODE (NO LCD)	4-BIT MONO STN MODE		8-BIT STN MODE	TFT MODE	ALI MODE
		SINGLE	DUAL			
PG4/LCDVEEEN/LCDMOD	PG4	LCDVEEEN	LCDVEEEN	LCDVEEEN	LCDVEEEN	LCDMOD
PG3/LCDVDDEN	PG3	LCDVDDEN	LCDVDDEN	LCDVDDEN	LCDVDDEN	LCDVDDEN
PG2/LCDDSPLEN/LCDREV	PG2	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN	LCDREV
PG1/LCDCLS	PG1	PG1	PG1	PG1	PG1	LCDCLS
PG0/LCDPS	PG0	PG0	PG0	PG0	PG0	LCDPS
PH7/LCDDCLK	PH7	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK
PH6/LCDLP/LCDHRLP	PH6	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP
PH5/LCDFP/LCDSPS	PH5	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP
PH4/LCDEN/LCDEN	PH4	LCDEN	LCDEN	LCDEN	LCDEN	LCDEN
PH3/LCDVD11	PH3	PH3	MLSTN3	PH3	LCDVD11	LCDVD11
PH2/LCDVD10	PH2	PH2	MLSTN2	PH2	LCDVD10	LCDVD10
PH1/LCDVD9	PH1	PH1	MLSTN1	PH1	LCDVD9	LCDVD9
PH0/LCDVD8	PH0	PH0	MLSTN0	PH0	LCDVD8	LCDVD8
PI7/LCDVD7	PI7	PI7	PI7	STN7	LCDVD7	LCDVD7
PI6/LCDVD6	PI6	PI6	PI6	STN6	LCDVD6	LCDVD6
PI5/LCDVD5	PI5	PI5	PI5	STN5	LCDVD5	LCDVD5
PI4/LCDVD4	PI4	PI4	PI4	STN4	LCDVD4	LCDVD4
PI3/LCDVD3	PI3	MUSTN3	MUSTN3	STN3	LCDVD3	LCDVD3
PI2/LCDVD2	PI2	MUSTN2	MUSTN2	STN2	LCDVD2	LCDVD2
PI1/LCDVD1	PI1	MUSTN1	MUSTN1	STN1	LCDVD1	LCDVD1
PI0/LCDVD0	PI0	MUSTN0	MUSTN0	STN0	LCDVD0	LCDVD0

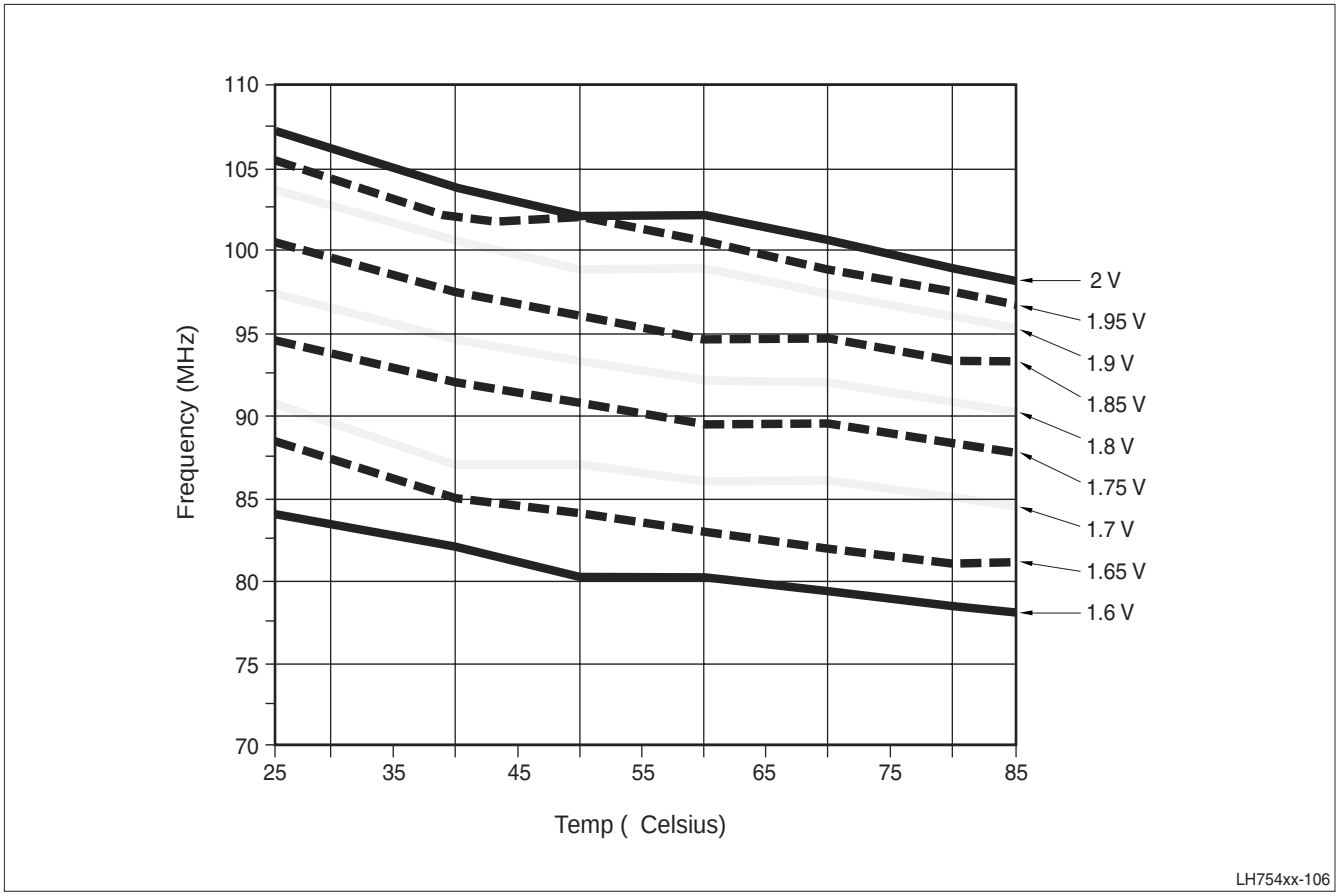


Figure 10. Maximum Core Frequency versus Voltage and Temperature

Very Low Operati ng Temperatures and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

SHARP recommends that users implementing a system to meet low industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (ie, noise immunity of the clock input to the SoC.

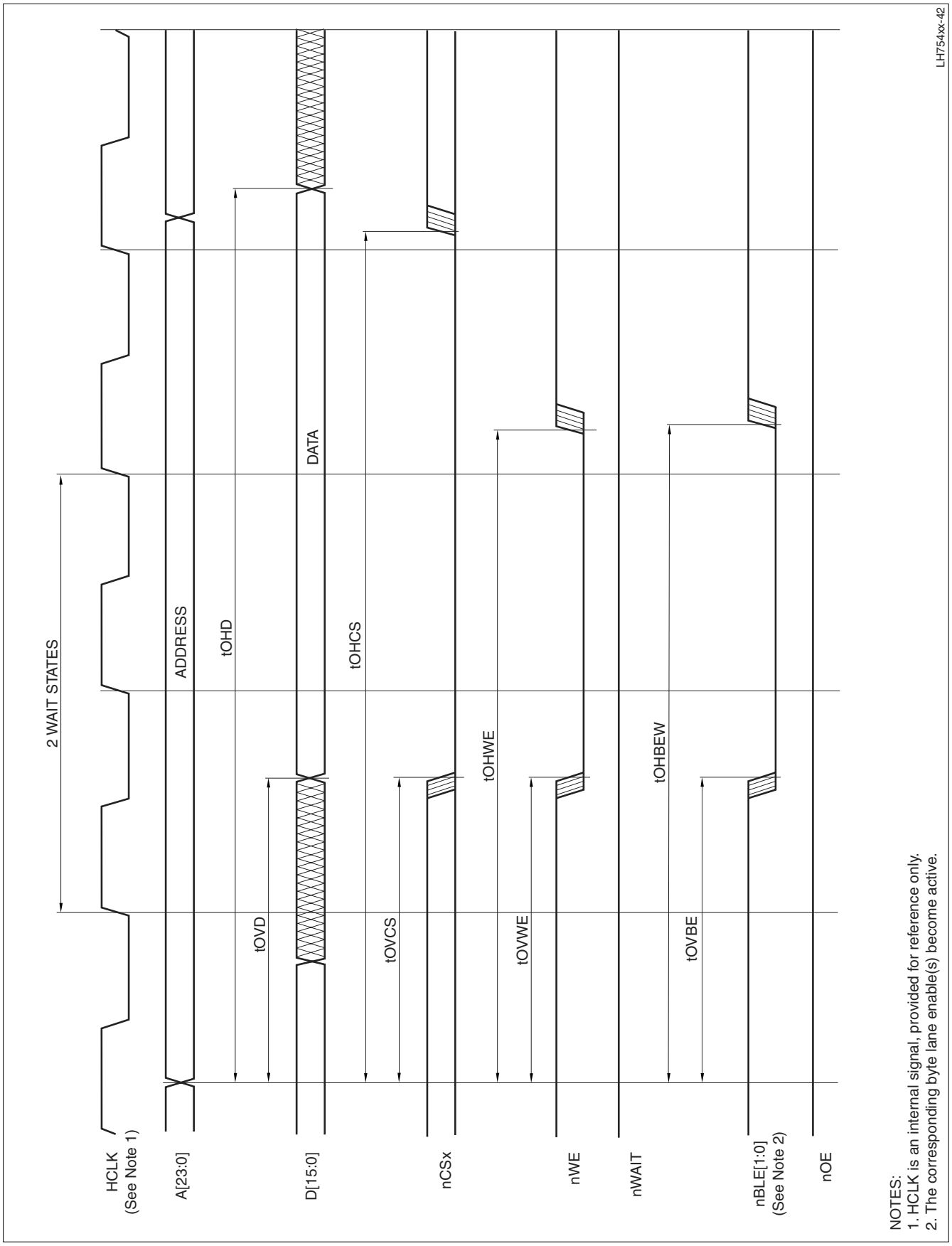


Figure 14. External Static Memory Write, Two Wait States

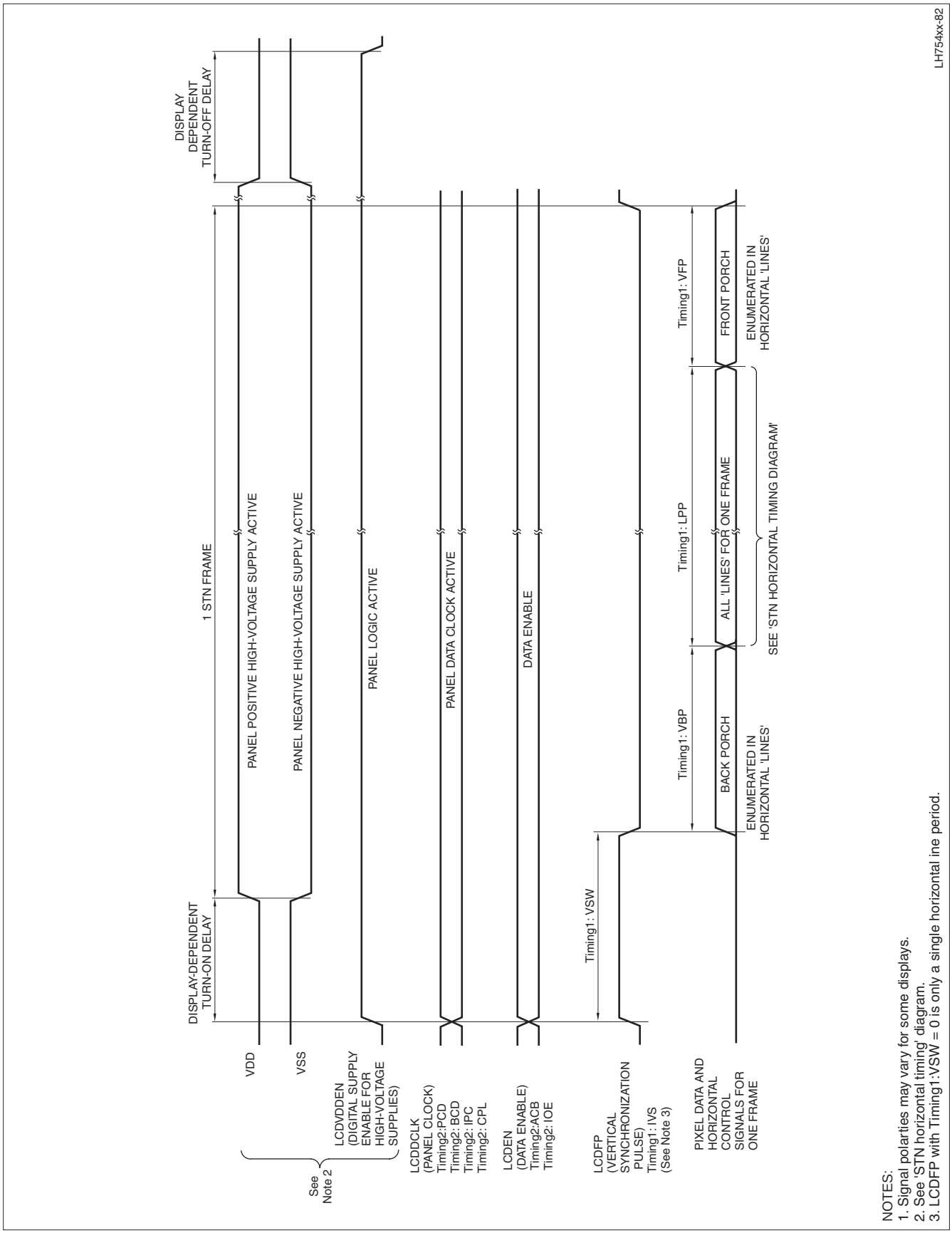


Figure 21. STN Vert ical Timing Diagram

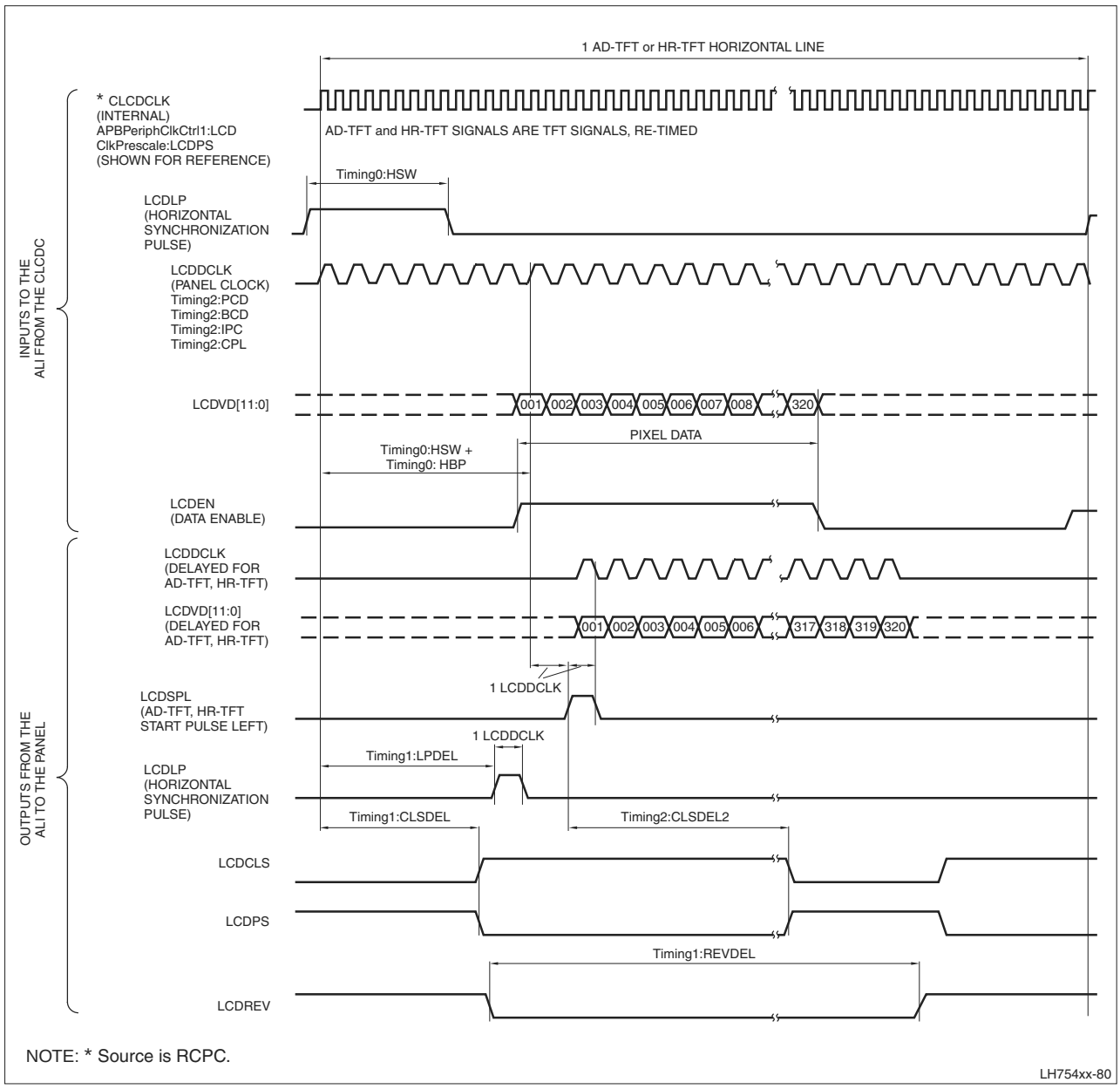


Figure 24. AD-TFT, HR-TFT Horizontal Timing Diagram

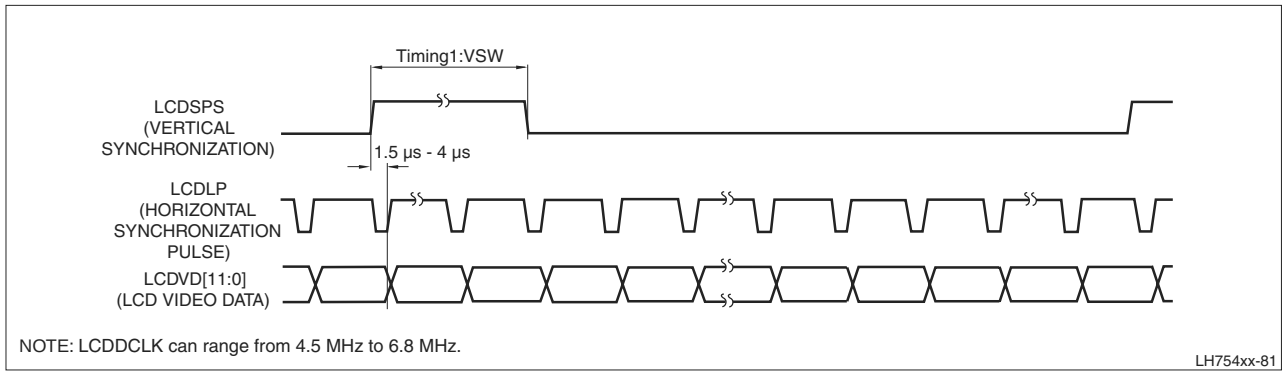
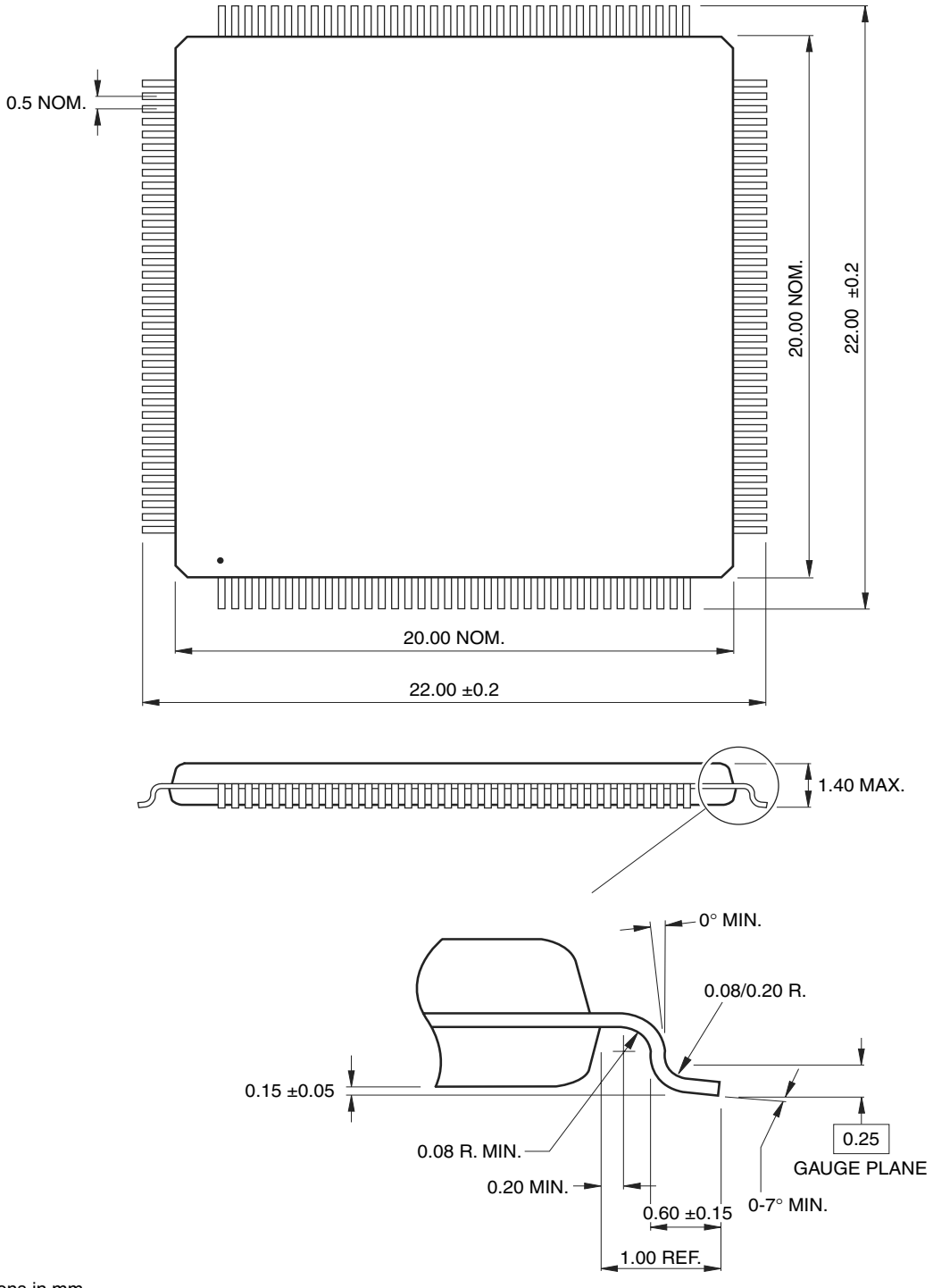


Figure 25. AD-TFT, HR-TFT Vertical Timing Diagram

PACKAGE SPECIFICATIONS

144LQFP (JEDEC MS-026) TOP VIEW



NOTE: Dimensions in mm.

144LQFP-JEDEC

Figure 28. 144-pin LQFP