



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, EBI/EMI, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75401n0q100c0

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP	LCDHRLP		8 mA	Bidirectional		
129	PH5	LCDFP	LCDSPS		8 mA	Bidirectional		
130	PH4	LCDEN	LCDSPL		8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V $\pm$ 10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEN	Output	Analog Supply Enable (AC Bias Signal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

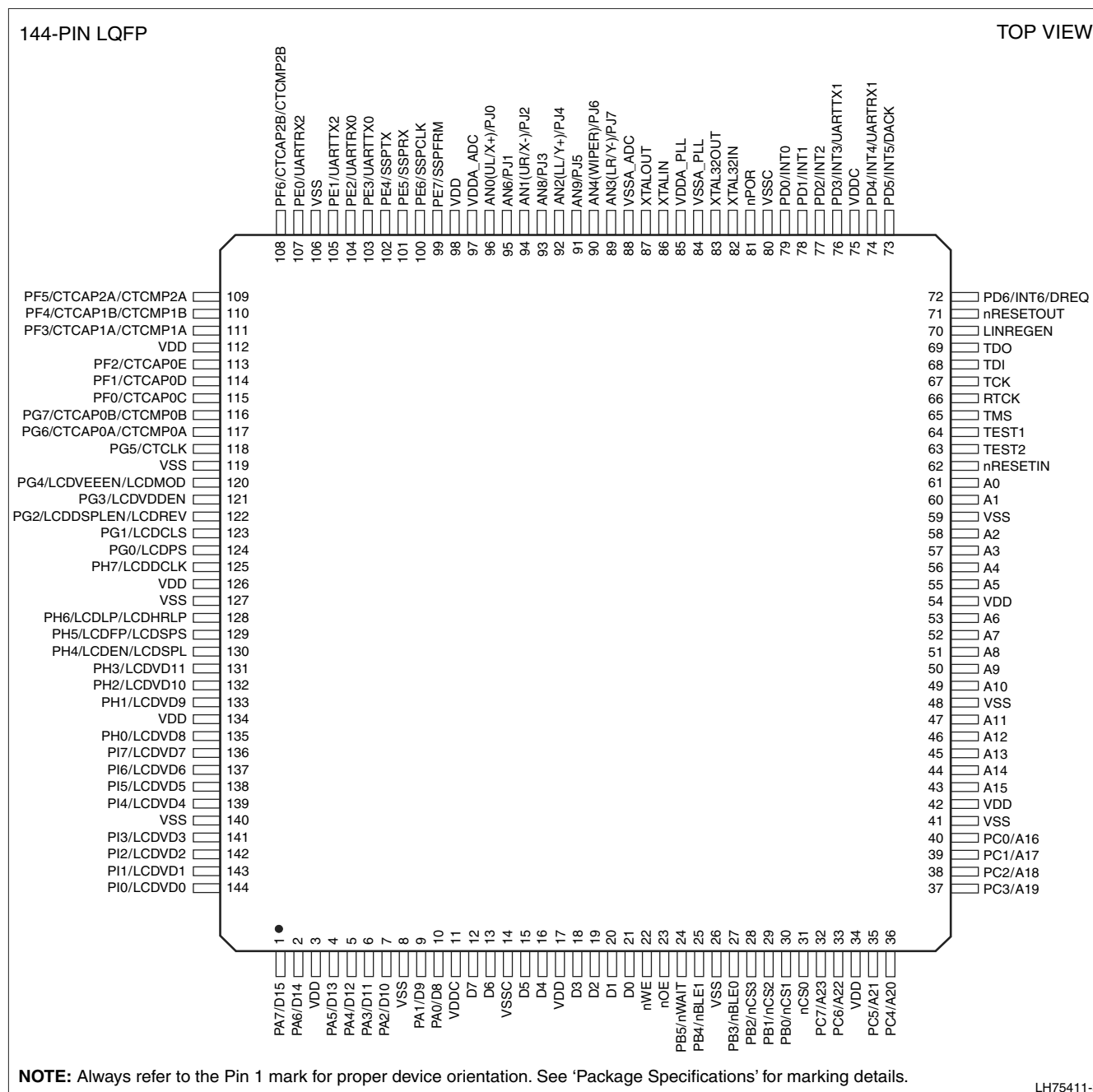
Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:

1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75411



NOTE: Always refer to the Pin 1 mark for proper device orientation. See 'Package Specifications' for marking details.

LH75411-3

Figure 6. LH75411 Pin Diagram

Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		
123	PG1	LCDCLS			8 mA	Bidirectional		
124	PG0	LCDPS			8 mA	Bidirectional		
125	PH7	LCDDCLK			8 mA	Bidirectional		

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEN	Output	Analog Supply Enable (AC Bias Signal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
104	UARTRX0	Input	UART0 Received Serial Data Input	1
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:

1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75410

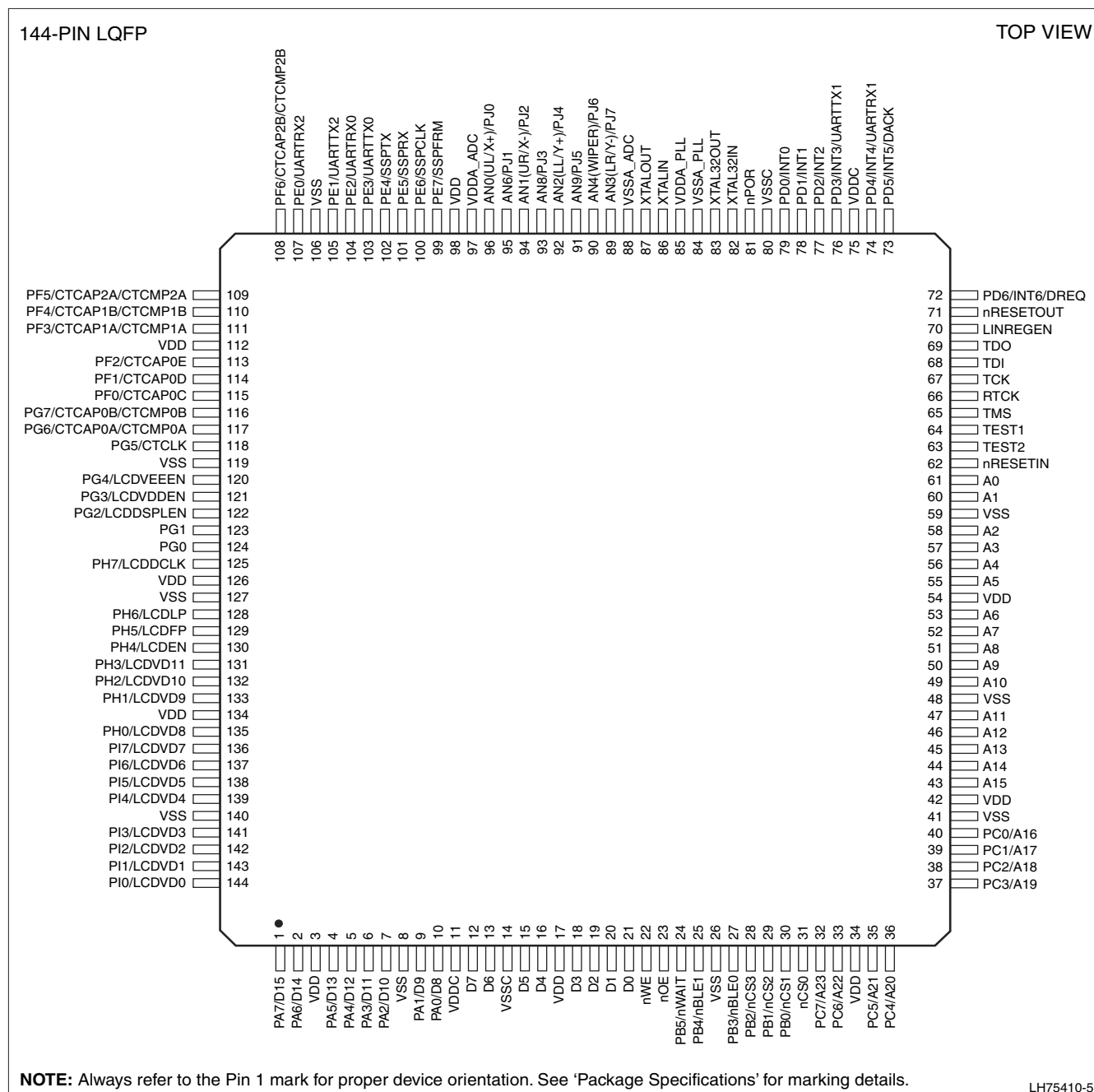


Figure 8. LH75410 Pin Diagram

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN			8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN			8 mA	Bidirectional		
123	PG1				8 mA	Bidirectional		
124	PG0				8 mA	Bidirectional		

CAN 2.0B FEATURES

- Full compliance with 2.0A and 2.0B Bosch specifications
- Supports 11-bit and 29-bit identifiers
- Supports bit rates up to 1Mbit/s
- 64-byte receive FIFO
- Software-driven bit-rate detection for hot plug-in support
- Single-shot transmission option
- Acceptance filtering
- Listen Only Mode
- Reception of 'own' messages
- Error interrupt generated for each CAN bus error
- Arbitration-lost interrupt with record of bit position
- Read/write error counters
- Last error register
- Programmable error-limit warning.

**Analog-to-Digital Converter (ADC)/
Brownout Detector**

The ADC is an AMBA-compliant peripheral that connects as a slave to the APB. The ADC block consists of an 8-channel, 10-bit Analog-to-Digital Converter with integrated Touch Screen Controller. The complete Touch Screen interface is achieved by combining the front-end biasing, control circuitry with analog-to-digital conversion, reference generation, and digital control.

The ADC also has a programmable measurement clock derived from the system clock. The clock drives the measurement sequencer and the successive-approximation circuitry.

The ADC includes a Brownout Detector. The Brownout Detector is an asynchronous comparator that compares a divided version of the 3.3 V supply and a bandgap-derived reference voltage. If the supply dips below a Trip point, the Brownout Detector sets a status register bit. The status bit is wired to the VIC and can interrupt the processor core. This allows the Host Controller to warn users of an impending shutdown and may provide the ADC with sufficient time to save its state.

ADC/BROWNOUT DETECTOR FEATURES

- 10-bit fully differential Successive Approximation Register (SAR) with integrated sample/hold
- 8-channel multiplexer for routing user-selected inputs to the ADC in Single Ended and Differential Modes
- 16-entry × 16-bit-wide FIFO that holds the 10-bit ADC output and a 4-bit tag number
- Front bias-and-control network for Touch Screen interface and support functions compatible with industry-standard 4- and 5-wire touch-sensitive panels

- Touch-pressure sensing circuits
- Pen-down sensing circuit and interrupt generator
- Voltage-reference generator that is independently controlled
- Conversion automation function to minimize controller interrupt overhead
- Brownout Detector.

Synchronous Serial Port (SSP)

The SSP is a master-only interface for synchronous serial communication with slave peripheral devices that have a Motorola SPI, National Semiconductor Microwire, or Texas Instruments DSP-compatible Synchronous Serial Interface (SSI).

The SSP performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with internal FIFO memories. These memories store eight 16-bit values independently in both transmit and receive modes. During transmission:

- Data writes to the transmit FIFO via the APB interface.
- The transmit data is queued for parallel-to-serial conversion onto the transmit interface.
- The transmit logic formats the data into the appropriate frame type:
 - Motorola SPI
 - National Semiconductor Microwire
 - Texas Instruments DSP-compatible SSI.

SSP FEATURES

- SSI in Master Only Mode. The SSP performs serial communications as a master device in one of three modes:
 - Motorola SPI
 - Texas Instruments DSP-compatible synchronous serial interface
 - National Semiconductor Microwire.
- Two 16-bit-wide, 8-entry-deep FIFOs, one for data transmission and one for data reception.
- Supports interrupt-driven data transfers that are greater than the FIFO watermark.
- Programmable clock bit rate.
- Programmable data frame size, from 4 to 16 bits long, depending on the size of data programmed. Each frame transmits starting with the most-significant bit.
- Four interrupts, each of which can be individually enabled or disabled using the SSP Control Register bits. A combined interrupt is also generated as an OR function of the individual interrupt requests.
- Loopback Test Mode.

Table 13. SSP Modes

MODE	DESCRIPTION	DATA TRANSFERS
Motorola SPI	For communications with Motorola SPI-compatible devices. Clock polarity and phase are programmable.	Full-duplex, 4-wire synchronous
SSI	For communications with Texas Instruments DSP-compatible Serial Synchronous Interface devices.	Full-duplex, 4-wire synchronous
National Semiconductor Microwire	For communications with National Semiconductor Microwire-compatible devices.	Half-duplex synchronous, using 8-bit control messages

Watchdog Timer (WDT)

The WDT consists of a 32-bit down-counter that allows a selectable time-out interval to detect malfunctions. The timer must be reset by software periodically. Otherwise, a time-out occurs, interrupting the system. If the interrupt is not serviced within the timeout period, the WDT triggers the RCPC to generate a System Reset. If the WDT times out, it sets a bit in the RCPC Reset Status Register.

The WDT supports 16 selectable time intervals, for a time-out of 216 through 231 system clock cycles. All Control and Status Registers for the Watchdog Timer are accessed through the APB.

WDT FEATURES

- Counter generates an interrupt at a set interval and the count reloads from the pre-set value after reaching zero.
- Default timeout period is set to the minimum timeout of 216 system clock cycles.
- WDT is driven by the APB.
- Built-in protection mechanism guards against interrupt-service failure.
- WDT can be programmed to trigger a System Reset on a timeout.
- WDT can be programmed to trigger an interrupt on the first timeout; then, if the service routine fails to clear the interrupt, the next WDT timeout triggers a System Reset.

Analog-To-Digital Converter Electrical Characteristics

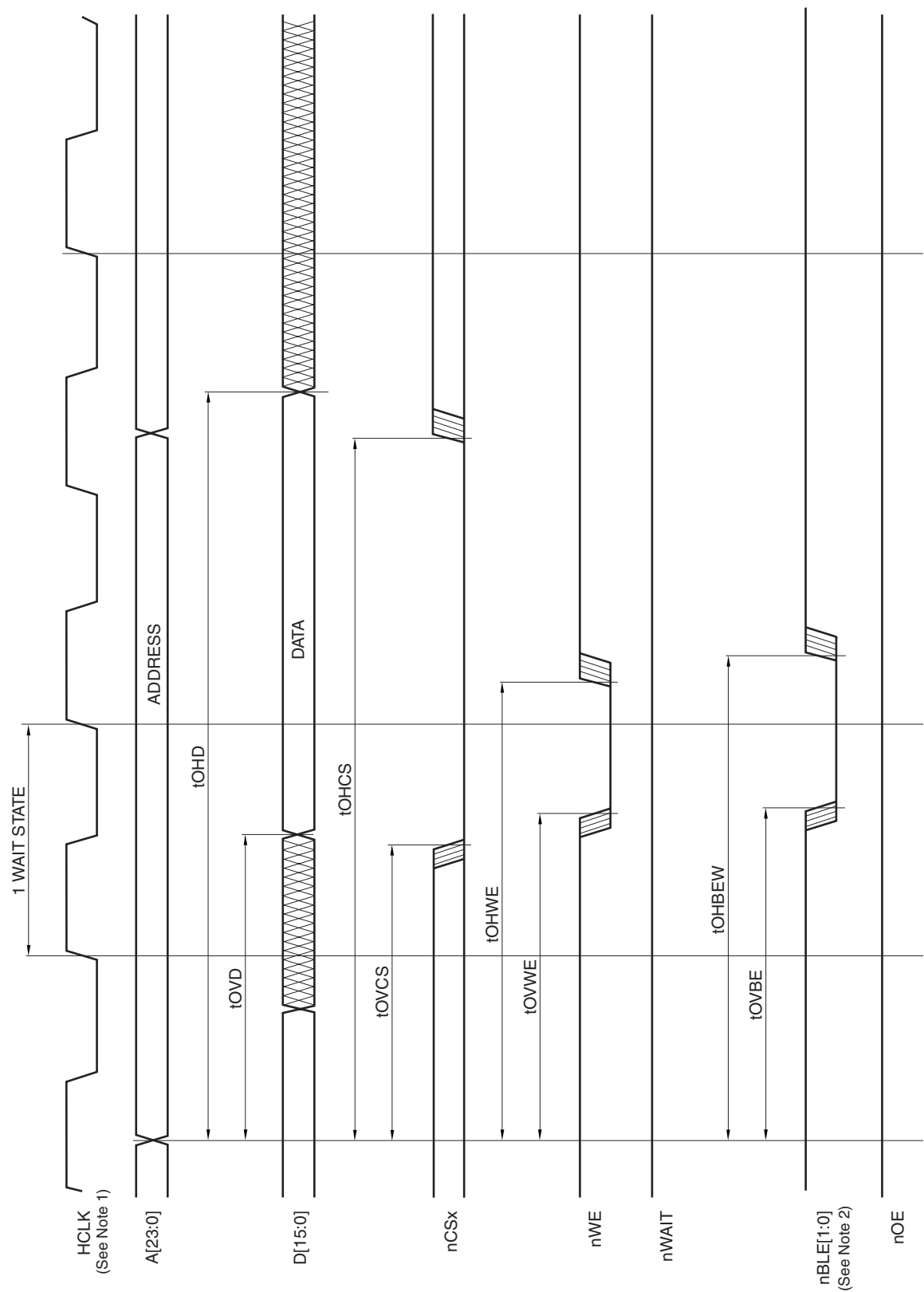
Table 25 shows the derated specifications for extended temperature operation. See Figure 11 for the ADC transfer characteristics.

Table 25. ADC Electrical Characteristics at Industrial Operating Range

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Clk Frequency	500		5,000	ns	
Differential Non-Linearity	-0.99		4.5	LSB	
Integral Non-Linearity	-3.5		+3.5	LSB	
Offset Error	-35		+35	mV	
Gain Error	-4.0		4.0	LSB	
On-chip Voltage Reference (VREF)	1.85	2.0	2.15	V	
Negative Reference Input (VREF-)	VSSA	VSSA	(VREF+) -1.0	V	2
Positive Reference Input (VREF+)	(VREF-) +1.0	VREF	VDDA	V	2
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDA	V	3
Analog Input Current			5	μA	
Reference Input Current			5	μA	
Analog input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDA		590		μA	
Standby Current		180		μA	4
Stop Current, VDDA		< 1		μA	
Brown Out Trip Point		2.63		V	
Brown Out Hysteresis		120		mV	
Operating Temperature	-40		85	°C	

NOTES:

1. The analog section of the ADC takes $16 \times A2DCLK$ cycles per conversion, plus $1 \times A2DCLK$ cycles to be made available in the PCLK domain.
An additional $3 \times PCLK$ cycles are required before being available on the APB.
2. The internal voltage reference is driven to nominal value $VREF = 2.0$ V. Using the Reference Multiplexer, alternative low impedance ($RS < 500$) voltages can be selected as reference voltages. The range of voltages allowed are specified above. However, the on-chip reference cannot drive the ADC unless the reference buffer is switched on.
3. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds $VREF+$ or is below $VREF-$, the A/D result will saturate appropriately at positive or negative full scale.
Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
4. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.



NOTES:

- 1. HCLK is an internal signal, provided for reference only.
- 2. The corresponding byte lane enable(s) become active.

LH754xx-40

Figure 13. External Static Memory Write, One Wait State

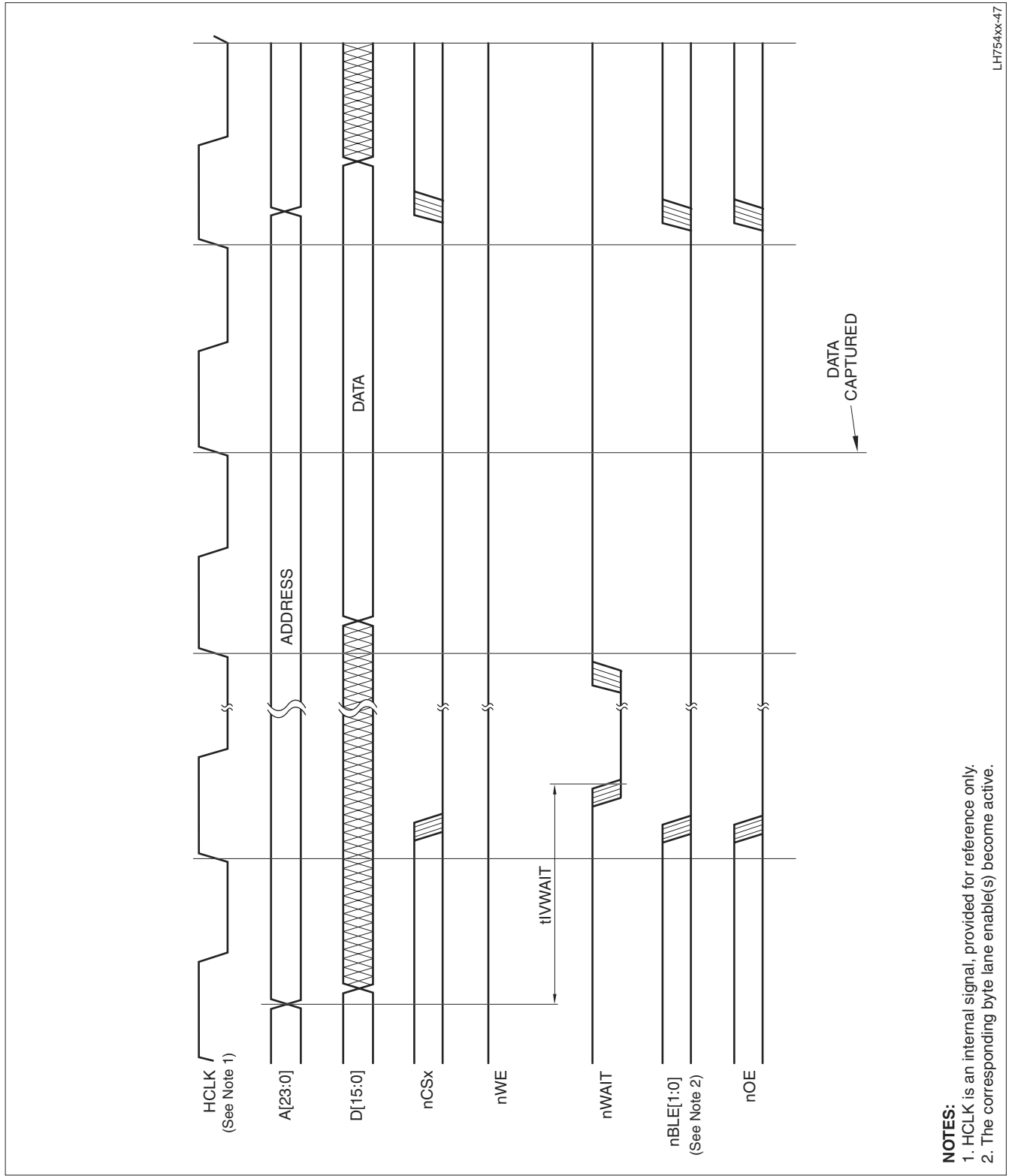


Figure 16. External Static Memory Read, nWAIT Active

DMA Controller Timing Diagrams

Figure 18 and Figure 19 show examples of DMA timing diagrams.

- Figure 18 shows the timing for a peripheral-to-memory data transfer, where

SoSize = DeSize and SoBurst = 4.

- Figure 19 shows the timing for a memory-to-peripheral data transfer, where
SoSize = DeSize and SoBurst = 4.

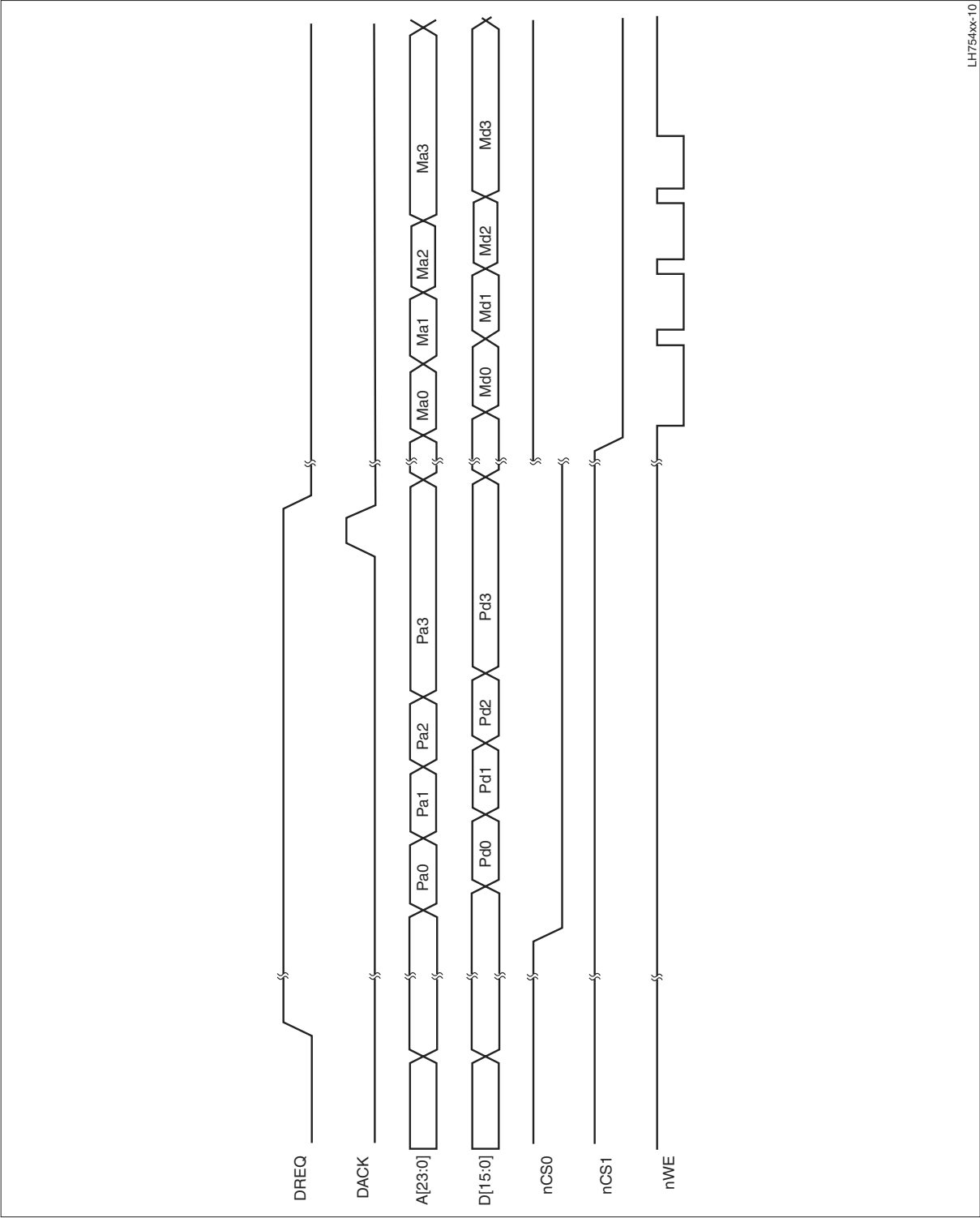


Figure 18. Peripheral-to-Memory Data-Transfer Timing

Color LCD Controller Timing Waveforms

This section describes typical output waveform diagrams for the CLCDC and the Advanced LCD Interface.

STN HORIZONTAL TIMING

Figure 20 shows typical horizontal timing waveforms for STN panels. In this figure, the CLCDC Clock (an input to the CLCDC) is scaled within the CLCDC and used to produce the LCDDCLK output. Programmable registers in the CLCDC set the timings (in terms of LCDDCLK pulses) to produce the other signals that control an STN display.

For example, Figure 20 shows that the duration of the LCDLP signal is controlled by Timing0:HSW (the HSW bit field in the Timing0 Register). Figure 20 also shows that the polarity of the LCDLP signal is set by Timing2:IHS.

STN VERTICAL TIMING

Figure 21 shows typical vertical timing waveforms for STN panels.

TFT HORIZONTAL TIMING

Figure 22 shows typical horizontal timing waveforms for TFT panels.

TFT VERTICAL TIMING

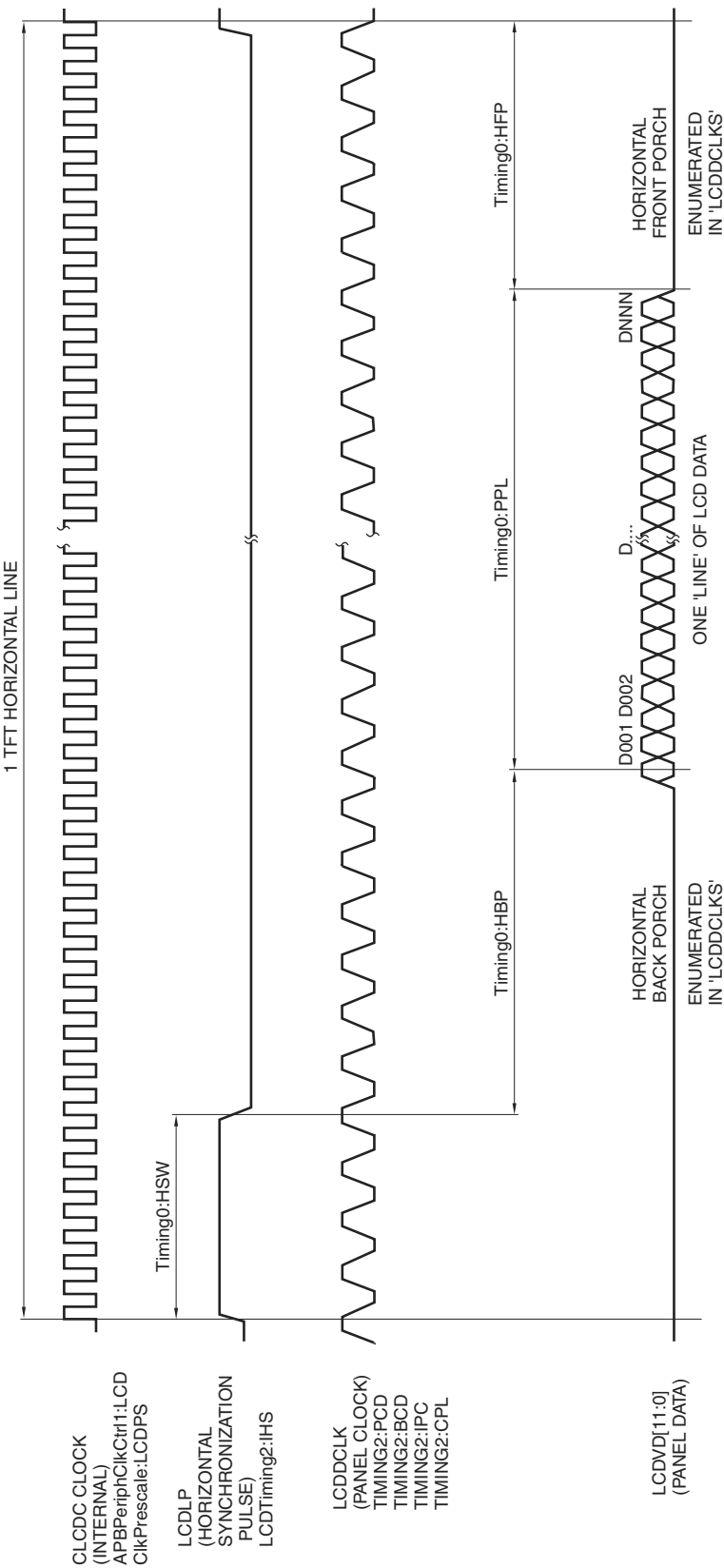
Figure 23 shows typical vertical timing waveforms for TFT panels.

AD-TFT/HR-TFT HORIZONTAL TIMING WAVEFORMS

Figure 24 shows typical horizontal timing waveforms for AD-TFT and HR-TFT panels. The ALI adjusts the normal TFT timing to accommodate these panels.

AD-TFT/HR-TFT VERTICAL TIMING WAVEFORMS

Figure 25 shows typical vertical timing waveforms for AD-TFT and HR-TFT panels. The power sequencing and register information is the same as for TFT vertical timing.



- NOTES:**
- 1. The CLCDC clock (from the RCPC) is scaled within the CLCDC and used to produce the LCDDCLK output. CLCDC registers set timing (in terms of LCDDCLK pulses) to produce the other signals that control a TFT display.
 - 2. The duration of the LCDLP signal is controlled by Timing0:HSW (the HSW bit field in the Timing0 Register).
 - 3. The polarity of the LCDLP signal is set by Timing2:IHS.

LH754xx-79

Figure 22. TFT Horizontal Timing Diagram

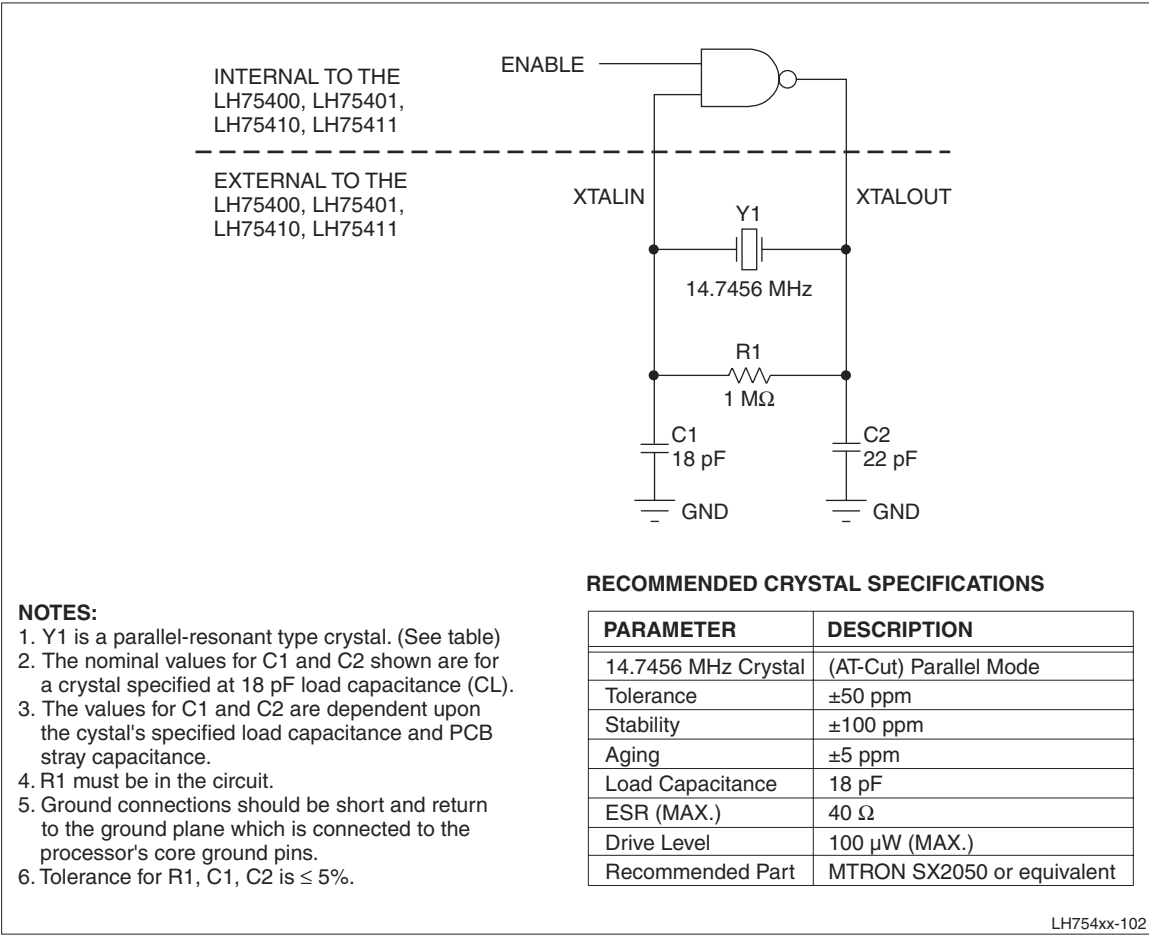


Figure 27. Suggested External Components, 14.7456 MHz Oscillator

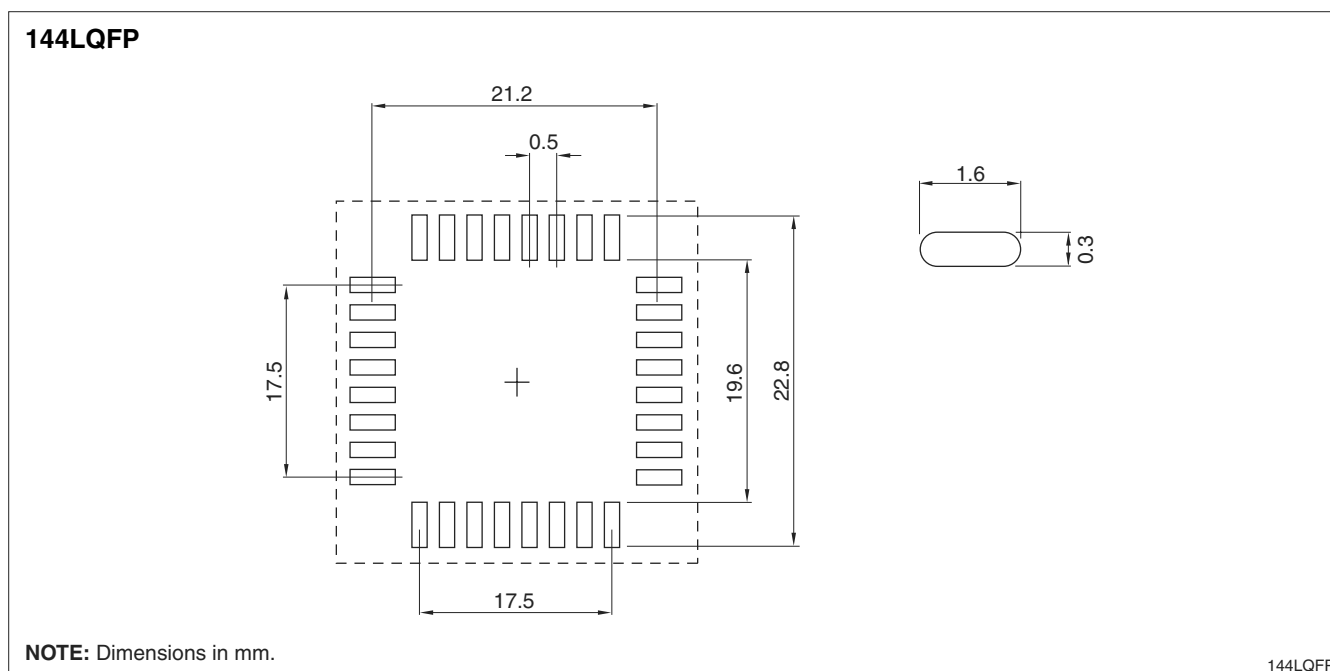


Figure 29. Recommended PCB Footprint