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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	EBI/EMI, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75410n0m100c0

LH75401 BLOCK DIAGRAM

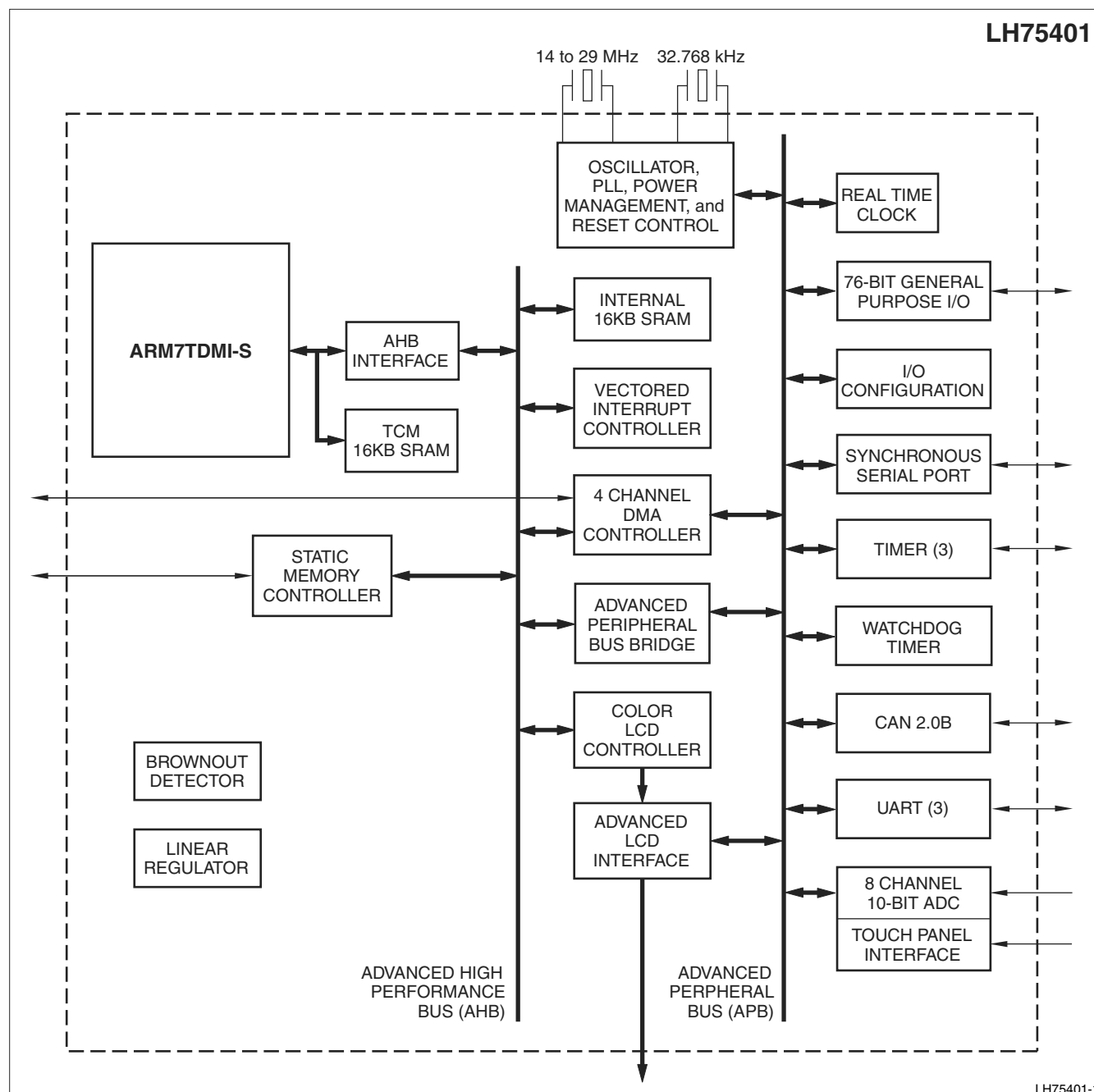


Figure 1. LH75401 Block Diagram

LH75400 BLOCK DIAGRAM

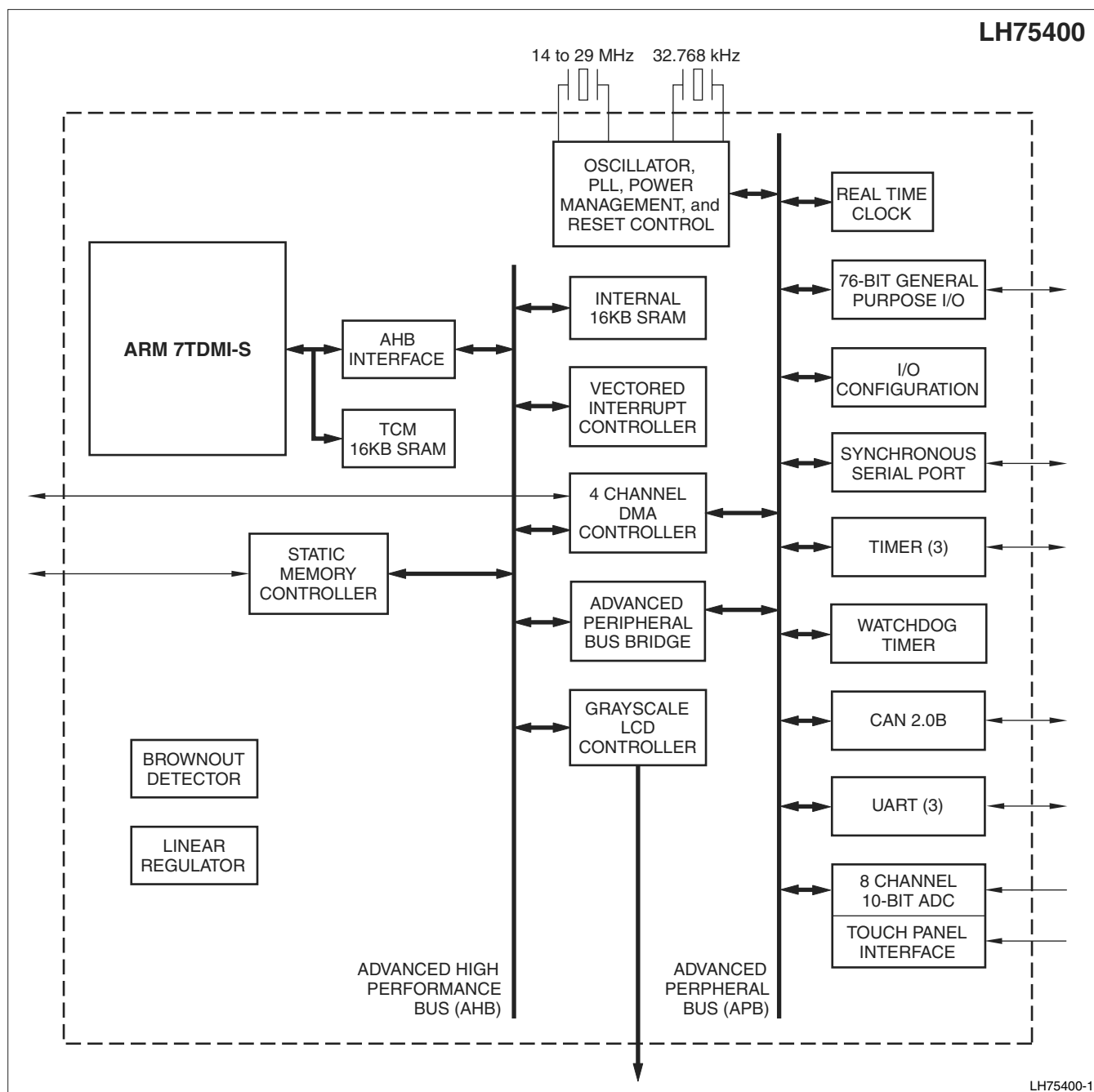


Figure 3. LH75400 Block Diagram

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	CANTX	UARTTX0		8 mA	Bidirectional	Pull-up	1
104	PE2	CANRX	UARTRX0		2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEN	Output	Analog Supply Enable (AC Bias Signal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
72 73 74 76 77 78 79	PD6 PD5 PD4 PD3 PD2 PD1 PD0	Input/Output	General Purpose I/O Signals - Port D	1
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

Table 5. LH75400 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
125	PH7	LCDDCLK			8 mA	Bidirectional		
126	VDD			Power	None			
127	VSS			Ground	None			
128	PH6	LCDLP			8 mA	Bidirectional		
129	PH5	LCDFP			8 mA	Bidirectional		
130	PH4	LCDEN			8 mA	Bidirectional		
131	PH3	LCDVD11			8 mA	Bidirectional		
132	PH2	LCDVD10			8 mA	Bidirectional		
133	PH1	LCDVD9			8 mA	Bidirectional		
134	VDD			Power	None			
135	PH0	LCDVD8			8 mA	Bidirectional		
136	PI7	LCDVD7			8 mA	Bidirectional		
137	PI6	LCDVD6			8 mA	Bidirectional		
138	PI5	LCDVD5			8 mA	Bidirectional		
139	PI4	LCDVD4			8 mA	Bidirectional		
140	VSS			Ground	None			
141	PI3	LCDVD3			8 mA	Bidirectional		
142	PI2	LCDVD2			8 mA	Bidirectional		
143	PI1	LCDVD1			8 mA	Bidirectional		
144	PI0	LCDVD0			8 mA	Bidirectional		

NOTES:

1. Signal is selectable as pull-up, pull-down, or no pull-up/pull-down via the I/O Configuration peripheral.
2. CMOS Schmitt trigger input.
3. Signals preceded with 'n' are active LOW.
4. Crystal Oscillator Inputs should be driven to 1.8 V $\pm$ 10% (MAX.)
5. LINREGEN activation requires a 0 Ω pull-up to VDD.

Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

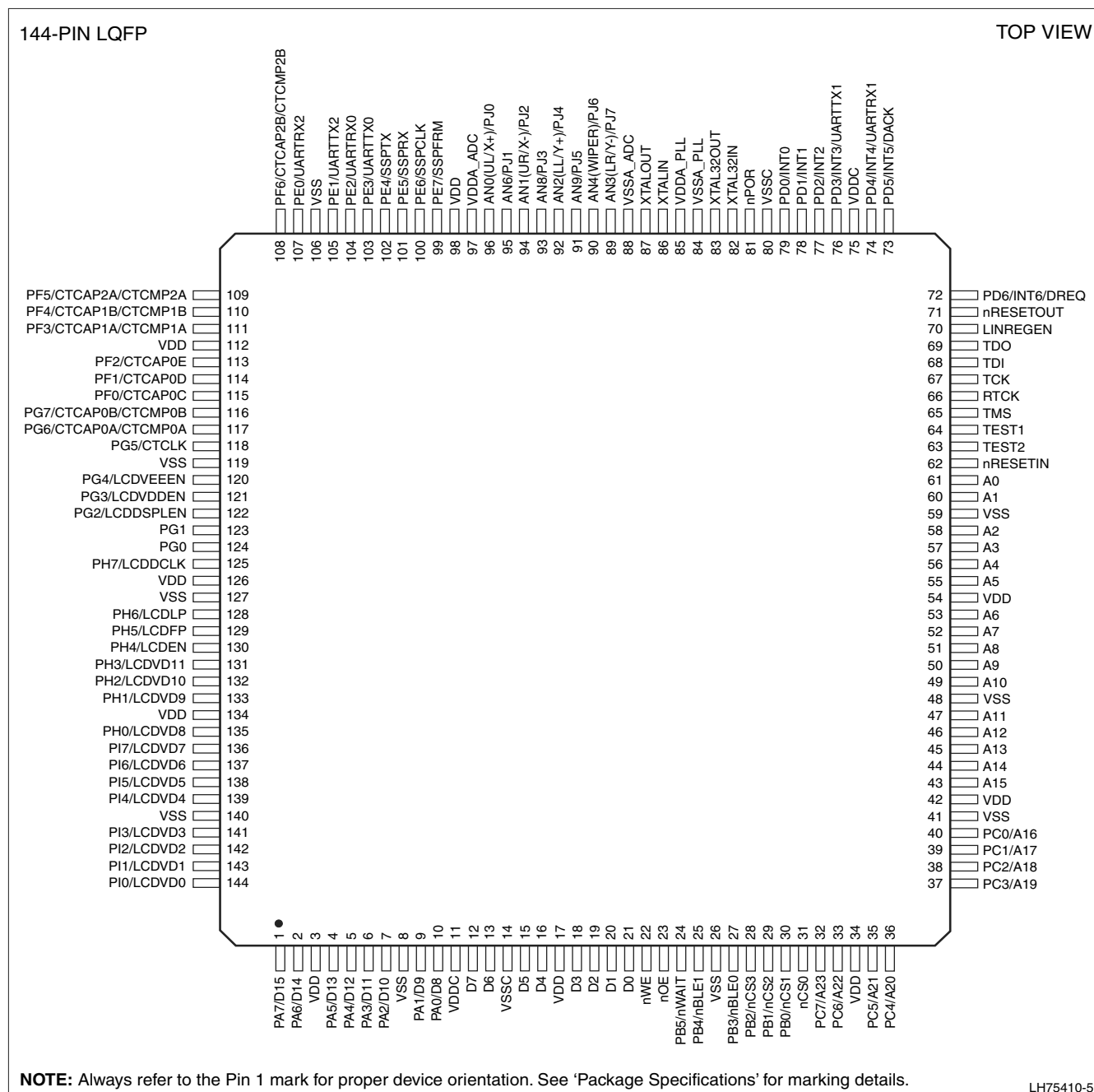
Table 6. LH75400 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:

1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

THE LH75410



NOTE: Always refer to the Pin 1 mark for proper device orientation. See 'Package Specifications' for marking details.

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Figure 8. LH75410 Pin Diagram

Table 7. LH75410 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	UARTTX0			8 mA	Bidirectional	Pull-up	1
104	PE2	UARTRX0			2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN			8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN			8 mA	Bidirectional		
123	PG1				8 mA	Bidirectional		
124	PG0				8 mA	Bidirectional		

LH75410 Signal Descriptions

Table 8. LH75410 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
LCD CONTROLLER (LCDC)				
120	LCDVEEN	Output	Analog Supply Enable (AC Bias Signal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
130	LCDEN	Output	LCD Data Enable	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1

Table 19. LCD External Pin Multiplexing (LH75400 and LH75410)

EXTERNAL PIN	DEFAULT MODE (NO LCD)	4-BIT MONO STN MODE		8-BIT MONO STN MODE
		SINGLE	DUAL	
PG4/LCDVEEEN	PG4	LCDVEEEN	LCDVEEEN	LCDVEEEN
PG3/LCDVDDEN	PG3	LCDVDDEN	LCDVDDEN	LCDVDDEN
PG2/LCDDSPLEN	PG2	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN
PG1	PG1	PG1	PG1	PG1
PG0	PG0	PG0	PG0	PG0
PH7/LCDDCLK	PH7	LCDDCLK	LCDDCLK	LCDDCLK
PH6/LCDLP	PH6	LCDLP	LCDLP	LCDLP
PH5/LCDFP	PH5	LCDFP	LCDFP	LCDFP
PH4/LCDEN	PH4	LCDEN	LCDEN	LCDEN
PH3/LCDVD11	PH3	PH3	MLSTN3	PH3
PH2/LCDVD10	PH2	PH2	MLSTN2	PH2
PH1/LCDVD9	PH1	PH1	MLSTN1	PH1
PH0/LCDVD8	PH0	PH0	MLSTN0	PH0
PI7/LCDVD7	PI7	PI7	PI7	MUSTN7
PI6/LCDVD6	PI6	PI6	PI6	MUSTN6
PI5/LCDVD5	PI5	PI5	PI5	MUSTN5
PI4/LCDVD4	PI4	PI4	PI4	MUSTN4
PI3/LCDVD3	PI3	MUSTN3	MUSTN3	MUSTN3
PI2/LCDVD2	PI2	MUSTN2	MUSTN2	MUSTN2
PI1/LCDVD1	PI1	MUSTN1	MUSTN1	MUSTN1
PI0/LCDVD0	PI0	MUSTN0	MUSTN0	MUSTN0

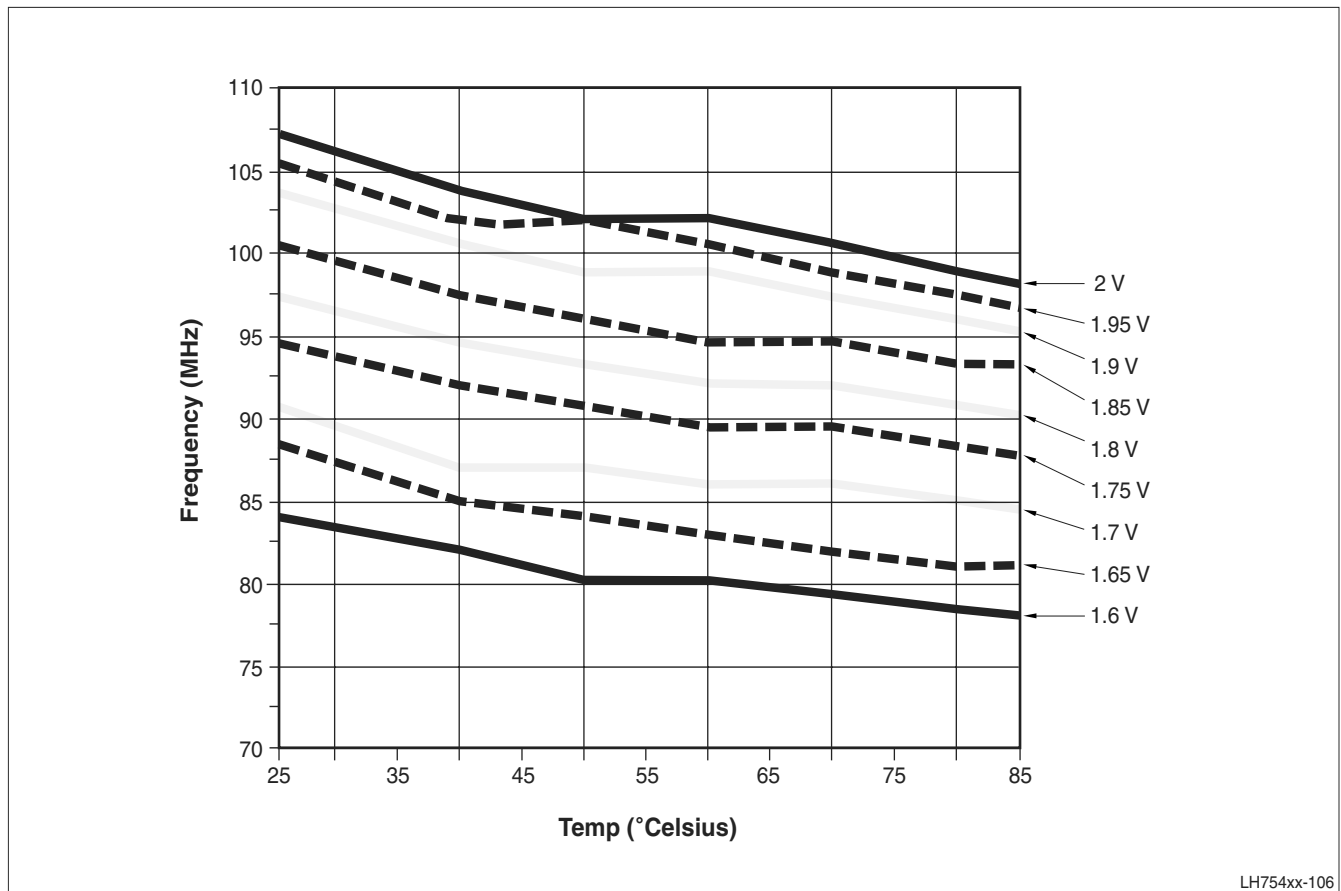


Figure 10. Maximum Core Frequency versus Voltage and Temperature

Very Low Operating Temperatures and Noise Immunity

The junction temperature, T_j , is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on T_j , and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

SHARP recommends that users implementing a system to meet low industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (ie, noise immunity of the clock input to the SoC).

POWER SUPPLY SEQUENCING

When using an external 1.8 V supply (instead of the internal 1.8 V regulator), the external 1.8 V power supply must be energized before the 3.3 V supply. Otherwise, the 1.8 V supply may not lag the 3.3 V supply by more than 10 μ s.

If a longer delay time is needed, the voltage difference between the two power supplies must be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

LINEAR REGULATOR

Although this device contains an on-board regulator, using its output to power external devices is not recommended. External loads can affect the regulator's stability and introduce noise into the supply. SHARP cannot guarantee device performance at rated speeds and temperatures with external loads connected to this supply.

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 26 were derived under the conditions presented here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All I/O loads at maximum (50 pF)
- All voltages at maximum specified values
- Maximum specified ambient temperature.

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- SPI, Timer, and UART peripherals operating; all other peripherals disabled
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate
- I/O loads at nominal
- FCLK = 51.6 MHz; HCLK = 51.6 MHz
- All voltages at typical values
- Nominal case temperature.

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 27 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the peripheral clock running at maximum frequency, typical conditions, and no I/O loads. This current is supplied by the 1.8 V power supply.

Table 26. Current Consumption by Mode

SYMBOL	PARAMETER	TYP.	UNITS
ACTIVE MODE			
ICHIP	Chip Current with Linear Regulator	50.2	mA
ICORE	Core Current without Linear Regulator	42.1	mA
IIO	I/O Current without Linear Regulator	5	mA
IANALOG	Analog Current	1.3	mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	42.7	mA
ICORE	Core Current without Linear Regulator	34.6	mA
IIO	Current drawn by I/O	0.8	mA
IANALOG	Analog Current	1.3	mA
SLEEP MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	3.9	mA
ICORE	Core Current without Linear Regulator	2.5	mA
IIO	Current drawn by I/O	400	μ A
IANALOG	Analog Current	1.2	mA
STOP1 MODE			
ISTOP	Core Current with Linear Regulator, I/O, and 14.7456 MHz osc.	2.96	mA
STOP2 MODE (RTC ON)			
ILEAK	Leakage Current, Core and I/O	34	μ A
STOP2 MODE (RTC OFF)			
ILEAK	Leakage Current, Core and I/O	18	μ A

NOTES:

1. ICHIP = Chip Current with Linear Regulator (Core + I/O)
2. ICORE, IIO, IANALOG are the respective current consumption specifications for VDDC, VDD, and VDDA.

Table 27. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
UARTs	200	μ A
RTC	5	μ A
DMA	4.1	mA
SSP	500	μ A
Counter/Timers	200	μ A
LCD	2.2	mA

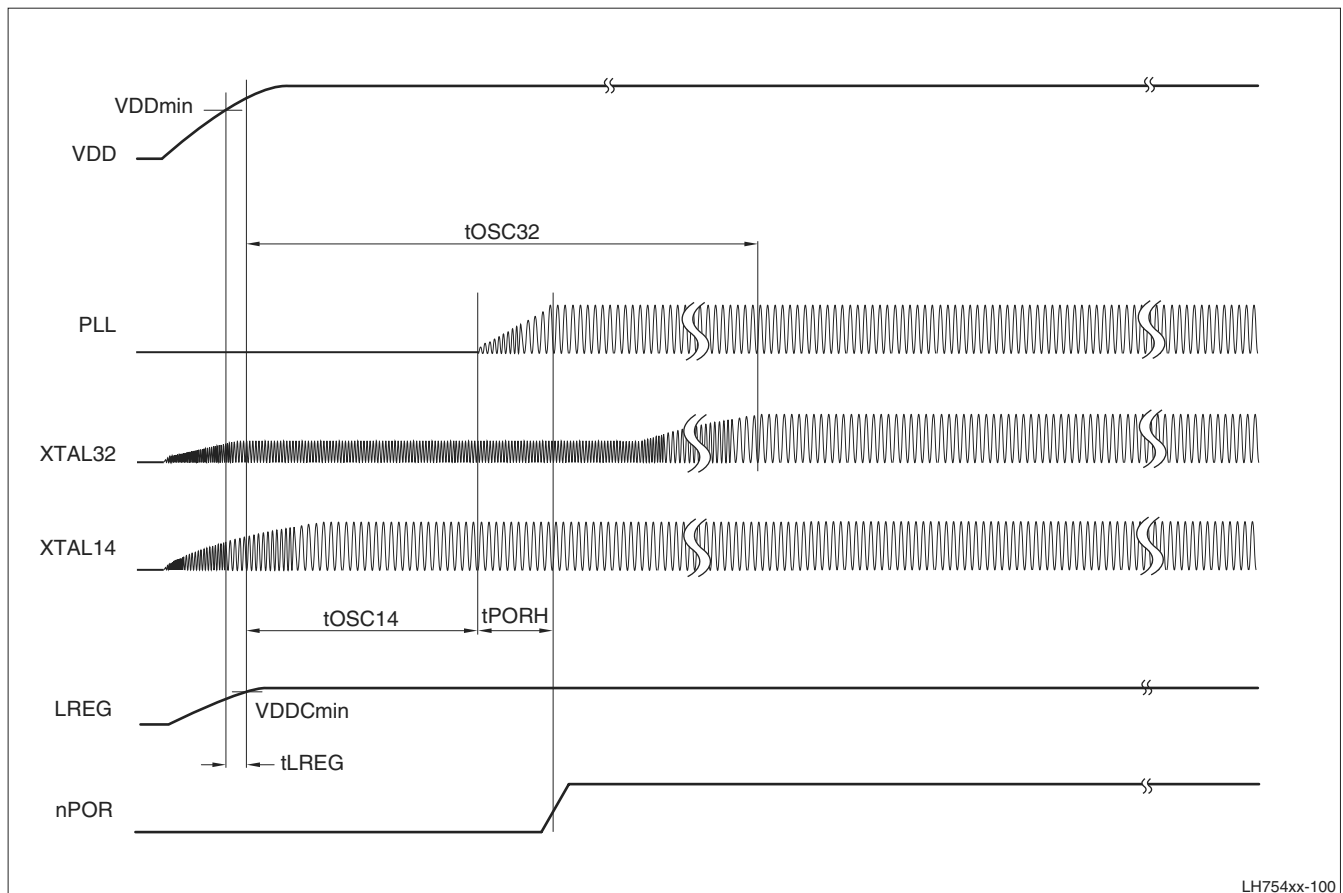


Figure 12. Power-up Stabilization

MEMORY CONTROLLER WAVEFORMS

Static Memory Controller Waveforms

Figure 13 shows the waveform and timing for an External Static Memory Write, with one Wait State. Figure 14 shows the waveform and timing for an External Static Memory Write, with two Wait States. Figure 15 shows the waveform and timing for an External Static Memory Read, with one Wait State.

The SMC supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 16. The SMC recognizes that nWAIT is active within 2 clock cycles after it has been asserted. To assure that the current access (read or write) will be extended by nWAIT, program at least two wait states for this bank of

memory. If N wait states are programmed, the SMC holds this state for N system clocks or until the SMC detects that nWAIT is inactive, whichever occurs last. As the number of wait states programmed increases, the amount of delay before nWAIT must be asserted also increases. If only 2 wait states are programmed, nWAIT must be asserted in the clock cycle immediately following the clock cycle during which the nCSx signal is asserted. Once the SMC detects that the external device has deactivated nWAIT, the SMC completes its access in 3 system clock cycles.

The formula for the allowable delay between asserting nCSx and asserting nWAIT is:

$$t_{\text{ASSERT}} = (\text{system clock period}) \times (\text{Wait States} - 1)$$

(where Wait States is from 2 to 31.)

The signal tIDD is shown without a setup time, as measurements are made from the Address Valid point and HCLK is an internal signal, shown for reference only.

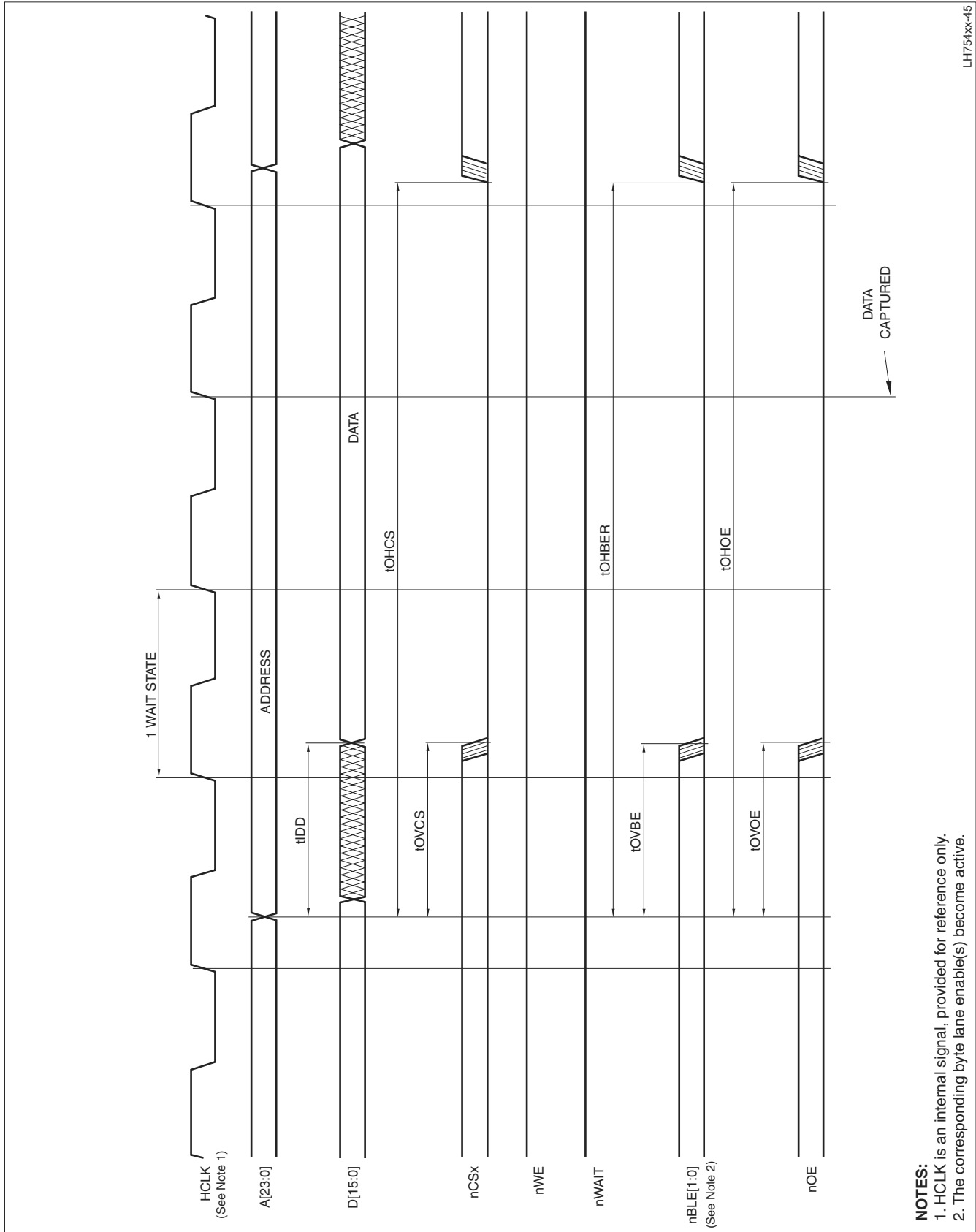


Figure 15. External Static Memory Read, One Wait State

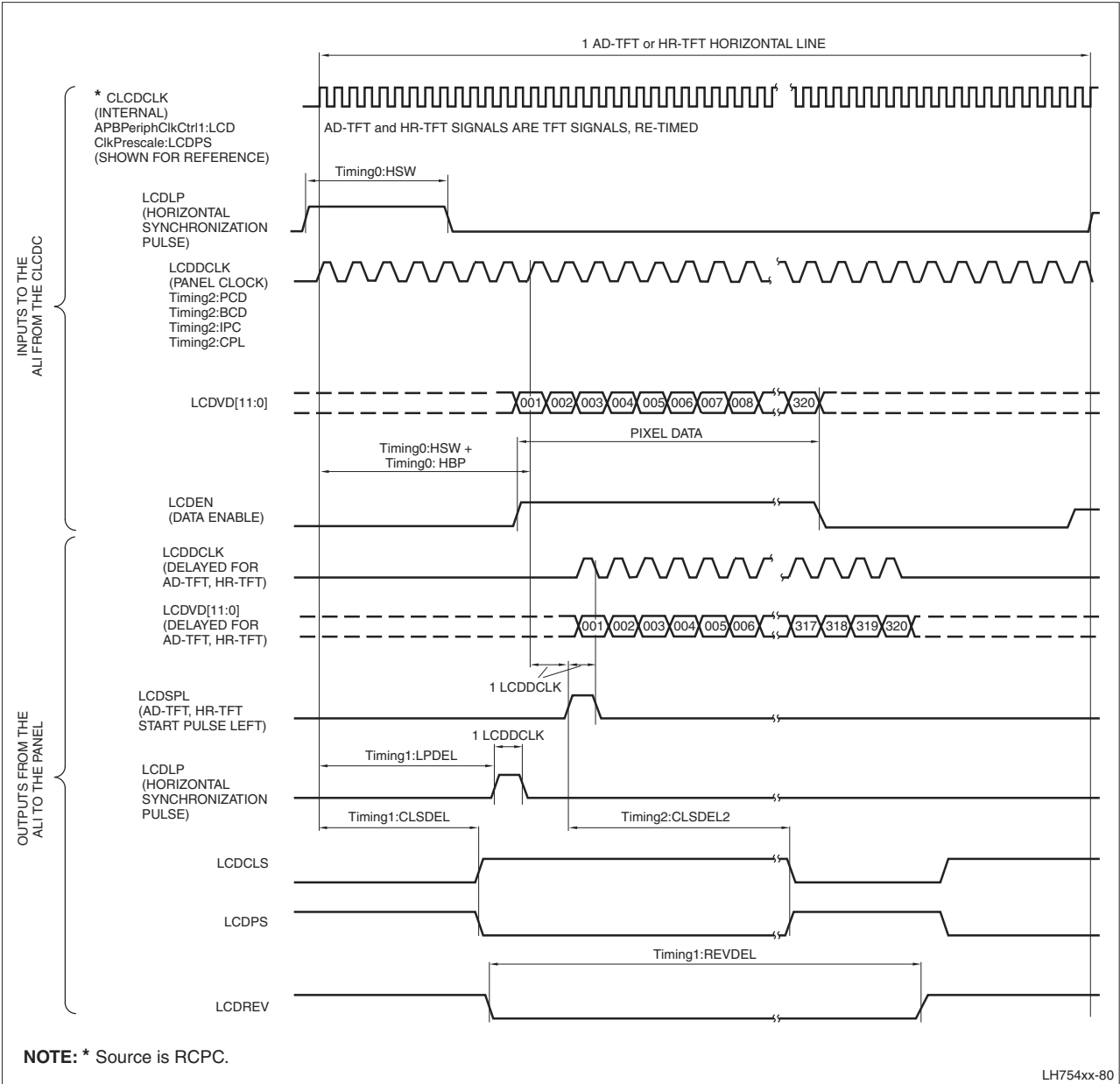


Figure 24. AD-TFT, HR-TFT Horizontal Timing Diagram

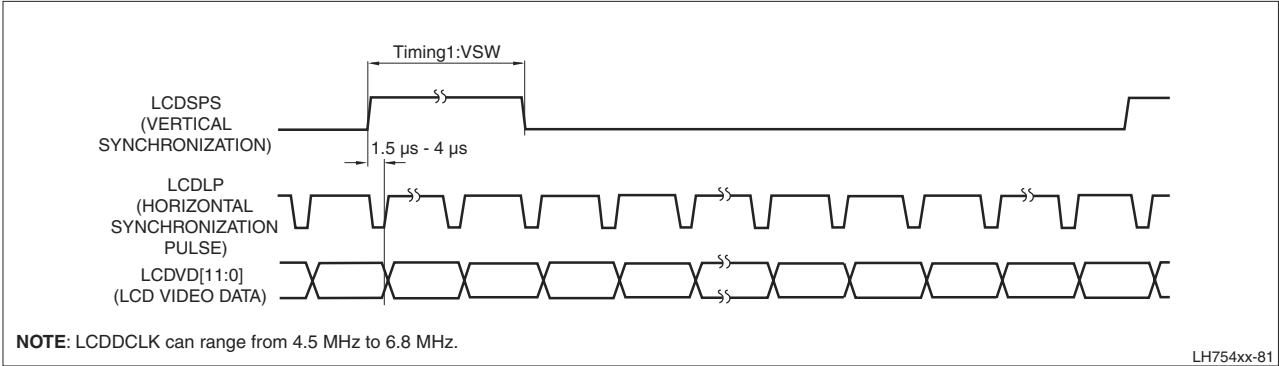


Figure 25. AD-TFT, HR-TFT Vertical Timing Diagram

PACKAGE SPECIFICATIONS

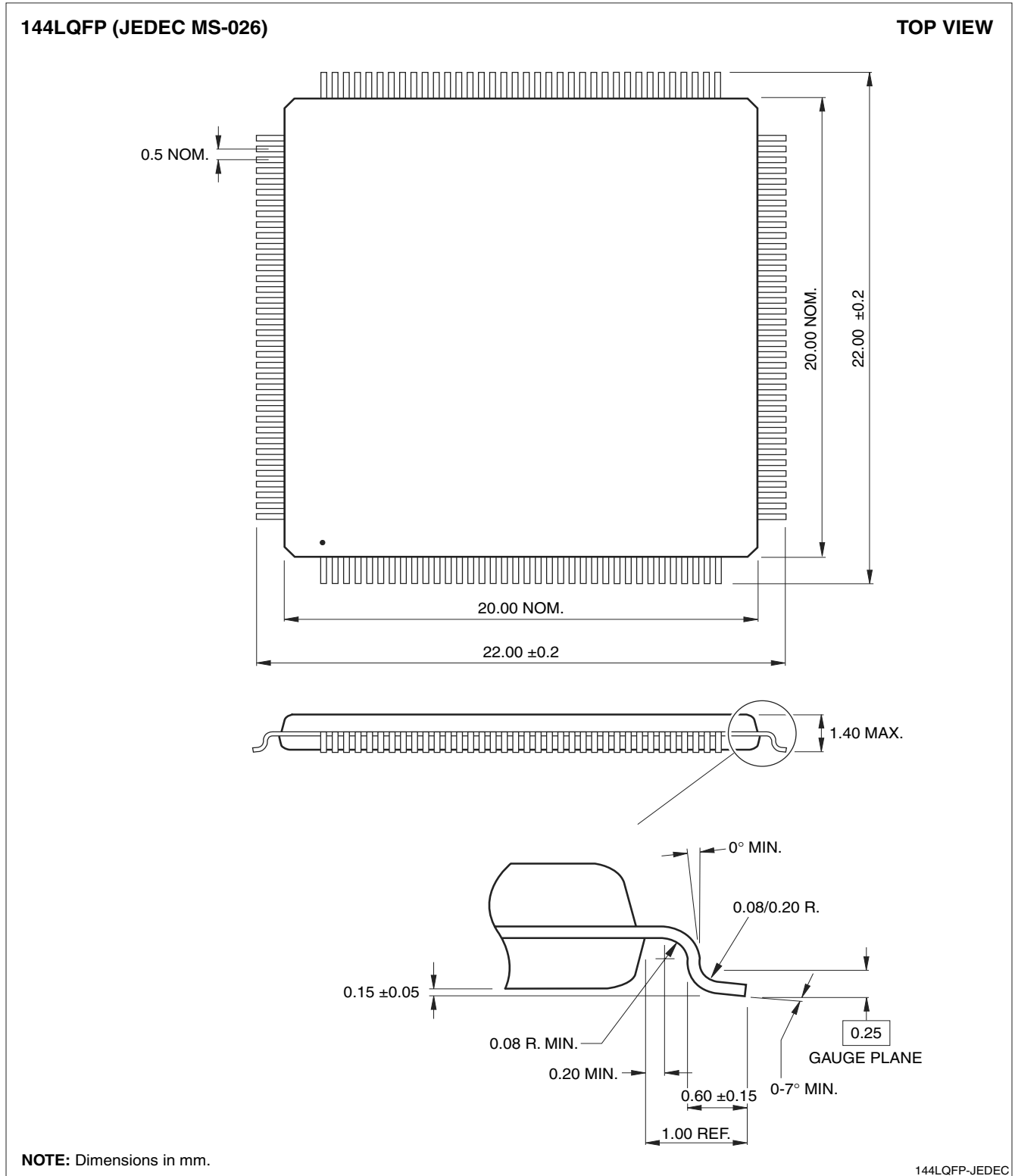


Figure 28. 144-pin LQFP