SHARP/Socle Technology - LH75410N0Q100C0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	EBI/EMI, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75410n0q100c0

LH75401 BLOCK DIAGRAM

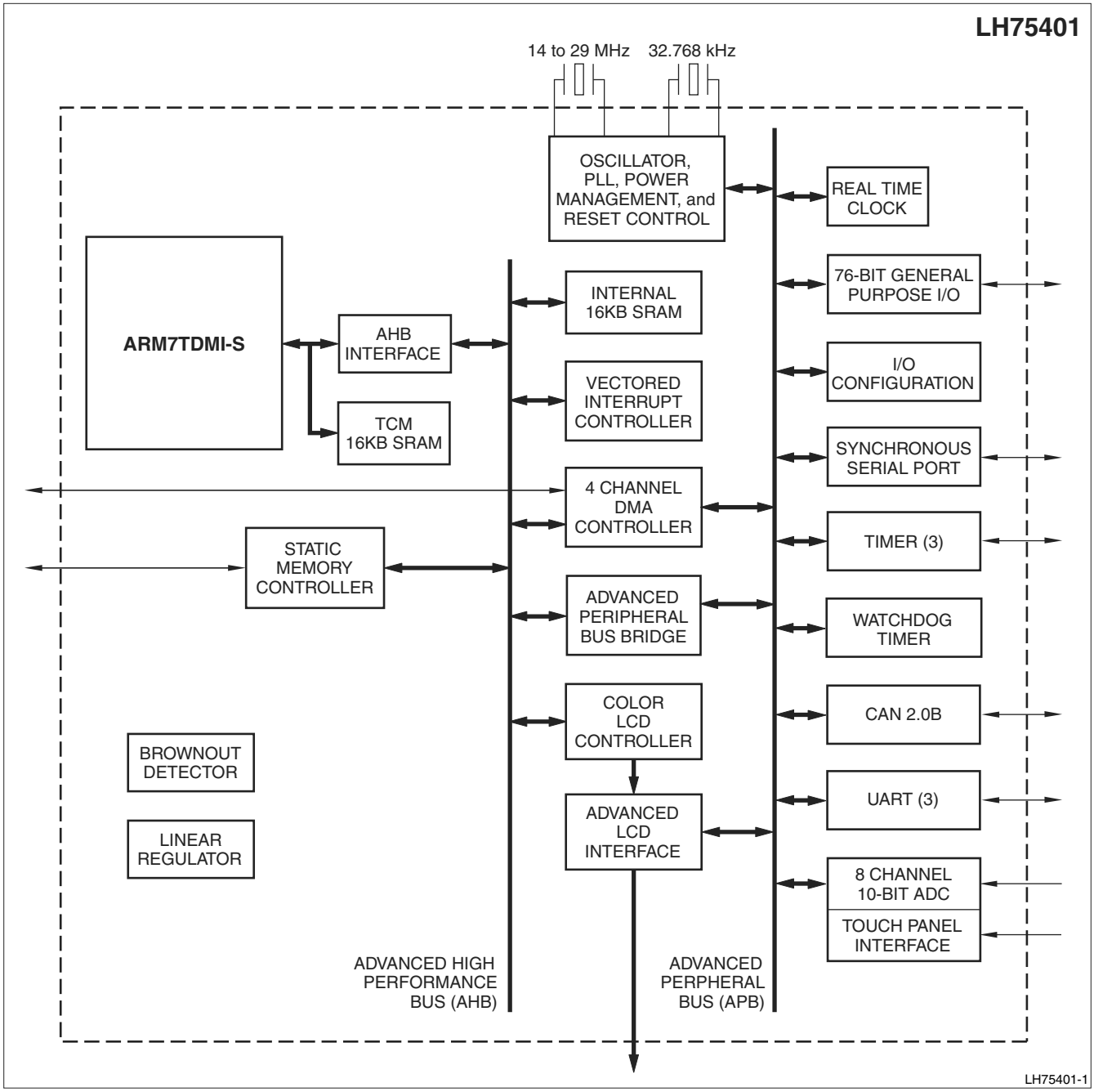


Figure 1. LH75401 Block Diagram

LH75411 BLOCK DIAGRAM

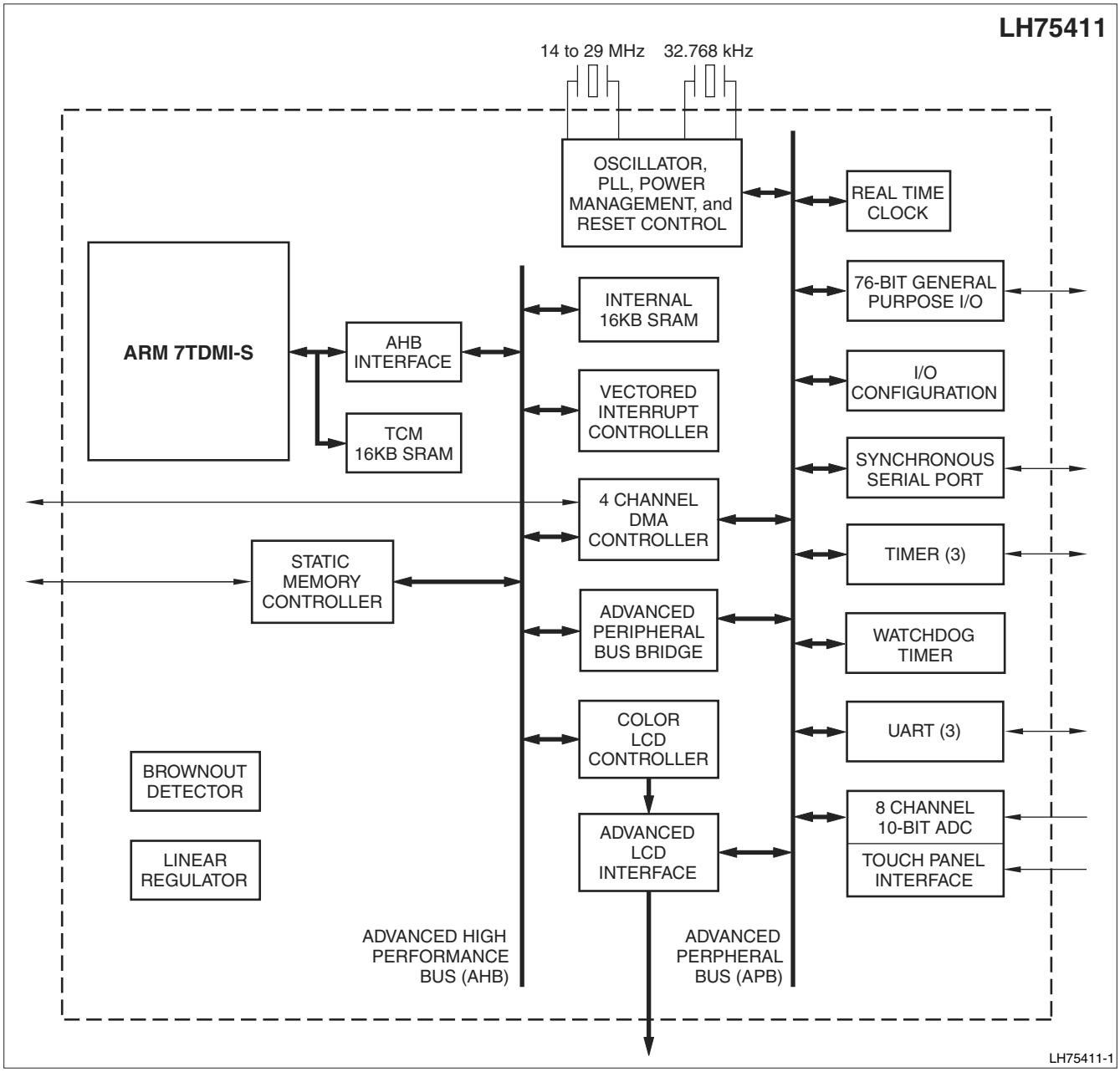


Figure 2. LH75411 Block Diagram

THE LH75401

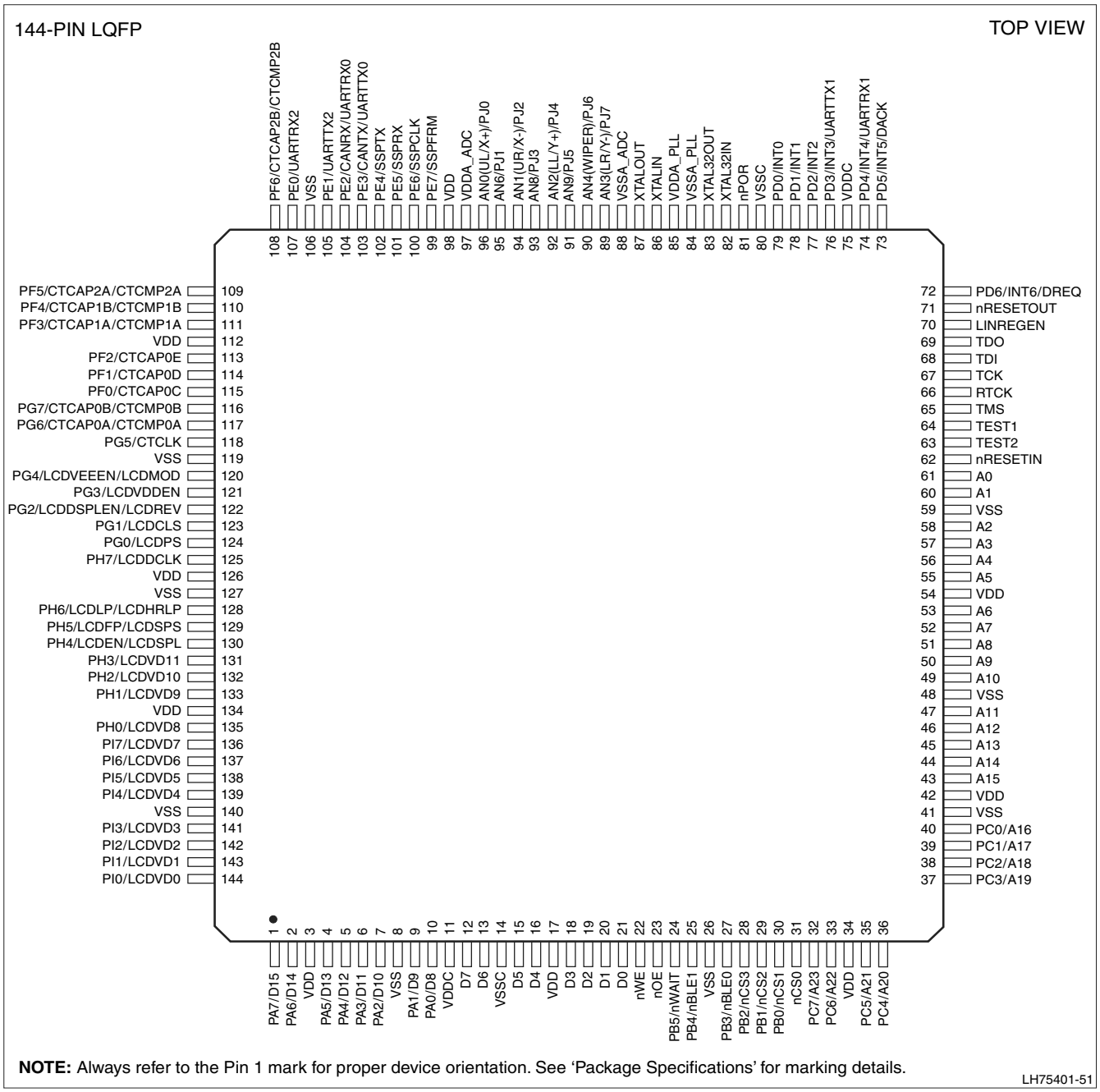


Figure 5. LH75401 Pin Diagram

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			

Table 1. LH75401 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4
83	XTAL32OUT				None	Output		
84	VSSA_PLL			Ground	None			
85	VDDA_PLL			Power	None			
86	XTALIN				None	Input		4
87	XTALOUT				None	Output		
88	VSSA_ADC			Ground	None			
89	AN3 (LR/Y-)	PJ7			None	Input		
90	AN4 (Wiper)	PJ6			None	Input		
91	AN9	PJ5			None	Input		
92	AN2 (LL/Y+)	PJ4			None	Input		
93	AN8	PJ3			None	Input		
94	AN1 (UR/X-)	PJ2			None	Input		
95	AN6	PJ1			None	Input		
96	AN0 (UL/X+)	PJ0			None	Input		
97	VDDA_ADC			Power	None			
98	VDD			Power	None			
99	PE7	SSPFRM			4 mA	Bidirectional	Pull-up	1
100	PE6	SSPCLK			4 mA	Bidirectional	Pull-down	1
101	PE5	SSPRX			4 mA	Bidirectional	Pull-up	1
102	PE4	SSPTX			4 mA	Bidirectional	Pull-down	1
103	PE3	CANTX	UARTTX0		8 mA	Bidirectional	Pull-up	1
104	PE2	CANRX	UARTRX0		2 mA	Bidirectional	Pull-up	1
105	PE1	UARTTX2			4 mA	Bidirectional	Pull-up	1
106	VSS			Ground	None			
107	PE0	UARTRX2			4 mA	Bidirectional	Pull-up	1
108	PF6	CTCAP2B	CTCMP2B		4 mA	Bidirectional		2
109	PF5	CTCAP2A	CTCMP2A		4 mA	Bidirectional		
110	PF4	CTCAP1B	CACMP1B		4 mA	Bidirectional		2
111	PF3	CTCAP1A	CTCMP1A		4 mA	Bidirectional		
112	VDD			Power	None			
113	PF2	CTCAP0E			4 mA	Bidirectional		2
114	PF1	CTCAP0D			4 mA	Bidirectional		
115	PF0	CTCAP0C			4 mA	Bidirectional		2
116	PG7	CTCAP0B	CTCMP0B		4 mA	Bidirectional		
117	PG6	CTCAP0A	CTCMP0A		4 mA	Bidirectional		2
118	PG5	CTCLK			4 mA	Bidirectional		
119	VSS			Ground	None			
120	PG4	LCDVEEEN	LCDMOD		8 mA	Bidirectional		
121	PG3	LCDVDDEN			8 mA	Bidirectional		
122	PG2	LCDDSPLEN	LCDREV		8 mA	Bidirectional		

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

LH75411 Numerical Pin Listing

Table 3. LH75411 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1
41	VSS			Ground	None			

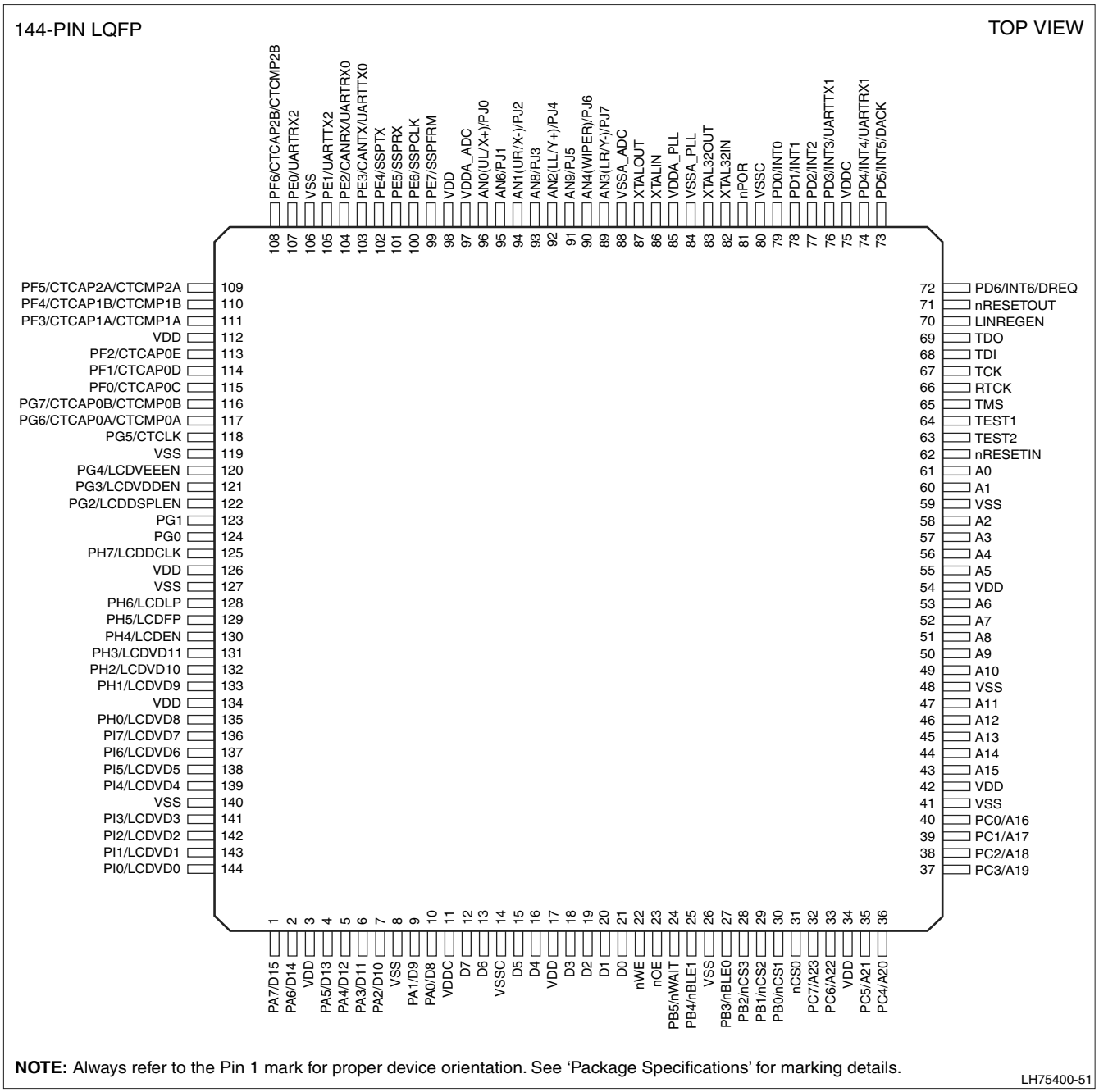
Table 3. LH75411 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
42	VDD			Power	None			
43	A15				8 mA	Output	LOW	
44	A14				8 mA	Output	LOW	
45	A13				8 mA	Output	LOW	
46	A12				8 mA	Output	LOW	
47	A11				8 mA	Output	LOW	
48	VSS			Ground	None			
49	A10				8 mA	Output	LOW	
50	A9				8 mA	Output	LOW	
51	A8				8 mA	Output	LOW	
52	A7				8 mA	Output	LOW	
53	A6				8 mA	Output	LOW	
54	VDD			Power	None			
55	A5				8 mA	Output	LOW	
56	A4				8 mA	Output	LOW	
57	A3				8 mA	Output	LOW	
58	A2				8 mA	Output	LOW	
59	VSS			Ground	None			
60	A1				8 mA	Output	LOW	
61	A0				8 mA	Output	LOW	
62	nRESETIN				None	Input	Pull-up	2, 3
63	TEST2				None	Input	Pull-up	2
64	TEST1				None	Input	Pull-up	2
65	TMS				None	Input	Pull-up	2
66	RTCK				4 mA	Output		
67	TCK				None	Input		
68	TDI				None	Input	Pull-up	2
69	TDO				4 mA	Output		
70	LINREGEN				None	Input		5
71	nRESETOUT				8 mA	Output		3
72	PD6	INT6	DREQ		6 mA	Bidirectional	Pull-down	1
73	PD5	INT5	DACK		6 mA	Bidirectional		1, 2
74	PD4	INT4	UARTRX1		8 mA	Bidirectional	Pull-up	1
75	VDDC			Power	None			
76	PD3	INT3	UARTTX1		8 mA	Bidirectional	Pull-up	1
77	PD2	INT2			2 mA	Bidirectional	Pull-up	1
78	PD1	INT1			6 mA	Bidirectional		1, 2
79	PD0	INT0			2 mA	Bidirectional		1
80	VSSC			Ground	None			
81	nPOR				None	Input	Pull-up	2, 3
82	XTAL32IN				None	Output		4
83	XTAL32OUT				None	Output		

Table 4. LH75411 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
89 90 91 92 93 94 95 96	PJ7 PJ6 PJ5 PJ4 PJ3 PJ2 PJ1 PJ0	Input	General Purpose I/O Signals - Port J	1
99 100 101 102 103 104 105 107	PE7 PE6 PE5 PE4 PE3 PE2 PE1 PE0	Input/Output	General Purpose I/O Signals - Port E	1
108 109 110 111 113 114 115	PF6 PF5 PF4 PF3 PF2 PF1 PF0	Input/Output	General Purpose I/O Signals - Port F	1
116 117 118 120 121 122 123 124	PG7 PG6 PG5 PG4 PG3 PG2 PG1 PG0	Input/Output	General Purpose I/O Signals - Port G	1
125 128 129 130 131 132 133 135	PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0	Input/Output	General Purpose I/O Signals - Port H	1
136 137 138 139 141 142 143 144	PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0	Input/Output	General Purpose I/O Signals - Port I	1
RESET, CLOCK, AND POWER CONTROLLER (RCPC)				
62	nRESETIN	Input	User Reset Input	2
71	nRESETOUT	Output	System Reset Output	2
72	INT6	Input	External Interrupt Input 6	1
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1

THE LH75400



NOTE: Always refer to the Pin 1 mark for proper device orientation. See 'Package Specifications' for marking details.

LH75400-51

Figure 7. LH75400 Pin Diagram

LH75400 Numerical Pin Listing

Table 5. LH75400 Numerical Pin List

PIN NO.	FUNCTION AT RESET	FUNCTION 2	FUNCTION 3	FUNCTION TYPE	OUTPUT DRIVE	BUFFER TYPE	BEHAVIOR DURING RESET	NOTES
1	PA7	D15		I/O	8 mA	Bidirectional	Pull-up	1
2	PA6	D14		I/O	8 mA	Bidirectional	Pull-up	1
3	VDD			Power	None			
4	PA5	D13		I/O	8 mA	Bidirectional	Pull-up	1
5	PA4	D12		I/O	8 mA	Bidirectional	Pull-up	1
6	PA3	D11		I/O	8 mA	Bidirectional	Pull-up	1
7	PA2	D10		I/O	8 mA	Bidirectional	Pull-up	1
8	VSS			Ground	None			
9	PA1	D9		I/O	8 mA	Bidirectional	Pull-up	1
10	PA0	D8		I/O	8 mA	Bidirectional	Pull-up	1
11	VDDC			Power	None			
12	D7			I/O	8 mA	Bidirectional	Pull-up	
13	D6			I/O	8 mA	Bidirectional	Pull-up	
14	VSSC			Ground	None			
15	D5			I/O	8 mA	Bidirectional	Pull-up	
16	D4			I/O	8 mA	Bidirectional	Pull-up	
17	VDD			Power	None			
18	D3			I/O	8 mA	Bidirectional	Pull-up	
19	D2			I/O	8 mA	Bidirectional	Pull-up	
20	D1			I/O	8 mA	Bidirectional	Pull-up	
21	D0			I/O	8 mA	Bidirectional	Pull-up	
22	nWE				8 mA	Output	HIGH	3
23	nOE				8 mA	Output	HIGH	3
24	PB5	nWAIT			8 mA	Bidirectional	Pull-up	1, 3
25	PB4	nBLE1			8 mA	Bidirectional	Pull-up	1, 3
26	VSS			Ground	None			
27	PB3	nBLE0			8 mA	Bidirectional	Pull-up	1, 3
28	PB2	nCS3			8 mA	Bidirectional	Pull-up	1, 3
29	PB1	nCS2			8 mA	Bidirectional	Pull-up	1, 3
30	PB0	nCS1			8 mA	Bidirectional	Pull-up	1, 3
31	nCS0				8 mA	Output	Pull-up	3
32	PC7	A23			8 mA	Bidirectional	Pull-down	1
33	PC6	A22			8 mA	Bidirectional	Pull-down	1
34	VDD			Power	None			
35	PC5	A21			8 mA	Bidirectional	Pull-down	1
36	PC4	A20			8 mA	Bidirectional	Pull-down	1
37	PC3	A19			8 mA	Bidirectional	Pull-down	1
38	PC2	A18			8 mA	Bidirectional	Pull-down	1
39	PC1	A17			8 mA	Bidirectional	Pull-down	1
40	PC0	A16			8 mA	Bidirectional	Pull-down	1

THE LH75410

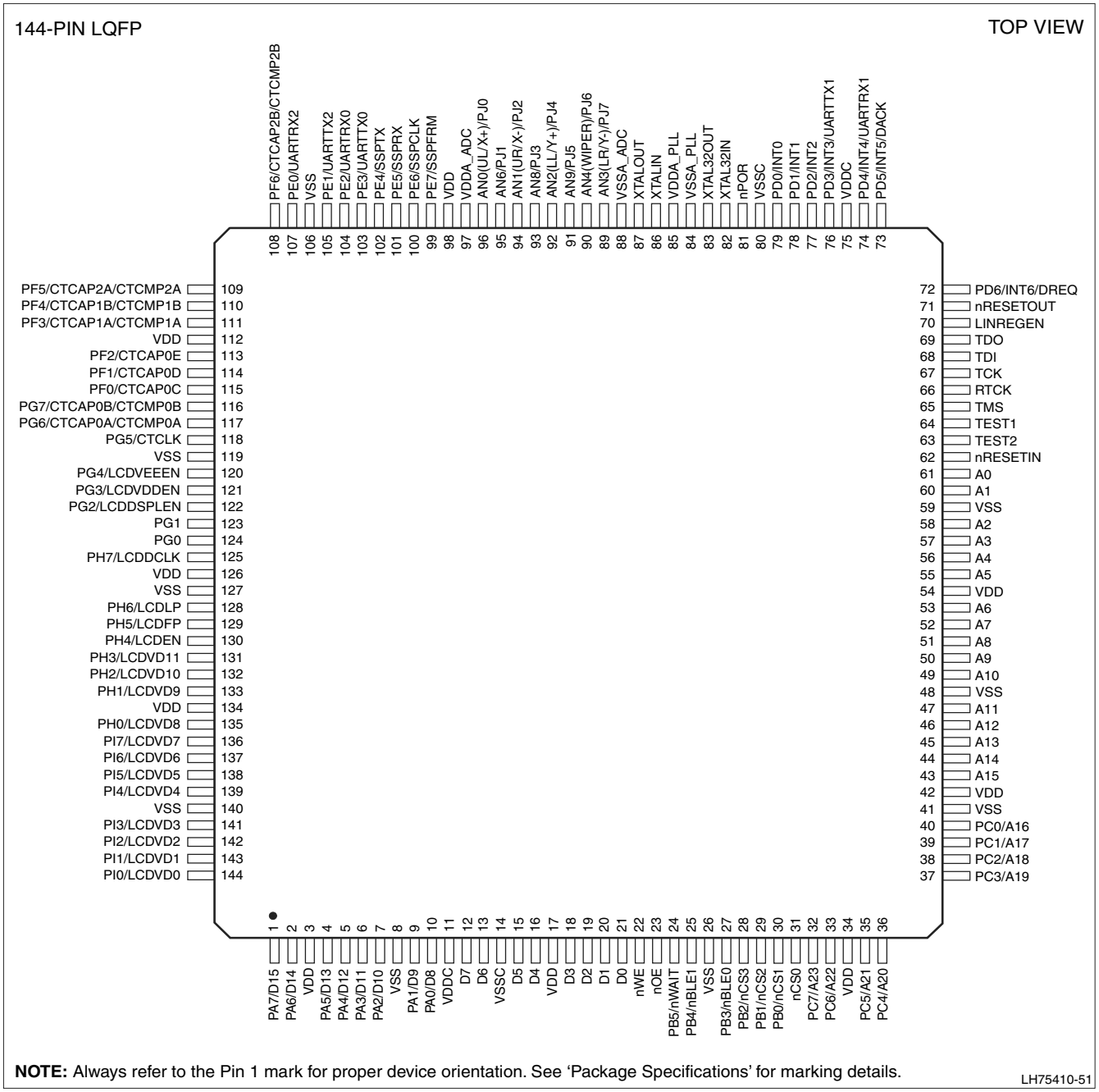


Figure 8. LH75410 Pin Diagram

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
LCD CONTROLLER (LCDC)				
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
130	LCDEN	Output	LCD Data Enable	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1

Table 13. SSP Modes

MODE	DESCRIPTION	DATA TRANSFERS
Motorola SPI	For communications with Motorola SPI-compatible devices. Clock polarity and phase are programmable.	Full-duplex, 4-wire synchronous
SSI	For communications with Texas Instruments DSP-compatible Serial Synchronous Interface devices.	Full-duplex, 4-wire synchronous
National Semiconductor Microwire	For communications with National Semiconductor Microwire-compatible devices.	Half-duplex synchronous, using 8-bit control messages

Watchdog Timer (WDT)

The WDT consists of a 32-bit down-counter that allows a selectable time-out interval to detect malfunctions. The timer must be reset by software periodically. Otherwise, a time-out occurs, interrupting the system. If the interrupt is not serviced within the timeout period, the WDT triggers the RCPC to generate a System Reset. If the WDT times out, it sets a bit in the RCPC Reset Status Register.

The WDT supports 16 selectable time intervals, for a time-out of 216 through 231 system clock cycles. All Control and Status Registers for the Watchdog Timer are accessed through the APB.

WDT FEATURES

- Counter generates an interrupt at a set interval and the count reloads from the pre-set value after reaching zero.
- Default timeout period is set to the minimum timeout of 216 system clock cycles.
- WDT is driven by the APB.
- Built-in protection mechanism guards against interrupt-service failure.
- WDT can be programmed to trigger a System Reset on a timeout.
- WDT can be programmed to trigger an interrupt on the first timeout; then, if the service routine fails to clear the interrupt, the next WDT timeout triggers a System Reset.

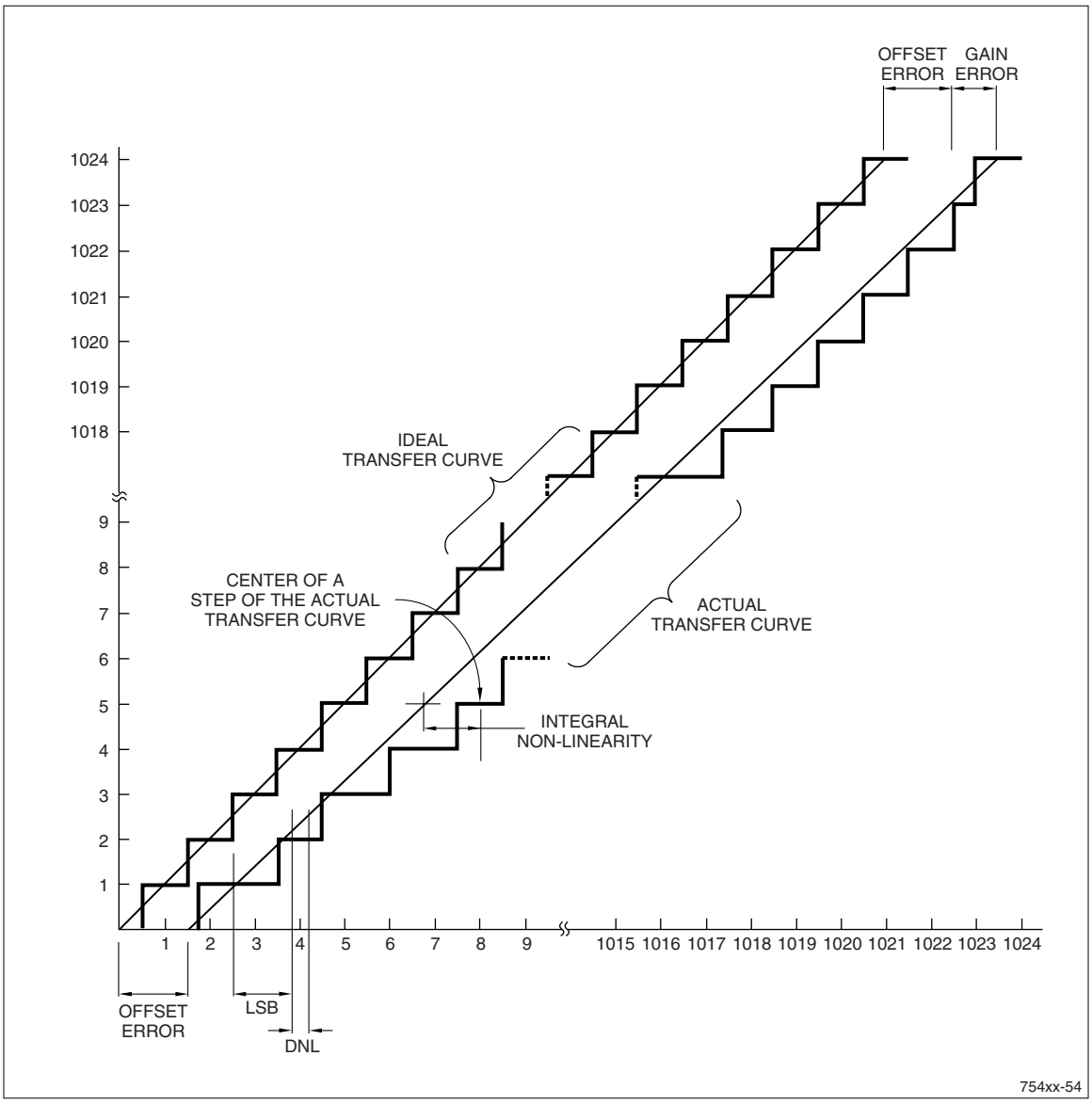


Figure 11. ADC Transfer Characteristics

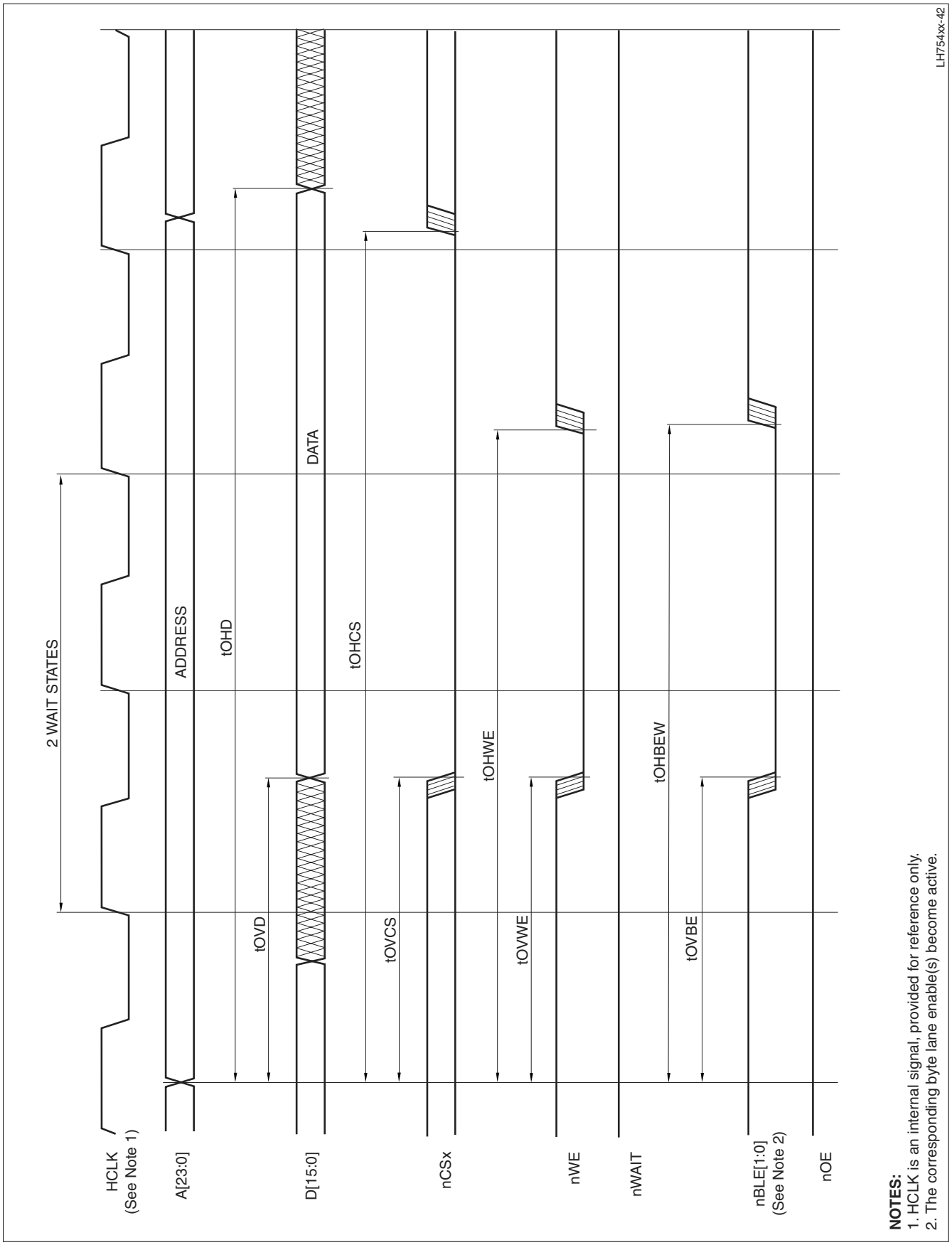


Figure 14. External Static Memory Write, Two Wait States

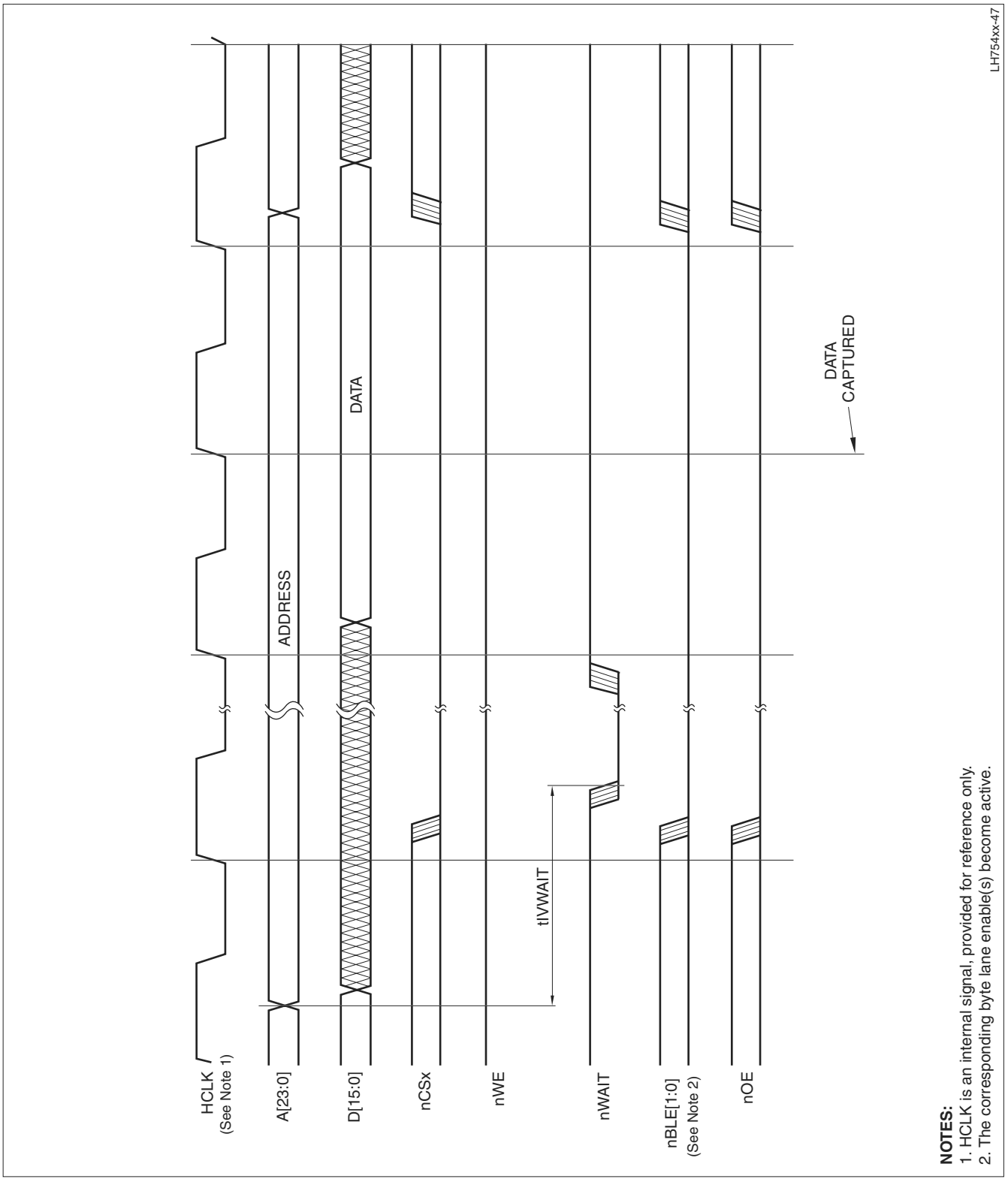
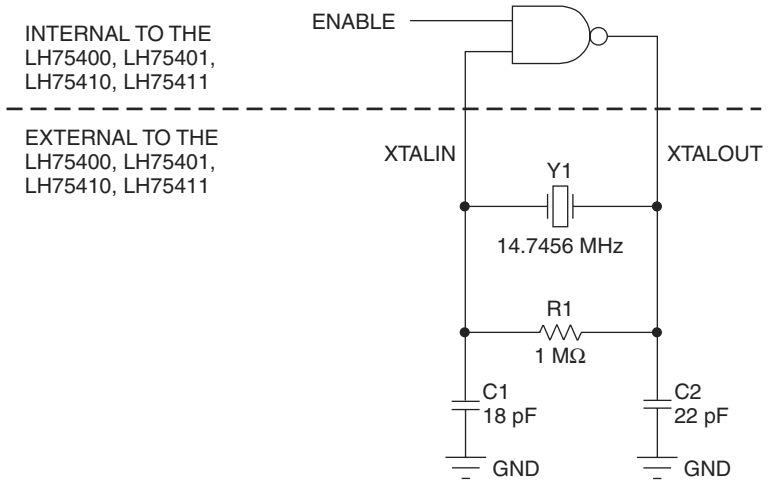


Figure 16. External Static Memory Read, nWAIT Active



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

LH754xx-102

Figure 27. Suggested External Components, 14.7456 MHz Oscillator

CONTENT REVISIONS

This document contains the following changes to content, causing it to differ from previous versions.

Table 31. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
5-14-04	—		'Preliminary' Status removed.
	1	—	Core Speed Specification and Crystal Specifications updated.
	1	Page Note	Tolerance of XTAL inputs noted.
	8 - 10, 18 - 20, 28 - 30,	Tables 1, 3, 5, 7	Column heading for Reset behavior clarified; memory interface lines behavior during Reset clarified; notes added regarding voltage tolerance of XTAL inputs, need for 10 kΩ pull-up resistor to activate the on-chip linear regulator; SSPFRM and SSPCLK signals type corrected to Output.
	12, 22, 49	AD-TFT, HR-TFT Interface description	Corrected to Advanced LCD Interface description, text updated for clarity.
	46	Clock Sources	Rewritten to reflect updated specifications
	58	Table 22	DC Characteristics of XTAL inputs added.
		Table 23	Pull-up resistor for Linear Regulator specified.
	61	Table 27	Start-up Characteristics Table expanded.
	62	Current Consumption	Current Consumption by Operating Mode added.
	64	Figure 11	Start-up Characteristics Figure expanded.
	69, 70	Figures 18, 19	Suggested External Components added.
	73	Figure 21	Recommended PCB Footprint added.
05-20-05	—	—	Version number rolled to 1.1.
	10, 20, 30, 40, 59	Table Notes Table Notes Table 24	Pull-up resistor value for Linear Regulator updated.
	51	SSP Features	Text regarding interrupt-driven transfers clarified.
	72	Figure 20	Specification Drawing updated to add clearance under chip.
03-30-06	—	—	Version number rolled to 1.2.
	1	Features	Top Speed adjusted to reflect MAX. Temp and MIN. Voltage
	1	Pin Drawings	Note added to refer to device Pin 1 marking for proper orientation.
	57	Table 21	Footnote added regarding power sequencing.
			MAX specification for Crystal Frequency changed to 20 MHz; Note 3 clarified.
	58	Very Low Temperatures and Noise Immunity	Text regarding operating the device at very low temperatures with an external clock. added.
	62	Power Supply Sequencing	Specifications for power supply sequencing added.
	62	Linear Regulator	Note about using the Linear Regulator to power external devices added.
	63	Table 28	Clarified tIDD for more than one WAIT state, added MAX. value for tOHWE.
	67,68	Figures 15,16	Added data latch point for Memory Read cycles.
	70 – 72	Figures 18 – 19	Moved DMA timing waveforms into the Data Sheet for ease of maintenance and to keep all interface diagrams together in one place.
	70 – 76	Figures 20 – 25	Moved LCD timing waveforms into the Data Sheet for ease of maintenance and to keep all interface diagrams together in one place.