SHARP/Socle Technology - LH75411N0M100C0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	EBI/EMI, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh75411n0m100c0

LH75401 BLOCK DIAGRAM

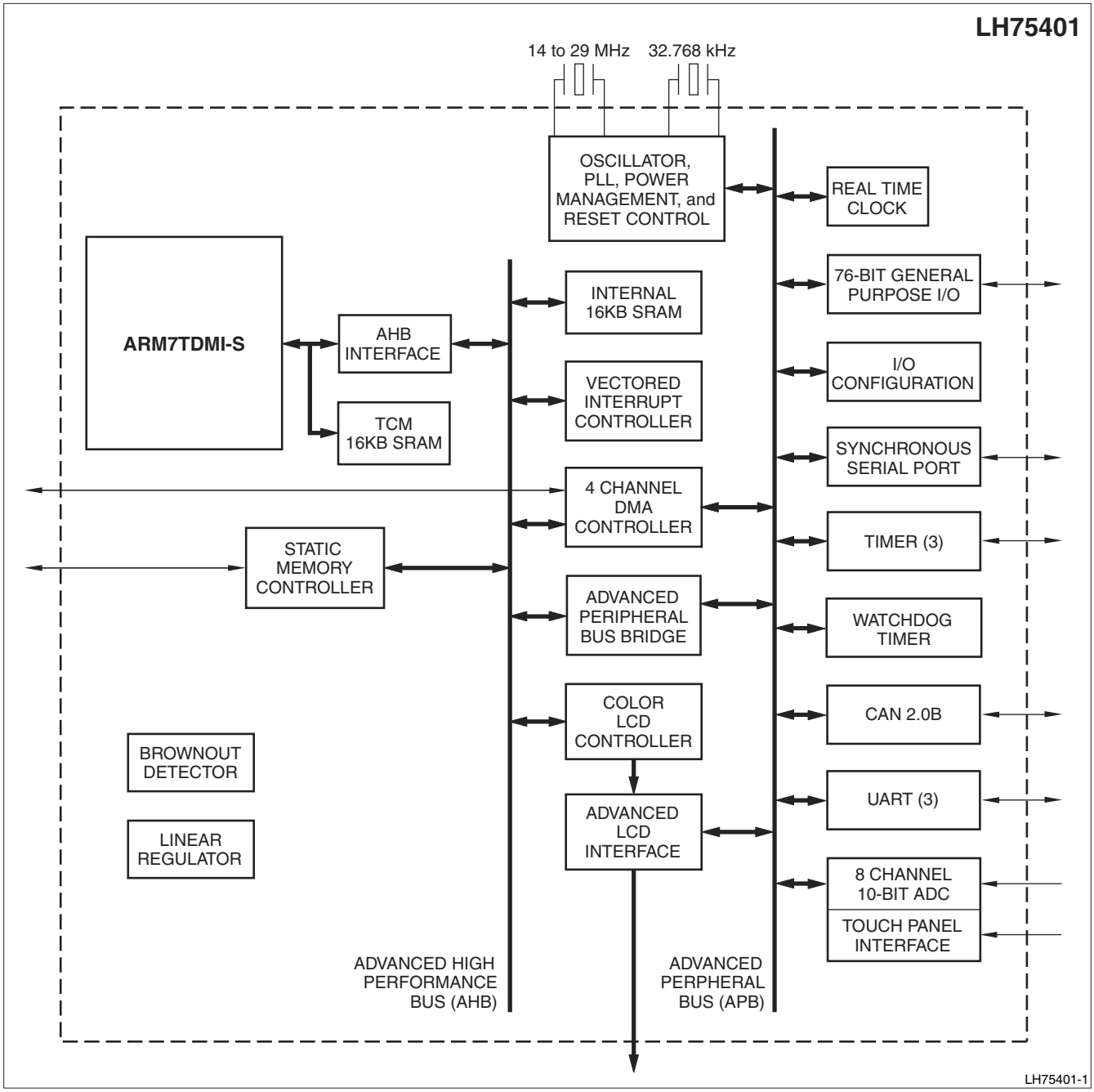


Figure 1. LH75401 Block Diagram

LH75400 BLOCK DIAGRAM

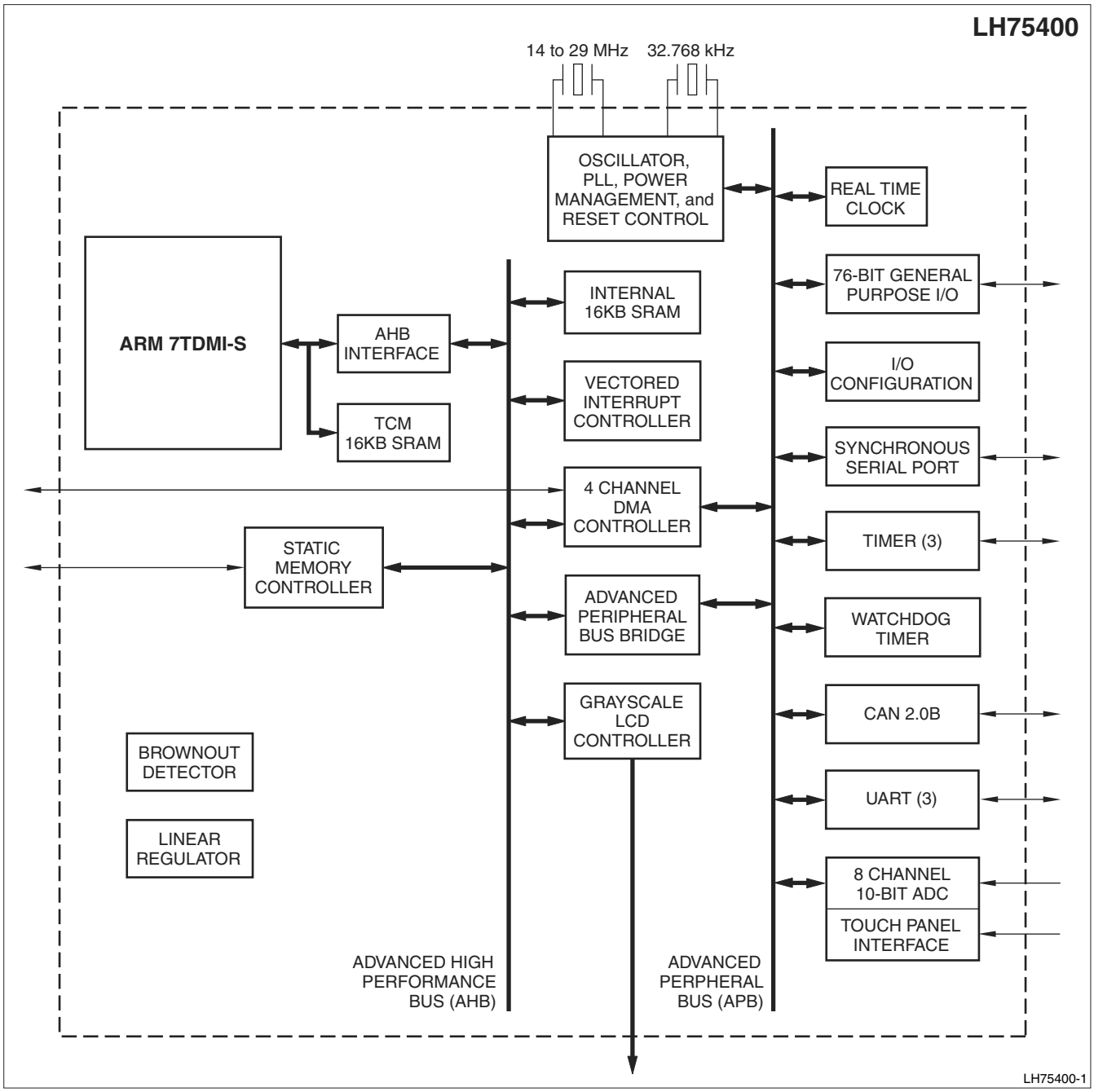


Figure 3. LH75400 Block Diagram

THE LH75401

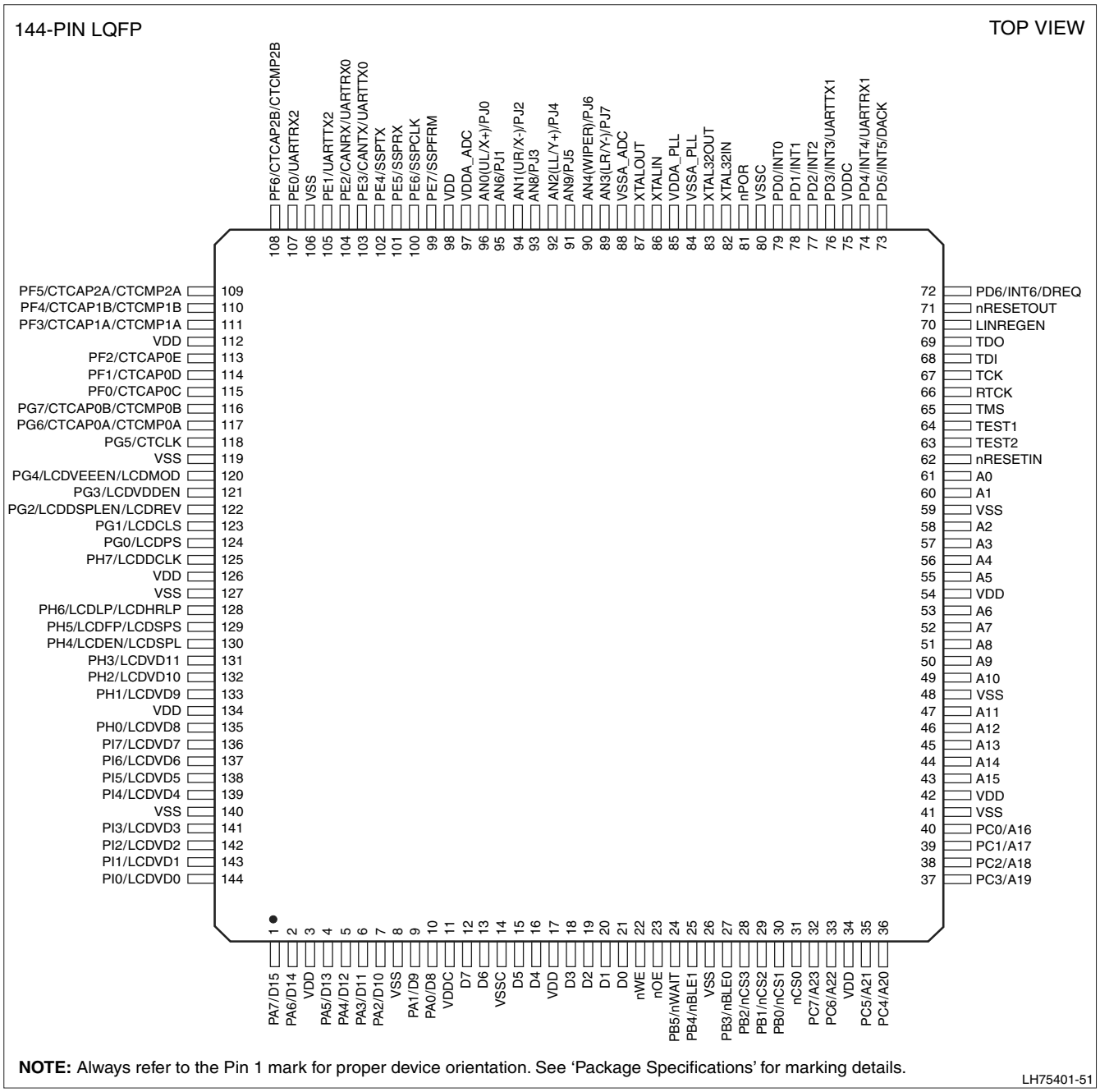


Figure 5. LH75401 Pin Diagram

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
COLOR LCD CONTROLLER (CLCDC)				
120	LCDMOD	Output	Signal Used by the Row Driver (AD-TFT, HR-TFT only)	1
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
122	LCDREV	Output	Reverse Signal (AD-TFT, HR-TFT only)	1
123	LCDCLS	Output	Clock to the Row Drivers (AD-TFT, HR-TFT only)	1
124	LCDPS	Output	Power Save (AD-TFT, HR-TFT only)	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
128	LCDHRLP	Output	Latch Pulse (AD-TFT, HR-TFT only)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
129	LCDSPS	Output	Row Driver Counter Reset Signal (AD-TFT, HR-TFT only)	1
130	LCDEN	Output	LCD Data Enable	1
130	LCDSPL	Output	Start Pulse Left (AD-TFT, HR-TFT only)	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
CONTROLLER AREA NETWORK (CAN)				
103	CANTX	Output	CAN Transmitted Serial Data Output	1
104	CANRX	Input	CAN Received Serial Data Input	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 1				
111 110	CTCAP1[A:B]	Input	Timer 1 Capture Inputs	1
111 110	CTCMP1[A:B]	Output	Timer 1 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
TIMER 2				
109 108	CTCAP2[A:B]	Input	Timer 2 Capture Inputs	1
109 108	CTCMP2[A:B]	Input	Timer 2 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1
GENERAL PURPOSE INPUT/OUTPUT (GPIO)				
1 2 4 5 6 7 9 10	PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	Input/Output	General Purpose I/O Signals - Port A	1
24 25 27 28 29 30	PB5 PB4 PB3 PB2 PB1 PB0	Input/Output	General Purpose I/O Signals - Port B	1
32 33 35 36 37 38 39 40	PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0	Input/Output	General Purpose I/O Signals - Port C	1

Table 2. LH75401 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
73	INT5	Input	External Interrupt Input 5	1
74	INT4	Input	External Interrupt Input 4	1
76	INT3	Input	External Interrupt Input 3	1
77	INT2	Input	External Interrupt Input 2	1
78	INT1	Input	External Interrupt Input 1	1
79	INT0	Input	External Interrupt Input 0	1
81	nPOR	Input	Power-on Reset Input	2
82	XTAL32IN	Input	32.768 kHz Crystal Clock Input	
83	XTAL32OUT	Output	32.768 kHz Crystal Clock Output	
86	XTALIN	Input	Crystal Clock Input	
87	XTALOUT	Output	Crystal Clock Output	
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pin numbers have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

LH75411 Signal Descriptions

Table 4. LH75411 Signal Descriptions

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
MEMORY INTERFACE (MI)				
1 2 4 5 6 7 9 10 12 13 15 16 18 19 20 21	D[15:0]	Input/Output	Data Input/Output Signals	1
22	nWE	Output	Static Memory Controller Write Enable	2
23	nOE	Output	Static Memory Controller Output Enable	2
24	nWAIT	Input	Static Memory Controller External Wait Control	1, 2
25	nBLE1	Output	Static Memory Controller Byte Lane Strobe	1, 2
27	nBLE0	Output	Static Memory Controller Byte Lane Strobe	1, 2
28	nCS3	Output	Static Memory Controller Chip Select	1, 2
29	nCS2	Output	Static Memory Controller Chip Select	1, 2
30	nCS1	Output	Static Memory Controller Chip Select	1, 2
31	nCS0	Output	Static Memory Controller Chip Select	2
32 33 35 36 37 38 39 40 43 44 45 46 47 49 50 51 52 53 55 56 57 58 60 61	A[23:0]	Output	Address Signals	1
DMA CONTROLLER (DMAC)				
72	DREQ	Input	DMA Request	1
73	DACK	Output	DMA Acknowledge	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
LCD CONTROLLER (LCDC)				
120	LCDVEEEN	Output	Analog Supply Enable (AC Bias SIgnal)	1
121	LCDVDDEN	Output	Digital Supply Enable	1
122	LCDDSPLEN	Output	LCD Panel Power Enable	1
125	LCDDCLK	Output	LCD Panel Clock	1
128	LCDLP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)	1
129	LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)	1
130	LCDEN	Output	LCD Data Enable	1
131 132 133 135 136 137 138 139 141 142 143 144	LCDVD[11:0]	Output	LCD Panel Data bus	1
SYNCHRONOUS SERIAL PORT (SSP)				
99	SSPFRM	Output	SSP Serial Frame	1
100	SSPCLK	Output	SSP Clock	1
101	SSPRX	Input	SSP RXD	1
102	SSPTX	Output	SSP TXD	1
UART0 (U0)				
103	UARTTX0	Output	UART0 Transmitted Serial Data Output	1
104	UARTRX0	Input	UART0 Received Serial Data Input	1
UART1 (U1)				
74	UARTRX1	Input	UART1 Received Serial Data Input	1
76	UARTTX1	Output	UART1 Transmitted Serial Data Output	1
UART2 (U2)				
105	UARTTX2	Output	UART2 Transmitted Serial Data Output	1
107	UARTRX2	Input	UART2 Received Serial Data Input	1
ANALOG-TO-DIGITAL CONVERTER (ADC)				
89 90 91 92 93 94 95 96	AN3 (LR/Y-) AN4 (Wiper) AN9 AN2 (LL/Y+) AN8 AN1 (UR/X-) AN6 AN0 (UL/X+)	Input	ADC Inputs	1
TIMER 0				
117 116 115 114 113	CTCAP0[A:E]	Input	Timer 0 Capture Inputs	1
117 116	CTCMP0[A:B]	Output	Timer 0 Compare Outputs	1
118	CTCLK	Input	Common External Clock	1

Table 8. LH75410 Signal Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION	NOTES
TEST INTERFACE				
63	TEST2	Input	Test Mode Pin 2	
64	TEST1	Input	Test Mode Pin 1	
65	TMS	Input	JTAG Test Mode Select Input	
66	RTCK	Output	Returned JTAG Test Clock Output	
67	TCK	Input	JTAG Test Clock Input	
68	TDI	Input	JTAG Test Serial Data Input	
69	TDO	Output	JTAG Test Data Serial Output	
POWER AND GROUND (GND)				
3 17 34 42 54 98 112 126 134	VDD	Power	I/O Ring VDD	
8 26 41 48 59 106 119 127 140	VSS	Power	I/O Ring VSS	
11 75	VDDC	Power	Core VDD supply (Output if Linear Regulator Enabled, Otherwise Input)	
14 80	VSSC	Power	Core VSS	
70	LINREGEN	Input	Linear Regulator Enable	
84	VSSA_PLL	Power	PLL Analog VSS	
85	VDDA_PLL	Power	PLL Analog VDD Supply	
88	VSSA_ADC	Power	A-to-D converter Analog VSS	
97	VDDA_ADC	Power	A-to-D converter Analog VDD Supply	

NOTES:
1. These pins have multiplexed functions.
2. Signals preceded with 'n' are active LOW.

Color LCD Controller (CLCDC)

The CLCDC is an AMBA master-slave module that connects to the AHB. It translates pixel-coded data into the required formats and timings to drive single/dual monochrome and color LCD panels. Packets of pixel-coded data are fed, via the AHB interface, to two independently programmable, 32-bit-wide DMA FIFOs. Each FIFO is 16 words deep by 32 bits wide.

The CLCDC generates a single combined interrupt to the Vectored Interrupt Controller (VIC) when an interrupt condition becomes true for upper/lower panel DMA FIFO underflow, base address update signification, vertical compare, or bus error.

NOTE: LH75401 and LH75411 microcontrollers support full-colo operation. LH75400 and LH75410 microcontrollers are monochrome only.

CLCDC FEATURES

- STN, Color STN, TFT, HR-TFT, and AD-TFT
  - Fully Programmable Timing Controls
  - Advanced LCD Interface for displays with a low level of integration, such as HR-TFT and AD-TFT
- Programmable Resolution
  - Up to VGA (640 × 480 DPI), 12-bit Direct Mode Color
  - Up to SVGA (800 × 600 DPI), 8-bit Direct/Paletized Color
  - Up to XGA (1,024 × 768 DPI), 4-bit Direct Color/ Grayscale
  - Direct or Paletized Colors
- Single and Dual Panels
- Supports Sharp and non-Sharp Panels
- CLCDC Outputs Available as General Purpose Inputs/Outputs (GPIOs) if LCDC is Not Needed
- Additional Features
  - Fully programmable horizontal and vertical timing for different display panels
  - 256-entry, 16-bit palette RAM physically arranged as a 128 × 32-bit RAM
  - AC bias signal for STN panels and a data-enable signal for TFT panels.
- Programmable Panel-related Parameters
  - STN mono/color or TFT display
  - Bits-per-pixel
  - STN 4- or 8-bit Interface Mode
  - STN Dual or Single Panel Mode
  - AC panel bias
  - Panel clock frequency
  - Number of panel clocks per line
  - Signal polarity, active HIGH or LOW
  - Little Endian data format
  - Interrupt-generation event.

ADVANCED LCD INTERFACE

The Advanced LCD Interface (ALI) allows for direct connection to ultra-thin panels that do not include a timing ASIC. It converts TFT signals from the Color LCD controller to provide the proper signals, timing and levels for direct connection to a panel's Row and Column drivers for AD-TFT, HR-TFT, or any technology of panel that allows for a connection of this type. The ALI also provides a bypass mode that allows interfacing to the built-in timing ASIC in standard TFT and STN panels.

NOTES:
1. The Advanced LCD Interface pertains to the LH75401 and LH75411 microcontrollers.
2. VGA and XGA modes require 66 MHz core speed.

Universal Asynchronous Receiver Transmitters (UARTs)

The LH75400/01/10/11 microcontrollers incorporate three UARTs, designated UART0, UART1, and UART2.

UART 0 AND 1 FEATURES

- Similar functionality to the industry-standard 16C550
- Supported baud rates up to 921,600 baud (given an external crystal frequency of 14.756 MHz)
- Supported character formats:
  - Data bits per character: 5, 6, 7, or 8
  - Parity generation and detection: Even, odd, stick, or none
  - Stop bit generation: 1 or 2
- Full-duplex operation
- Separate transmit and receive FIFOs, with:
  - Programmable depth (1 to 16)
  - Programmable-service 'trigger levels' (1/8, 1/4, 1/2, 3/4, and 7/8)
  - Overrun protection.
- Programmable baud-rate generator that:
  - Enables the UART input clock to be divided by 16 to 65,535 × 16
  - Generates an internal clock common to both transmit and receive portions of the UART.
- DMA support
- Support for generating and detecting breaks during UART transactions
- Loopback testing.

Reset, Clock, and Power Controller (RCPC)

The RCPC lets users control System Reset, clocks, power management, and external interrupt conditioning via the AMBA APB interface. This control includes:

- Enabling and disabling various clocks
- Managing power-down sequencing
- Selecting the sources for various clocks.

The RCPC provides for an orderly start-up until the crystal oscillator stabilizes and the PLL acquires lock. If users want to change the system clock frequency during normal operation, the RCPC ensures a seamless transition between the old and new frequencies.

RCPC FEATURES

- Manages five Power Modes for minimizing power consumption: Active, Standby, Sleep, Stop1, and Stop2
- Generates the system clock (HCLK) from either the PLL clock or the PLL-bypassed (oscillator) clock, divided by 2, 4, 6, 8, … 30
- Generates three UART clocks from oscillator clock
- Generates the 1 Hz RTC clock
- Generates the SSP and LCD clocks from HCLK, divided by 1, 2, 4, 8, 16, 32, or 64
- Provides a selectable external clock output
- Generates system and RTC Resets based on an external reset, Watchdog Timer reset, or soft reset
- Configures seven HIGH/LOW-level or rising/falling edge-trigger external interrupts and converts them to HIGH-level trigger interrupt outputs required by the VIC
- Generates remap outputs used by the memory map decoder
- Provides an identification register
- Supports external or watchdog reset status.

Operating Modes

The LH75400/01/10/11 microcontrollers support three operating modes:

- Normal Mode
- PLL Bypass Mode, where the internal PLL is bypassed and an external clock source is used; otherwise the chip operates normally
- EmbeddedICE Mode, where the JTAG port accesses the TAP Controller in the core and the core is placed in Debug Mode.

The state of the TEST1, TEST2, and nRESETIN signals determines the operating mode entered at Power-on Reset (see Table 15).

Table 15. Device Operating Modes

OPERATING MODE	TEST2	TEST1	nRESETIN
Reserved	0	0	0
PLL Bypass	0	0	1
Reserved	0	1	x
Reserved	1	0	0
EmbeddedICE	1	0	1
Normal	1	1	x

NOTE: TEST1, TEST2, and nRESETIN are latched on the rising edge of nPOR. The microcontroller stays in that operating mode until power is removed or nPOR transitions from LOW to HIGH.

General Purpose Input/Output (GPIO)

The LH75400/01/10/11 microcontrollers have 10 GPIO ports:

- Seven 8-bit ports
- Two 7-bit ports
- One 6-bit port.

The GPIO ports are designated A through J and provide 76 bits of programmable input/output (see Table 16). Pins of all ports, except Port J, can be configured as inputs or outputs. Port J is input only. Upon System Reset, all ports default to inputs.

Table 16. GPIO Ports

PORT	PROGRAMMABLE PINS
A	8 Input/Output Pins
B	6 Input/Output Pins
C	8 Input/Output Pins
D	7 Input/Output Pins
E	8 Input/Output Pins
F	7 Input/Output Pins
G	8 Input/Output Pins
H	8 Input/Output Pins
I	8 Input/Output Pins
J	8 Input Pins

Table 19. LCD External Pin Multiplexing (LH75400 and LH75410)

EXTERNAL PIN	DEFAULT MODE (NO LCD)	4-BIT MONO STN MODE		8-BIT MONO STN MODE
		SINGLE	DUAL	
PG4/LCDVEEEN	PG4	LCDVEEEN	LCDVEEEN	LCDVEEEN
PG3/LCDVDDEN	PG3	LCDVDDEN	LCDVDDEN	LCDVDDEN
PG2/LCDDSPLEN	PG2	LCDDSPLEN	LCDDSPLEN	LCDDSPLEN
PG1	PG1	PG1	PG1	PG1
PG0	PG0	PG0	PG0	PG0
PH7/LCDDCLK	PH7	LCDDCLK	LCDDCLK	LCDDCLK
PH6/LCDLP	PH6	LCDLP	LCDLP	LCDLP
PH5/LCDFP	PH5	LCDFP	LCDFP	LCDFP
PH4/LCDEN	PH4	LCDEN	LCDEN	LCDEN
PH3/LCDVD11	PH3	PH3	MLSTN3	PH3
PH2/LCDVD10	PH2	PH2	MLSTN2	PH2
PH1/LCDVD9	PH1	PH1	MLSTN1	PH1
PH0/LCDVD8	PH0	PH0	MLSTN0	PH0
PI7/LCDVD7	PI7	PI7	PI7	MUSTN7
PI6/LCDVD6	PI6	PI6	PI6	MUSTN6
PI5/LCDVD5	PI5	PI5	PI5	MUSTN5
PI4/LCDVD4	PI4	PI4	PI4	MUSTN4
PI3/LCDVD3	PI3	MUSTN3	MUSTN3	MUSTN3
PI2/LCDVD2	PI2	MUSTN2	MUSTN2	MUSTN2
PI1/LCDVD1	PI1	MUSTN1	MUSTN1	MUSTN1
PI0/LCDVD0	PI0	MUSTN0	MUSTN0	MUSTN0

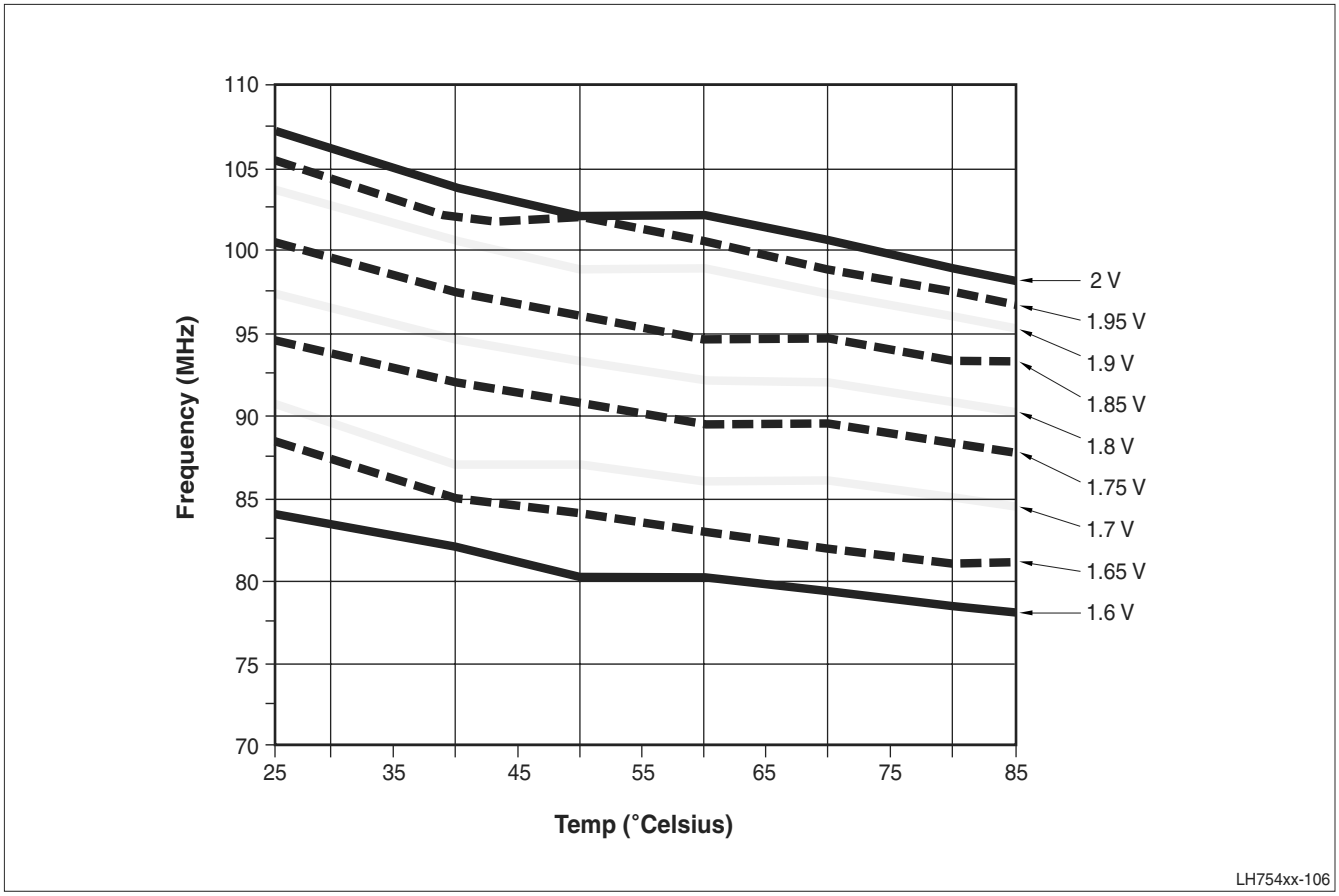


Figure 10. Maximum Core Frequency versus Voltage and Temperature

Very Low Operating Temperatures and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

SHARP recommends that users implementing a system to meet low industrial temperature standards should use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (ie, noise immunity of the clock input to the SoC.

POWER SUPPLY SEQUENCING

When using an external 1.8 V supply (instead of the internal 1.8 V regulator), the external 1.8 V power supply must be energized before the 3.3 V supply. Otherwise, the 1.8 V supply may not lag the 3.3 V supply by more than 10 µs.

If a longer delay time is needed, the voltage difference between the two power supplies must be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

LINEAR REGULATOR

Although this device contains an on-board regulator, using its output to power external devices is not recommended. External loads can affect the regulator's stability and introduce noise into the supply. SHARP cannot guarantee device performance at rated speeds and temperatures with external loads connected to this supply.

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make this data more usable, the values presented in Table 26 were derived under the conditions presented here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All I/O loads at maximum (50 pF)
- All voltages at maximum specified values
- Maximum specified ambient temperature.

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- SPI, Timer, and UART peripherals operating; all other peripherals disabled
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate
- I/O loads at nominal
- FCLK = 51.6 MHz; HCLK = 51.6 MHz
- All voltages at typical values
- Nominal case temperature.

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 27 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the peripheral clock running at maximum frequency, typical conditions, and no I/O loads. This current is supplied by the 1.8 V power supply.

Table 26. Current Consumption by Mode

SYMBOL	PARAMETER	TYP.	UNITS
ACTIVE MODE			
ICHIP	Chip Current with Linear Regulator	50.2	mA
ICORE	Core Current without Linear Regulator	42.1	mA
IIO	I/O Current without Linear Regulator	5	mA
IANALOG	Analog Current	1.3	mA
STANDBY MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	42.7	mA
ICORE	Core Current without Linear Regulator	34.6	mA
IIO	Current drawn by I/O	0.8	mA
IANALOG	Analog Current	1.3	mA
SLEEP MODE (TYPICAL CONDITIONS ONLY)			
ICHIP	Core Current with Linear Regulator	3.9	mA
ICORE	Core Current without Linear Regulator	2.5	mA
IIO	Current drawn by I/O	400	µA
IANALOG	Analog Current	1.2	mA
STOP1 MODE			
ISTOP	Core Current with Linear Regulator, I/O, and 14.7456 MHz osc.	2.96	mA
STOP2 MODE (RTC ON)			
ILEAK	Leakage Current, Core and I/O	34	µA
STOP2 MODE (RTC OFF)			
ILEAK	Leakage Current, Core and I/O	18	µA

NOTES:
1. ICHIP = Chip Current with Linear Regulator (Core + I/O)
2. ICORE, IIO, IANALOG are the respective current consumption specifications for VDDC, VDD, and VDDA.

Table 27. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
UARTs	200	µA
RTC	5	µA
DMA	4.1	mA
SSP	500	µA
Counter/Timers	200	µA
LCD	2.2	mA

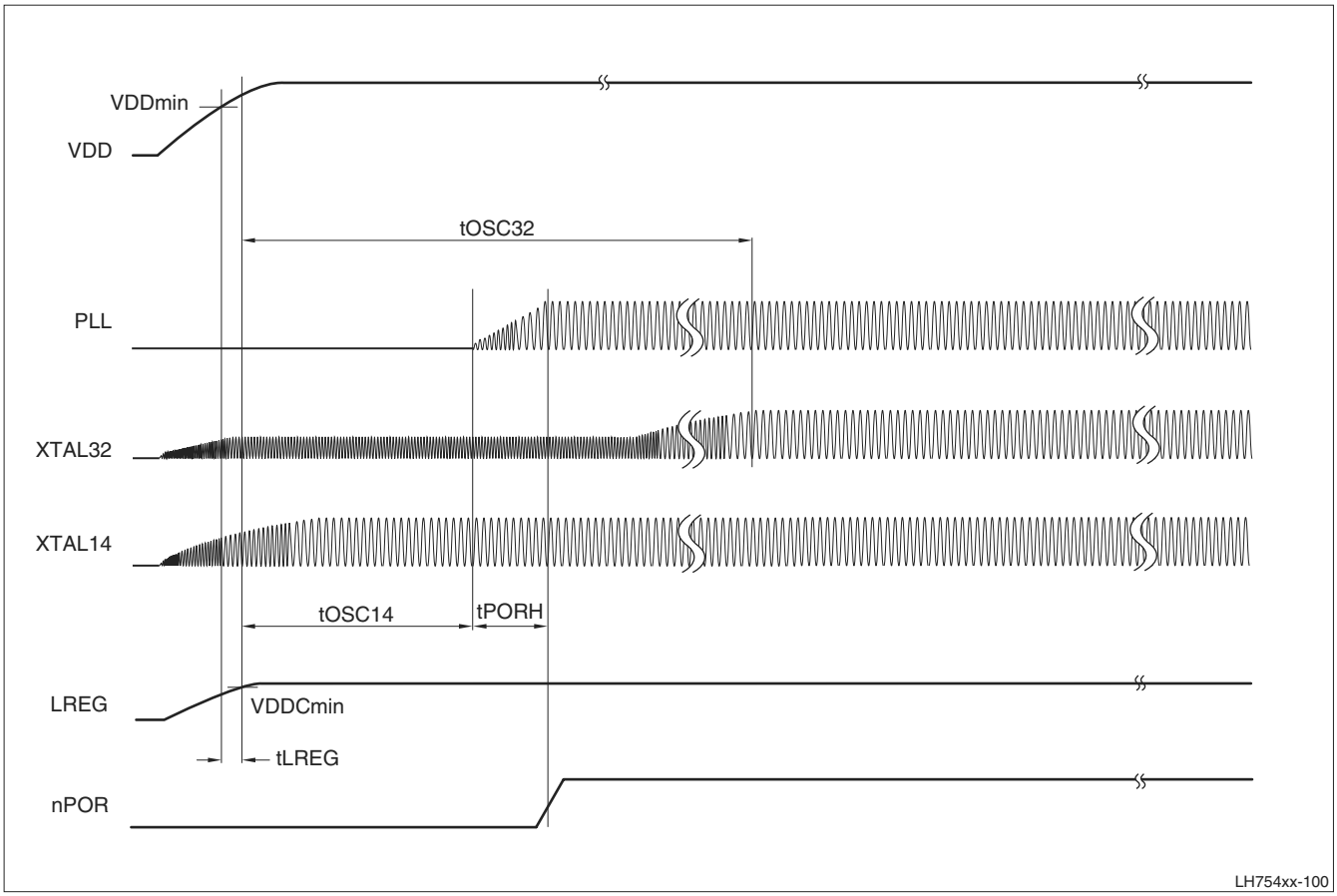


Figure 12. Power-up Stabilization

MEMORY CONTROLLER WAVEFORMS

Static Memory Controller Waveforms

Figure 13 shows the waveform and timing for an External Static Memory Write, with one Wait State. Figure 14 shows the waveform and timing for an External Static Memory Write, with two Wait States. Figure 15 shows the waveform and timing for an External Static Memory Read, with one Wait State.

The SMC supports an nWAIT input that can be used by an external device to extend the wait time during a memory access. The SMC samples nWAIT at the beginning of at the beginning of each system clock cycle. The system clock cycle in which the nCSx signal is asserted counts as the first wait state. See Figure 16. The SMC recognizes that nWAIT is active within 2 clock cycles after it has been asserted. To assure that the current access (read or write) will be extended by nWAIT, program at least two wait states for this bank of memory. If N wait states are programmed, the SMC holds this state for N system clocks or until the SMC detects that nWAIT is inactive, whichever occurs last. As the number of wait states programmed increases, the amount of delay before nWAIT must be asserted also increases. If only 2 wait states are programmed, nWAIT must be asserted in the clock cycle immediately following the clock cycle during which the nCSx signal is asserted. Once the SMC detects that the external device has deactivated nWAIT, the SMC completes its access in 3 system clock cycles.

The formula for the allowable delay between asserting nCSx and asserting nWAIT is:

tASSERT = (system clock period) × (Wait States - 1)
(where Wait States is from 2 to 31.)

The signal tIDD is shown without a setup time, as measurements are made from the Address Valid point and HCLK is an internal signal, shown for reference only.

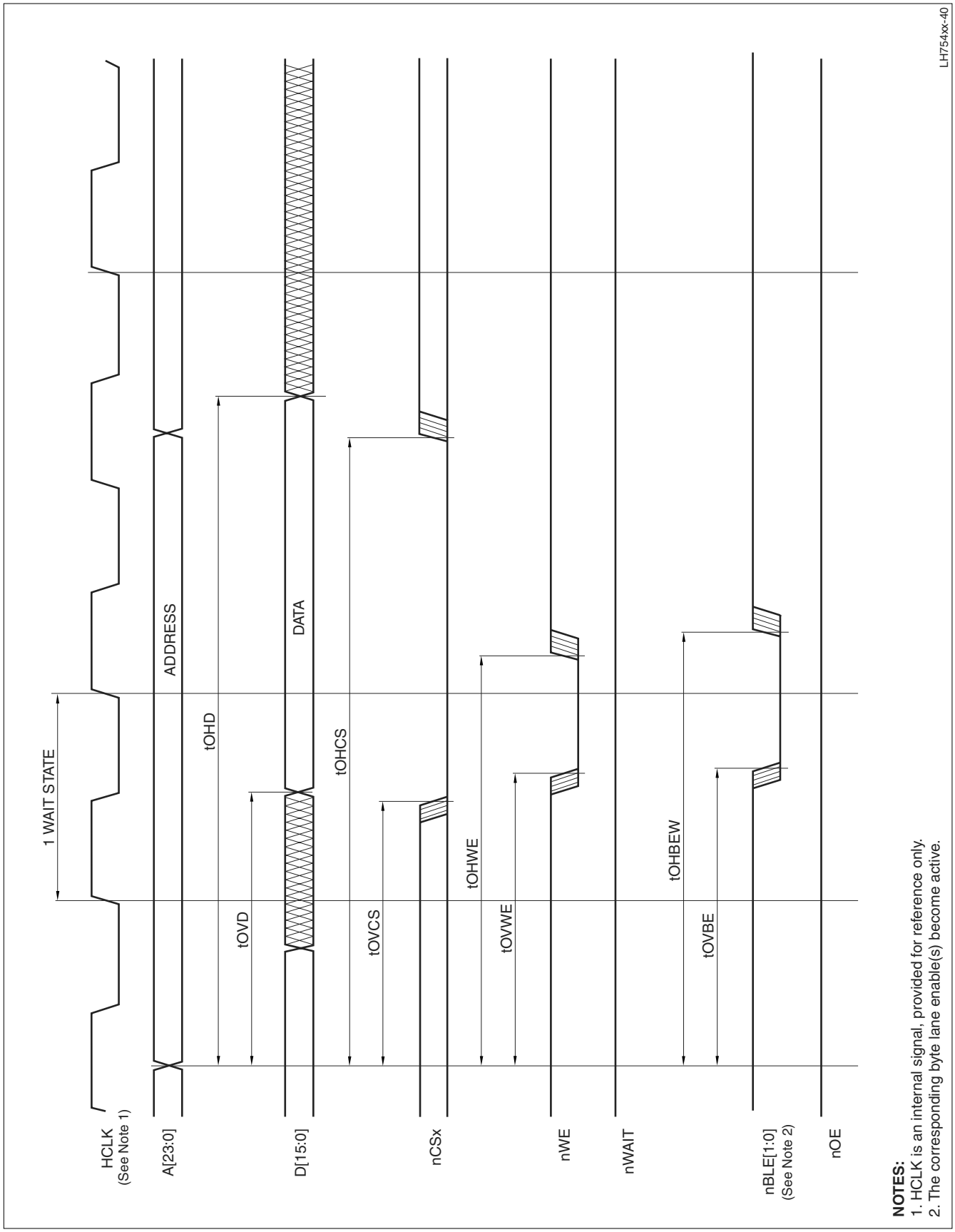


Figure 13. External Static Memory Write, One Wait State

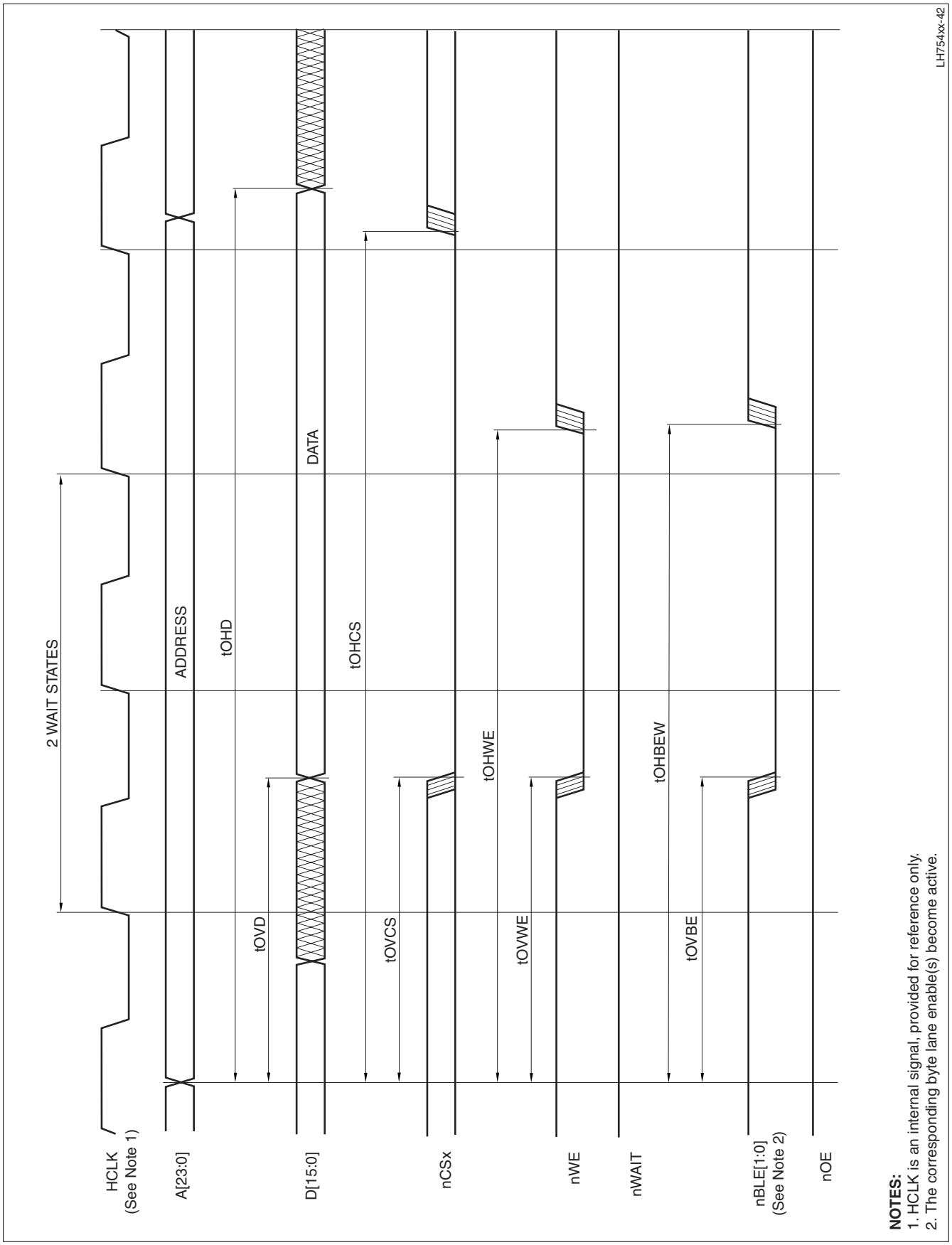


Figure 14. External Static Memory Write, Two Wait States

Synchronous Serial Port Waveform

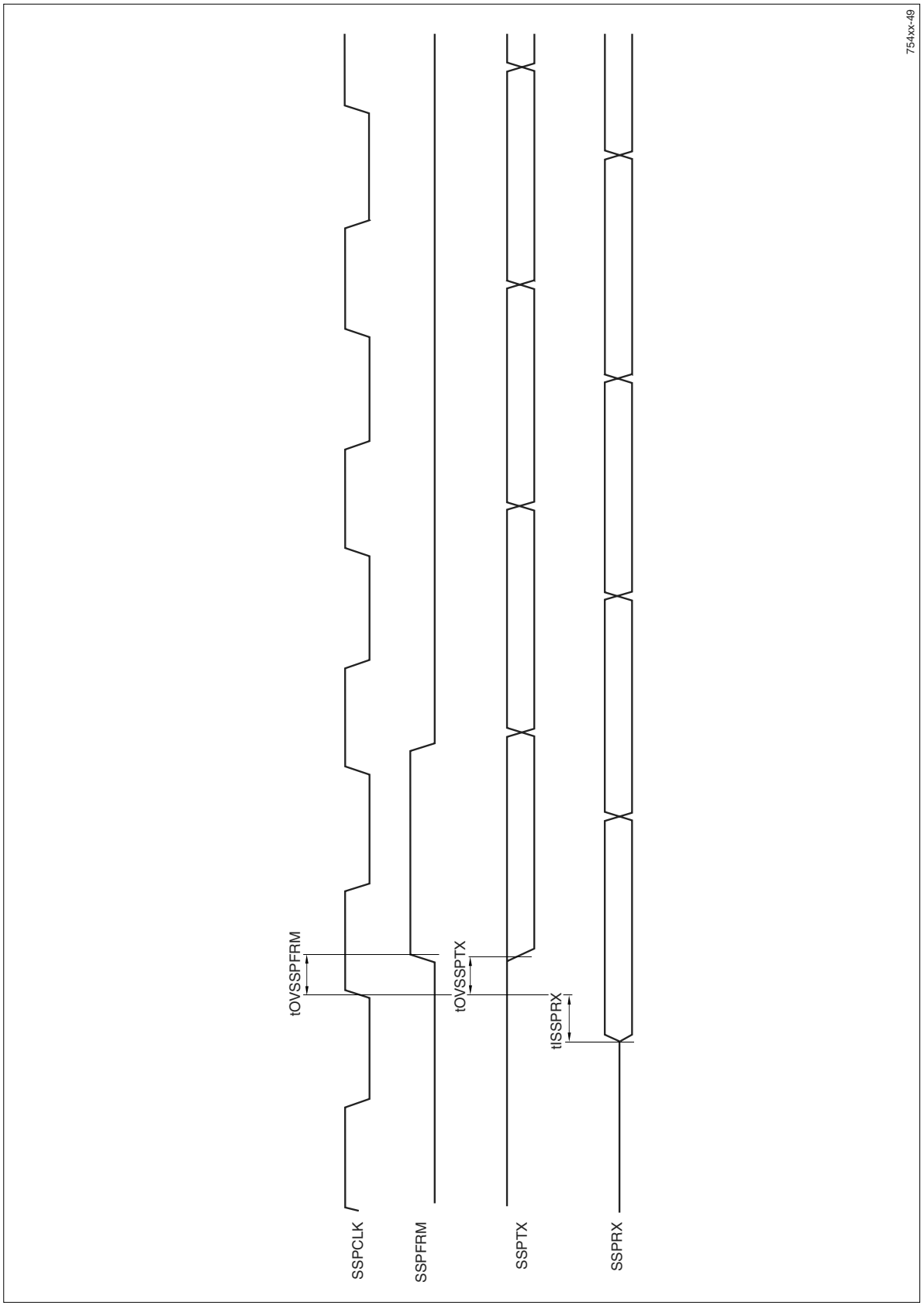


Figure 17. Synchronous Serial Port Waveform

DMA Controller Timing Diagrams

Figure 18 and Figure 19 show examples of DMA timing diagrams.

- Figure 18 shows the timing for a peripheral-to-memory data transfer, where SoSize = DeSize and SoBurst = 4.
- Figure 19 shows the timing for a memory-to-peripheral data transfer, where SoSize = DeSize and SoBurst = 4.

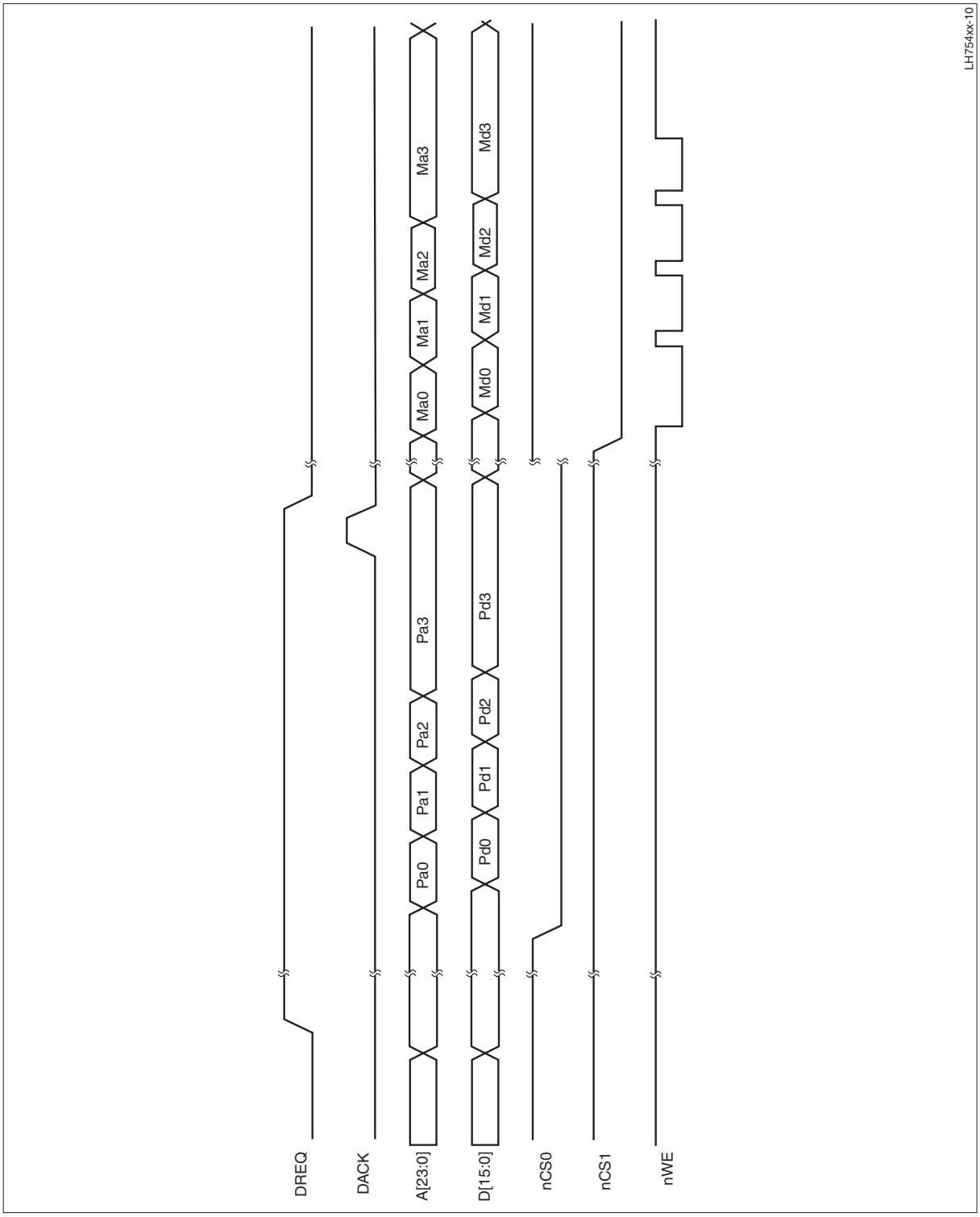
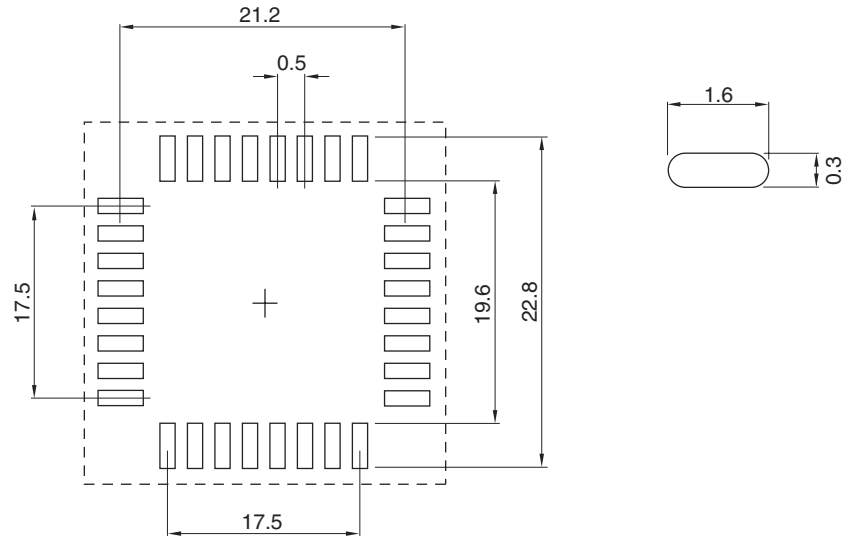


Figure 18. Peripheral-to-Memory Data-Transfer Timing

144LQFP



NOTE: Dimensions in mm.

144LQFP

Figure 29. Recommended PCB Footprint