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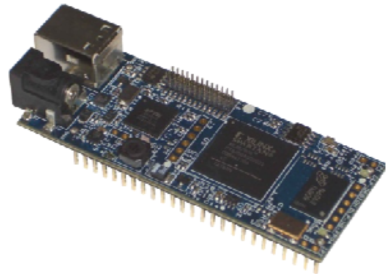
Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

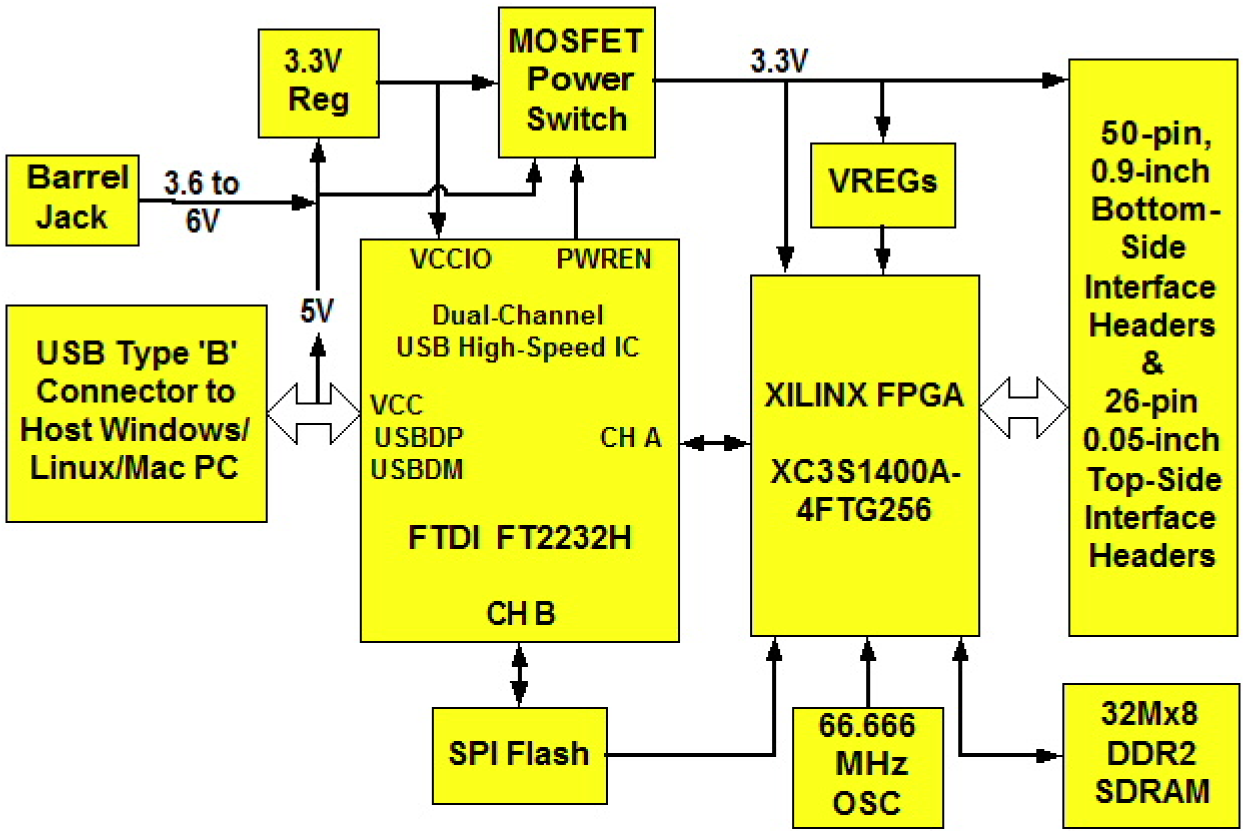
Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-3A, XC3S1400A
Co-Processor	FT2232H
Speed	66MHz
Flash Size	-
RAM Size	32MB
Connector Type	USB - B, Pin Header
Size / Dimension	3" x 1.2" (76.2mm x 30.5mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/dlp-design/dlp-hs-fpga3



DLP-HS-FPGA3
LEAD FREE

USB - FPGA MODULE



FEATURES:

- Xilinx XC3S1400A-4FTG256C FPGA Utilized on the DLP-HS-FPGA3
- Micron 32M x 8 DDR2 SDRAM Memory
- Built-In Configuration Loader; Writes the Bit File Directly to SPI Flash via High-Speed USB 2.0 Interface
- 63 User I/O Channels: 21 Differential Pairs and 8 Global Clocks
- 66.666 MHz Oscillator
- 133 MHz DDR2 Interface Reference Design Provided
- USB Port Powered or 5V External Power Barrel Jack
- USB 1.1 and 2.0 Compatible Interface
- Small Footprint: 3.0 x 1.2-Inch PCB and Standard 50-Pin, 0.9-Inch DIP Interface

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APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control
- Data Acquisition/Processing
- Embedded Processor

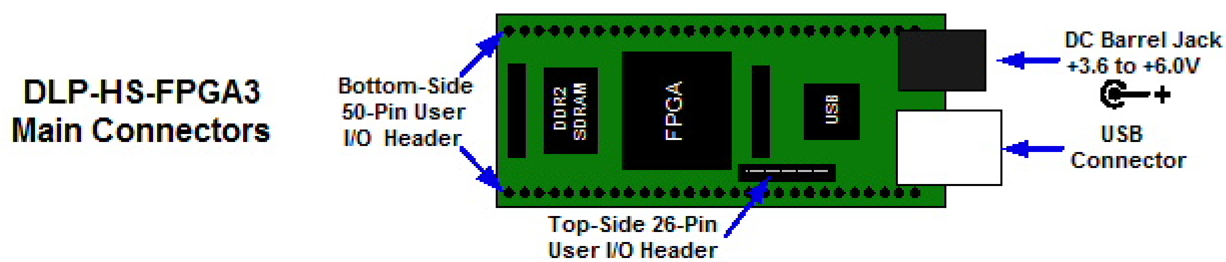
1.0 INTRODUCTION

The DLP-HS-FPGA3 module is a low-cost, compact prototyping tool that can be used for rapid proof of concept or within educational environments. The module is based on the Xilinx Spartan™ 3A and Future Technology Devices International's FT2232H Dual-Channel High-Speed USB IC. The DLP-HS-FPGA3 provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the free ISE™ WebPACK™ tools from Xilinx, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

As a bonus feature, one channel of the dual-channel USB interface is used to load user bit files directly to the SPI Flash—no external programmer is required. This represents a savings of as much as $200 in that no additional programming cable is required for configuring the FPGA. All that is needed to load bit files to the DLP-HS-FPGA3 is a Windows software utility (free with purchase), a Windows PC and a USB cable. The module can also be programmed from within the Xilinx ISE tool environment using a Xilinx programming cable (purchased separately).

The DLP-HS-FPGA3 is fully compatible with the free ISE™ WebPACK™ tools from Xilinx. ISE™ WebPACK™ offers the ideal development environment for FPGA designs with HDL synthesis and simulation, implementation, device fitting and JTAG programming.

The DLP-HS-FPGA3 has on-board voltage regulators that generate all required power supply voltages from a single, 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply via an onboard standard barrel connector.



Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025-square inch post DIP header on the bottom of the board and a 26-pin, 0.05-inch wide top-side 2x13 header. The bottom-side 50-pin header provides access to 41 of the FPGA user input/output pins. The top-side header provides access to 22 of the FPGA user input/output pins. The bottom-side header mates with a user-supplied, standard, 50-pin, 0.9-inch spaced DIP socket. The top-side header mates with a user-supplied, 0.05-inch spaced, 2x13 connector such as the FFSD-13-D-xx.xx-01 (xx.xx = cable length) ribbon cable assembly from Samtec.

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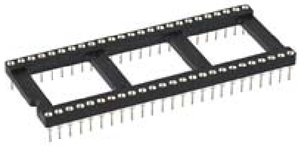
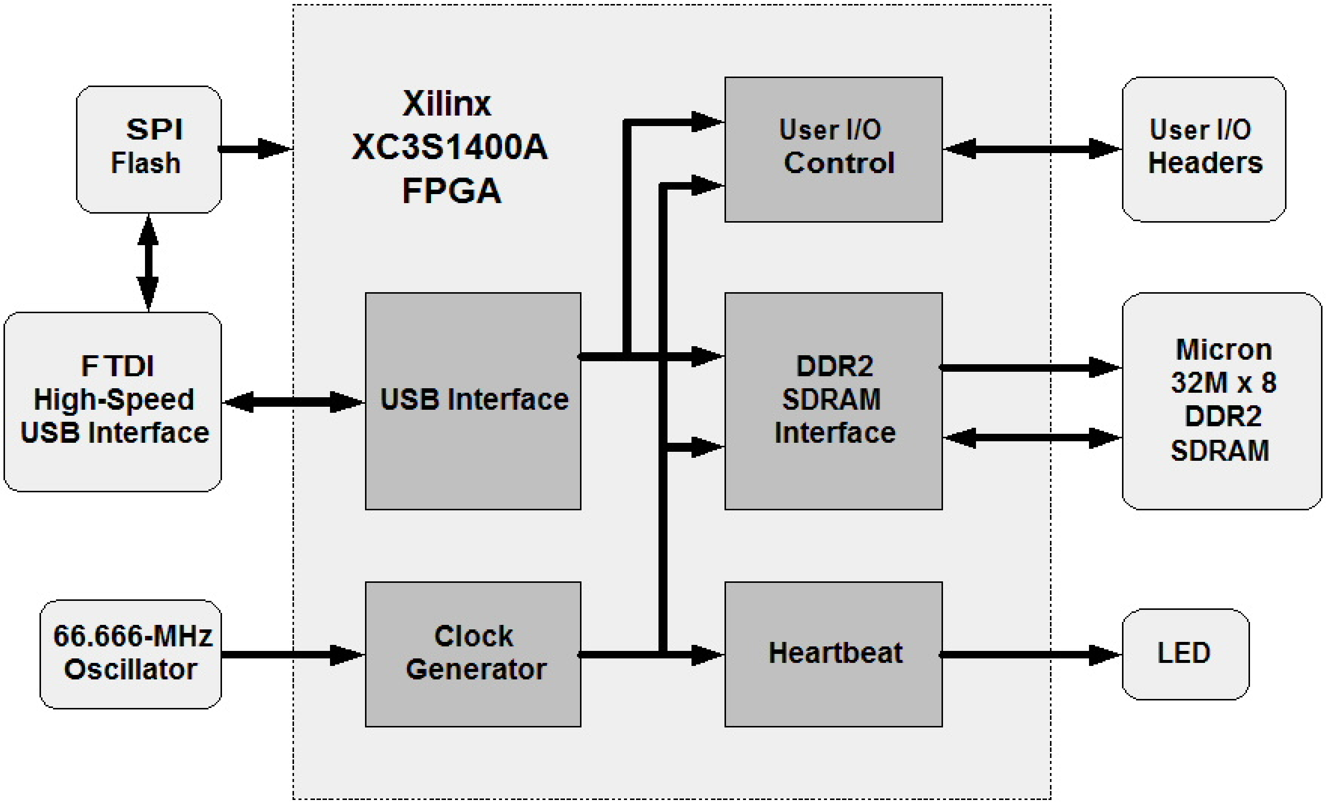
DIP Socket  **Ribbon Cable** 

Other on-board features include a 32M x 8 DDR2 SDRAM memory IC for user projects and both JTAG and SPI Flash interface ports for connection to Xilinx programming tools.

2.0 REFERENCE DESIGN

A 10,000-line reference design is available for the Spartan™ 3A FPGA on the DLP-HS-FPGA3 to those who purchase the module. The design was written in VHDL and built using the free Xilinx ISE™ WebPACK™ tools. The reference design consists of the following blocks:



It contains a USB Interface Block, a User I/0 Block, a DDR2 SDRAM interface, a Heartbeat Pulse Generator and a Clock Generator. The SPI Flash is used to store the design's FPGA configuration file.

The USB interface captures, interprets and returns command and data information sent from the host PC through the FTDI USB interface to the FPGA. Commands include Ping, Return Status, Loopback Data, Set a User I/O Pin High or Low, Read a User I/O Pin, Initialize the DDR2 SDRAM Memory and Read (from) or Write (to) the DDR2 SDRAM Memory. (Section 11 explains these in detail.)

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The User I/O Block controls access to the 63 user I/O pins accessible through the top- and bottom-side headers. Every one of these pins can be either an input or an output. The User I/O Block can configure these pins as inputs and read their state, or as outputs and drive them high or low. (As a side note, 48 of these user I/O pins can be configured as 24 differential pairs, 8 can be configured as global clock inputs and 6 can be configured as regional clock inputs.)

The DDR2 SDRAM interface block manages the memory's initialization, the refresh cycle and the read and write access. Read and write access is available in 4-byte bursts. The traces between the DDR2 SDRAM and FPGA are matched within 10 mils to accommodate reliable data transfer at 266 Mbit/s (clocked at 133MHz). The interface creates and aligns the Data Strobes (DQS) based on an external feedback trace that matches two times the trace length between the FPGA and the DDR2 SDRAM. The Initialization, Read and Write commands are initiated by the USB interface block and executed by the DDR2 SDRAM interface block.

The Heartbeat Pulse Generator takes the internal system clock and divides it down so that the onboard Heartbeat LED will be turned on and off for a duration of approximately one-half second.

The Clock Generator Block receives the 66.666-MHz clock and produces both the 133-MHz clocks required to run the DDR2 SDRAM memory device and the 100-MHz clock for the remaining internal logic in the FPGA. It also handles reset and lock synchronization between internal DCM blocks.

The design occupies the following FPGA resources on the DLP-HS-FPGA3 module's XC3S1400A:

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	1,263	22,528	5%
Number of 4 input LUTs	1,182	22,528	5%
Number of occupied Slices	1,157	11,264	10%
Number of Slices containing only related logic	1,157	1,157	100%
Number of Slices containing unrelated logic	0	1,157	0%
Total Number of 4 input LUTs	1,254	22,528	5%
Number used as logic	1,066		
Number used as a route-thru	72		
Number used for Dual Port RAMs	32		
Number used as Shift registers	84		
Number of bonded IOBs	123	161	76%
IOB Flip Flops	20		
IOB Master Pads	2		
IOB Slave Pads	2		
Number of ODDR2s used	12		
Number of BUFGMUXs	7	24	29%
Number of DCMs	2	8	25%
Number of RPM macros	1		
Average Fanout of Non-Clock Nets	3.04		

More reference designs are planned. Please contact DLP Design with any specific requests.

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3.0 FPGA SPECIFICATIONS

The FPGA device used on the DLP-HS-FPGA3 is the Xilinx Spartan™ 3A:

- Part Number: XC3S1400A-4FTG256C
- System Gates: 1,400,000
- Equivalent Logic Cells: 25,344

- CLB Array:

  Rows: 72
  Columns: 40
  Total CLB's: 2,816
  Total Slices: 11,264
  Total Flip Flops: 22,528
  Total 4-Input LUT's: 22,528

- Distributed RAM Bits: 176K
- Block RAM Bits: 576K
- Dedicated Multipliers: 32
- DCM's: 8

4.0 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed here may cause permanent damage to the DLP-HS-FPGA3:

Operating Temperature: 0-70°C

Voltage on Digital Inputs with Respect to Ground: -0.5V to +4.1 V

Sink/Source Current on Any I/O: 24 mA (using LVTTL as the FPGA I/O standard)

5.0 WARNINGS

- Unplug from the host PC and power adapter before connecting to I/O on the DLP-HS-FPGA3.

- Isolate the bottom of the board from all conductive surfaces.

- Observe static precautions to prevent damage to the DLP-HS-FPGA3 module.

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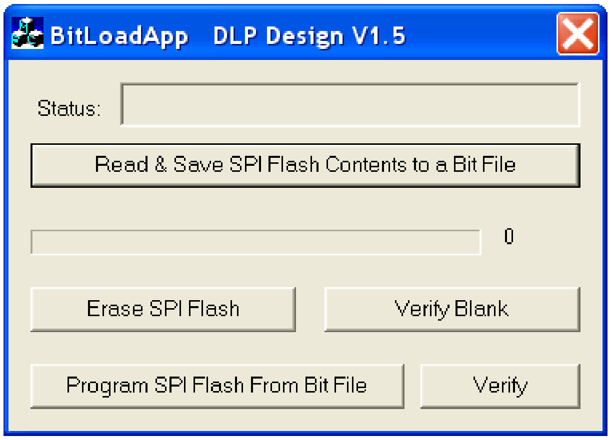
6.0 BITLOADAPP SOFTWARE

Windows software is provided for use with the DLP-HS-FPGA3 that will load an FPGA configuration (*.bit) file directly to the SPI Flash device via the USB interface. This application (illustrated below) will allow the user to erase the Flash, verify the erasure and then program and verify the Flash:



7.0 JTAG INTERFACE

The easiest way to load an FPGA configuration (*.bit) file to the FPGA is to run the BitLoadApp software then select and program a file from the local hard drive directly to the SPI Flash. Once written to the SPI Flash, the configuration will load to the FPGA and execute. Alternatively, a traditional JTAG header location is provided on the DLP-HS-FPGA3 giving the user access to the specific pins required by the development tools. (Refer to the schematic contained within this datasheet for details.)

8.0 EEPROM SETUP / MPROG

The DLP-HS-FPGA3 has a dual-channel USB interface to the host PC. Channel B is used exclusively to load an FPGA configuration (*.bit) file to the SPI Flash. This configuration data is automatically transferred to the FPGA when power is applied to the module or when the PROG pin is driven low and then released by the application software. Channel A is used for communication between the FPGA and the host PC at run time. A 93LC56B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

As mentioned above, Channel B is used exclusively for loading the FPGA's configuration to the SPI Flash, and Channel A is used for communication between the host PC and the DLP-HS-FPGA3. As such, the D2XX drivers and 245 FIFO mode must be selected in the EEPROM for Channel B. Channel A must use the 245 FIFO mode, but it can use either the VCP or D2XX drivers. The VCP drivers make the DLP-HS-FPGA3 appear as an RS232 port to the host application. The D2XX drivers provide faster throughput but require working with a *.lib or *.dll library in the host application.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at **www.dlpdesign.com**.

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9.0 TEST BIT FILE

A test file is provided as a download from the DLP Design website that provides rudimentary access to the I/O features of the DLP-HS-FPGA3. The following features are provided:

- Ping
- Read the High/Low State of the Input-Only Pins
- Drive I/O Pins High/Low or Read their High/Low State
- Simple Loopback on Channel A
- 4-Byte Read/Write Access of the Row, Column, and Bank Address in the DDR2 SDRAM

This bit file is available from the DLP-HS-FPGA3 download page. The command structure that supports these features is explained in Section 11.

10.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at **www.dlpdesign.com**:

OPERATING SYSTEM SUPPORT	
Windows 7 32-bit	**Windows 7 64-bit**
Windows Vista, Vista x64	**Mac OSX**
Windows XP, XP x64	**Mac OS9**
Windows Server 2008, x64	**Mac OS8**
Windows Server 2003, x64	**Linux**
Windows 2000	**Windows CE 4.2 – 6.0**

Notes:

1. The bit file load utility only runs on the Windows platforms.

2. The bit file load utility requires the use of USB channel B, and channel B is dedicated to this function.

3. If you are utilizing the dual-mode drivers from FTDI (CDM2.x.x) and you want to use the Virtual COM Port (VCP) drivers, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the entry under USB Controllers that appears when the DLP-HS-FPGA3 is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Then unplug and replug the DLP-HS-FPGA3, and a COM port should appear in Device Manager under Ports (COM & LPT).

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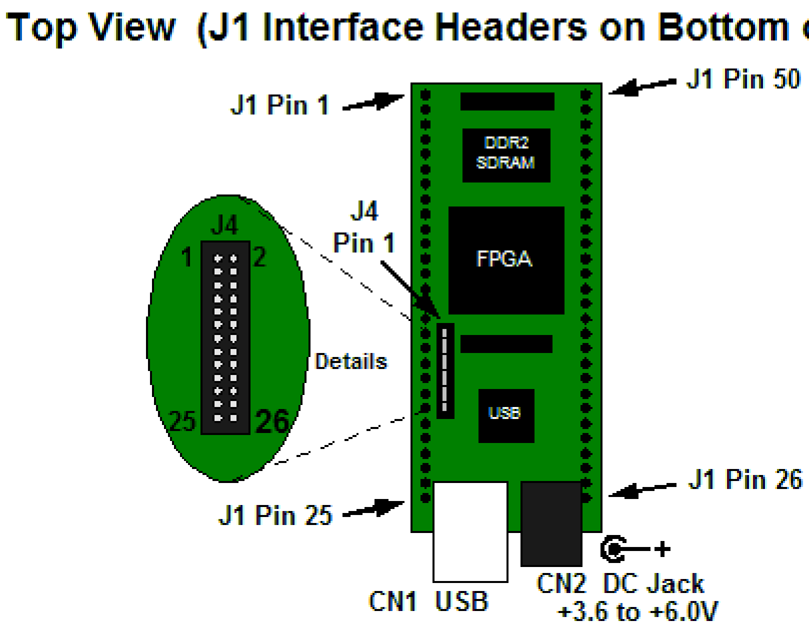
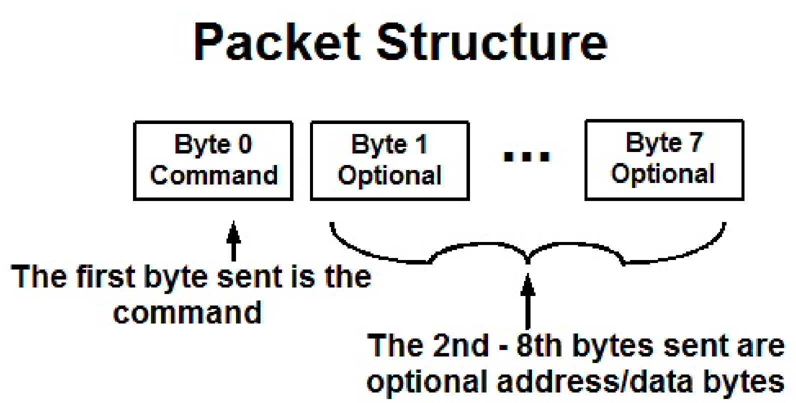
11.0 USING THE DLP-HS-FPGA3

Select a power source via Header Pins 23 and 24, and connect the DLP-HS-FPGA3 to the PC to initiate loading of the USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-HS-FPGA3 is ready for use.



Simply connect the DLP-HS-FPGA3 to the PC to initiate the loading of USB drivers.



You can either utilize the Test Application available from **http://www.dlpdesign.com/test.shtml** with the DLP-HS-FPGA3 (as described in Section 12), or you can write your own program in your language of choice.

If you are using the VCP drivers, begin by opening the COM port, and send multi-byte commands as shown in Table 1 below. There is no need to set the baud rate because the DLP-HS-FPGA3 uses a parallel interface between the USB IC and the FPGA. (The Ping Command can be used to locate the correct COM port used for communicating with the DLP-HS-FPGA3, or you can look in Device Manager to see which port was assigned by Windows.) If you are using the D2XX drivers as with the Test Application, no COM port selection is necessary.

TABLE 1

Command Packets				
Command Packet	**Description**	**Byte**	**Hex Value**	**Return/Comments**
Ping	Issues Ping	0	0x00	Ping Command - 0x56 will be returned indicating that the DLP-HS-FPGA3 is found on the selected port.
Read Version/ Status	Accesses the internal version/ status registers	0	0x10	Read Version/Status Registers Command
		1	0xnn	Register Address: 0xnn = 0x00 = Board ID (0x30 = Production PCB) 0x01 = FPGA Type ID : 0x6A = XC3S1400A 0x02 = Design Version ID 1 (Design Month) 0x03 = Design Version ID 2 (Design Day) 0x04 = Design Version ID 3 (Design Year) 0x05 = Design Version ID 4 (Design Version) 0x06 = DDR2 Status: 0x00 = Not Initialized 0x01 = Initialized
Loopback	Returns the data byte received	0	0x20	Loopback Command
		1	0xnn	The byte sent to the DLP-HS-FPGA3 (0xnn) will be returned back.
Loopback Compliment	Returns the compliment of data byte received	0	0x21	Loopback Compliment Command
		1	0xnn	The byte sent to the DLP-HS-FPGA3 (0xnn) will be complimented and returned back.
Read Pin	Reads the state of one of the user I/O pins	0	0x30	Read Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is read and returns: 0x00 = User I/O pin 0xnn is low 0x01 = User I/O pin 0xnn is high
Clear Pin	Forces the selected user I/O pin low	0	0x40	Clear Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is cleared. The specified user I/O number is returned.
Set Pin	Forces the selected user I/O pin high	0	0x41	Set Pin Command
		1	0x00 – 0x3E	The user I/O pin numbers are described in Table 2. User I/O pin 0xnn is set. The specified user I/O number is returned.
Initialize Memory	Initializes DDR2 SDRAM	0	0x70	The Initialize Memory Command configures the DDR2 SDRAM for access by the FPGA. **The memory cannot be accessed without being initialized.**

IMPORTANT NOTE ON DDR2 SDRAM DATA ACCESS:

Writes and reads made to and from the DDR2 SDRAM using the reference design on the DLP-HS-FPGA3 module are always performed **4 bytes at a time** due to the fact that the device is configured for a burst length of four. What this means is that Column Address Bits 0 and 1 only change the order of the read or write bytes; they still refer to the same 4 bytes. Therefore, to increment the DDR2 SDRAM address for consecutive memory locations, the column address must be incremented by 4.

Incrementing the column address by anything less than 4 simply changes the order in which the 4 bytes specified by Column Address 9:3 are written to the memory or returned to the user.

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For example, a write to a column starting address of 0 will write to column locations 0, 1, 2 and 3. But if the user then writes to column address 1, they will actually be writing to column locations 1, 2, 3 and 0, which will overwrite the previous write operation.

More details on how the DDR2 SDRAM column bits 1 and 0 function can be found in Figure 4 and Table 40 of the Micron™ MT47H32M8 datasheet. For details on how the bank, row and column bits are sent via USB to the memory, refer to the commands below:

Memory Read	Reads 4 bytes from the DDR2 SDRAM	0	0x8n	Reads 4 bytes from the DDR2 SDRAM starting with the address specified. The command byte is OR'd with the Most Significant Row Address Bit (24). n = 0 the Most Sig Row Address Bit is low (0x80) n = 1 the Most Sig Row Address Bit is high (0x81)
		1	0xah	Bits 23-16: Middle 8 bits of Row Address to be read from
		2	0xam	Bits 15-12: Lower 4 bits of Row Address to be read from Bits 11-8: Upper 4 bits of Column Address to be read from
		3	0xal	Bits 7-2: Lower 6 bits of Column Address to be read from **NOTES:** Refer to the text above regarding Column Bits 1 and 0 (equates to 0xal bits 3-2). Bits 1-0: Bank Address to be read from. If the memory has not been initialized, the data returned will be invalid, and the command returned will be 0xE7 indicating the error.
Memory Write	Writes 4 bytes to the DDR2 SDRAM	0	0x9n	Writes 4 bytes to the DDR2 SDRAM starting with the address specified. The command byte is OR'd with the Most Significant Row Address bit (24). n = 0 the Most Sig Row Address Bit is low (0x90) n = 1 the Most Sig Row Address Bit is high (0x91)
		1	0xah	Bits 23-16: Middle 8 bits of Row Address to be written to
		2	0xam	Bits 15-12: Lower 4 bits of Row Address to be written to Bits 11-8: Upper 4 bits of Column Address to be written to
		3	0xal	Bits 7-2: Lower 6 bits of column address to be written to **NOTE:** Refer to the text above regarding Column Bits 1 and 0 (equates to 0xal bits 3-2). Bits 1-0: Bank Address to be written to
		4	0xd0	Data Byte 0 written to Address Specified
		5	0xd1	Data Byte 1 written to Address Specified + 1
		6	0xd2	Data Byte 2 written to Address Specified + 2
		7	0xd3	Data Byte 3 written to Address Specified + 3. Returns the 4 bytes written followed by an echo back of the command and address data sent. **NOTE:** If the memory has not been initialized, the command returned will be 0xE7 indicating the error.

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The USER I/O Pin Read/Set/Clear Commands I/O number mapping to the physical I/O pins on the DLP-HS-FPGA3 board are described in the following table:

TABLE 2 User I/O				
I/O Number	**DLP-HS-FPGA3 Pin**	**XC3S1400A Pin**	**XC3S1400A Bank**	**FPGA Pin Configurations Available**
0x00 (0)	J1 Pin 2	D13	0	Digital Input, Output, Differential Pair 0+
0x01 (1)	J1 Pin 3	C13	0	Digital Input, Output, Differential Pair 0-
0x02 (2)	J1 Pin 4	D12	0	Digital Input, Output, Differential Pair 1-
0x03 (3)	J1 Pin 5	C12	0	Digital Input, Output, Differential Pair 1+
0x04 (4)	J1 Pin 6	C10	0	Digital Input, Output, Differential Pair 2+, Global Clock
0x05 (5)	J1 Pin 7	D9	0	Digital Input, Output, Differential Pair 2-, Global Clock
0x06 (6)	J1 Pin 8	C8	0	Digital Input, Output, Differential Pair 3+, Global Clock
0x07 (7)	J1 Pin 9	D8	0	Digital Input, Output, Differential Pair 3-, Global Clock
0x08 (8)	J1 Pin 10	A14	0	Digital Input, Output, Differential Pair 4+
0x09 (9)	J1 Pin 12	A13	0	Digital Input, Output, Differential Pair 4-
0x0A (10)	J1 Pin 13	A6	0	Digital Input, Output, Differential Pair 5+
0x0B (11)	J1 Pin 14	B6	0	Digital Input, Output, Differential Pair 5-
0x0C (12)	J1 Pin 15	C11	0	Digital Input, Output, Differential Pair 6+
0x0D (13)	J1 Pin 16	A11	0	Digital Input, Output, Differential Pair 6-
0x0E (14)	J1 Pin 17	B8	0	Digital Input, Output, Differential Pair 7-, Global Clock
0x0F (15)	J1 Pin 18	A8	0	Digital Input, Output, Differential Pair 7+, Global Clock
0x10 (16)	J1 Pin 19	C5	0	Digital Input, Output, Differential Pair 8-
0x11 (17)	J1 Pin 20	A5	0	Digital Input, Output, Differential Pair 8+
0x12 (18)	J1 Pin 21	B3	0	Digital Input, Output, Differential Pair 9-
0x13 (19)	J1 Pin 22	A3	0	Digital Input, Output, Differential Pair 9+
0x14 (20)	J1 Pin 27	F3	3	Digital Input, Output
0x15 (21)	J1 Pin 29	G2	3	Digital Input, Output
0x16 (22)	J1 Pin 30	C2	3	Digital Input, Output, Differential Pair 11+
0x17 (23)	J1 Pin 31	C1	3	Digital Input, Output, Differential Pair 11-
0x18 (24)	J1 Pin 32	E1	3	Digital Input, Output, Differential Pair 12-
0x19 (25)	J1 Pin 33	D1	3	Digital Input, Output, Differential Pair 12+
0x1A (26)	J1 Pin 34	F4	3	Digital Input, Output
0x1B (27)	J1 Pin 35	J2	3	Digital Input, Output
0x1C (28)	J1 Pin 36	C6	0	Digital Input, Output
0x1D (29)	J1 Pin 37	G3	3	Digital Input, Output
0x1E (30)	J1 Pin 38	M4	3	Digital Input, Output, Differential Pair 15-
0x1F (31)	J1 Pin 39	N3	3	Digital Input, Output, Differential Pair 15+
0x20 (32)	J1 Pin 41	E3	3	Digital Input, Output, Differential Pair 16+
0x21 (33)	J1 Pin 42	E2	3	Digital Input, Output, Differential Pair 16-
0x22 (34)	J1 Pin 43	H3	3	Digital Input, Output, Differential Pair 17+
0x23 (35)	J1 Pin 44	J3	3	Digital Input, Output, Differential Pair 17-

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0x24 (36)	J1 Pin 45	K1	3	Digital Input, Output, Differential Pair 18, Regional Clock
0x25 (37)	J1 Pin 46	K3	3	Digital Input, Output, Differential Pair 18, Regional Clock
0x26 (38)	J1 Pin 47	P1	3	Digital Input, Output, Differential Pair 19-
0x27 (39)	J1 Pin 48	N2	3	Digital Input, Output, Differential Pair 19+
0x28 (40)	J1 Pin 49	T9	2	Digital Input, Output, Global Clock
0x29 (41)	J4 Pin 1	B15	0	Digital Input, Output
0x2A (42)	J4 Pin 3	A12	0	Digital Input, Output
0x2B (43)	J4 Pin 5	B10	0	Digital Input, Output, Differential Pair 20+
0x2C (44)	J4 Pin 7	A10	0	Digital Input, Output, Differential Pair 20-
0x2D (45)	J4 Pin 9	A9	0	Digital Input, Output, Global Clock
0x2E (46)	J4 Pin 11	N1	3	Digital Input, Output
0x2F (47)	J4 Pin 13	E7	0	Digital Input, Output
0x30 (48)	J4 Pin 15	C4	0	Digital Input, Output
0x31 (49)	J4 Pin 17	C7	0	Digital Input, Output
0x32 (50)	J4 Pin 19	K4	3	Digital Input, Output
0x33 (51)	J4 Pin 21	R1	3	Digital Input, Output
0x34 (52)	J4 Pin 2	A7	0	Digital Input, Output
0x35 (53)	J4 Pin 4	A4	0	Digital Input, Output, Differential Pair 21+
0x36 (54)	J4 Pin 6	B4	0	Digital Input, Output, Differential Pair 21-
0x37 (55)	J4 Pin 8	F1	3	Digital Input, Output, Differential Pair 22+
0x38 (56)	J4 Pin 10	G1	3	Digital Input, Output, Differential Pair 22-
0x39 (57)	J4 Pin 12	H1	3	Digital Input, Output, Regional Clock
0x3A (58)	J4 Pin 14	J1	3	Digital Input, Output, Regional Clock
0x3B (59)	J4 Pin 16	L1	3	Digital Input, Output
0x3C (60)	J4 Pin 18	M1	3	Digital Input, Output
0x3D (61)	J4 Pin 20	M3	3	Digital Input, Output, Differential Pair 23+
0x3E (62)	J4 Pin 22	L4	3	Digital Input, Output, Differential Pair 23-
SUSPEND	J4 Pin 23	R16	1	Force Suspend Mode (when enabled)
AWAKE	J4 Pin 24	T11	2	Return from Suspend Mode Operation
+5V IN	J1 Pin 23	-	-	+5V input to the DLP-HS-FPGA3
+5V USB	J1 Pin 24	-	-	+5V supplied by host PC USB port
+3.3V OUT	J1 Pin 28, J4 Pin 26	-	-	+3.3V supplied by the onboard regulator after module enumerated
GND	J1 Pin 1, J1 Pin 11, J1 Pin 25, J1 Pin 26, J1 Pin 40, J1 Pin 50, J4 Pin 25	-	-	Ground

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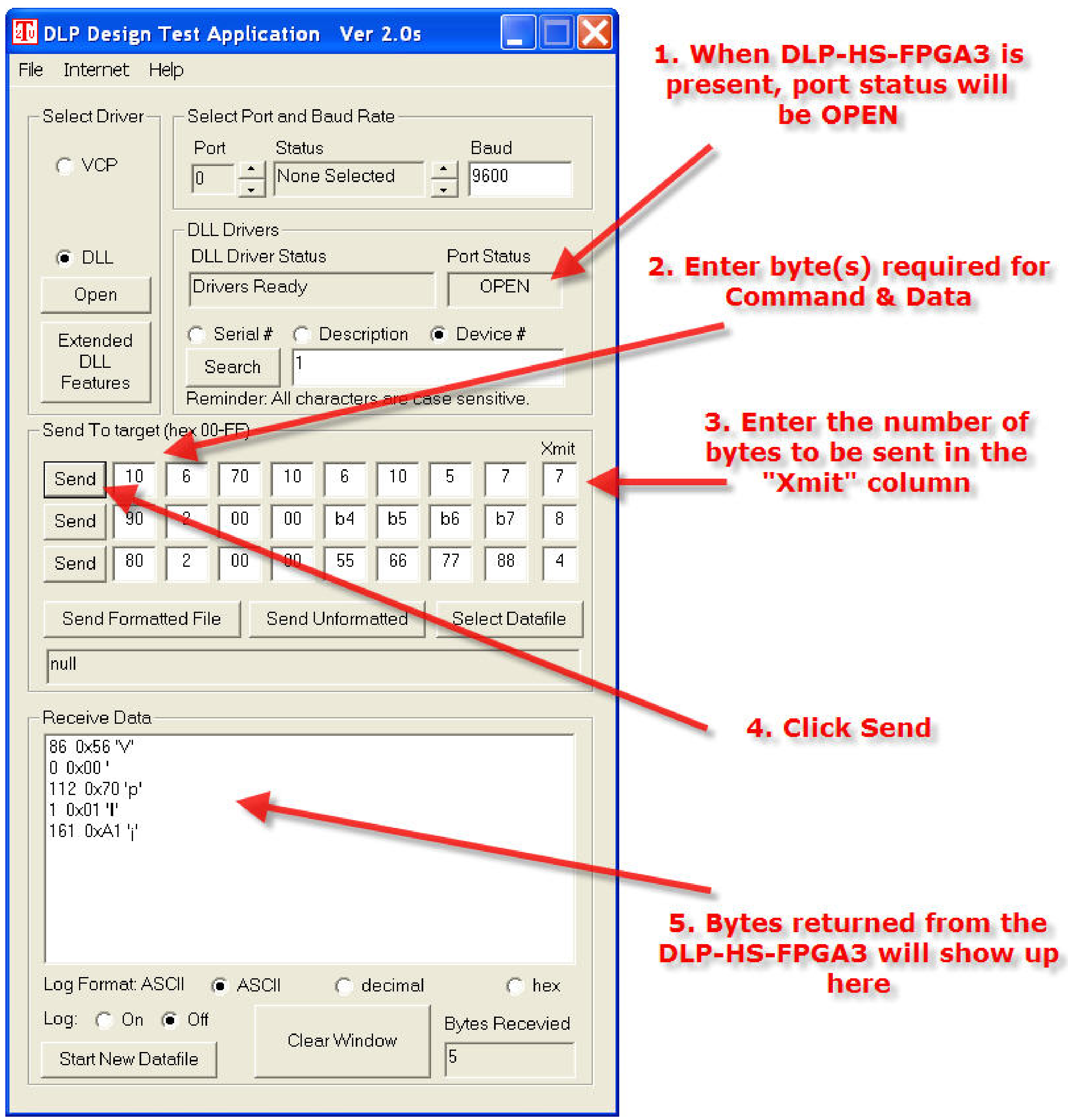
12.0 USING THE DLP TEST APPLICATION (OPTIONAL)

Users can design their own application interface to send USB commands to the DLP-HS-FPGA3 module or utilize the test application tool available from DLP Design. The DLP Test Application is available in a free version for download from the DLP Design website at **www.dlpdesign.com/ test.shtml**. Using this tool, single- and multi-byte commands can be sent to the DLP-HS-FPGA3 board.

Once installed the test application is used as follows:



The commands used to interface to the DLP-HS-FPGA3 are detailed in Section 11 of this datasheet.

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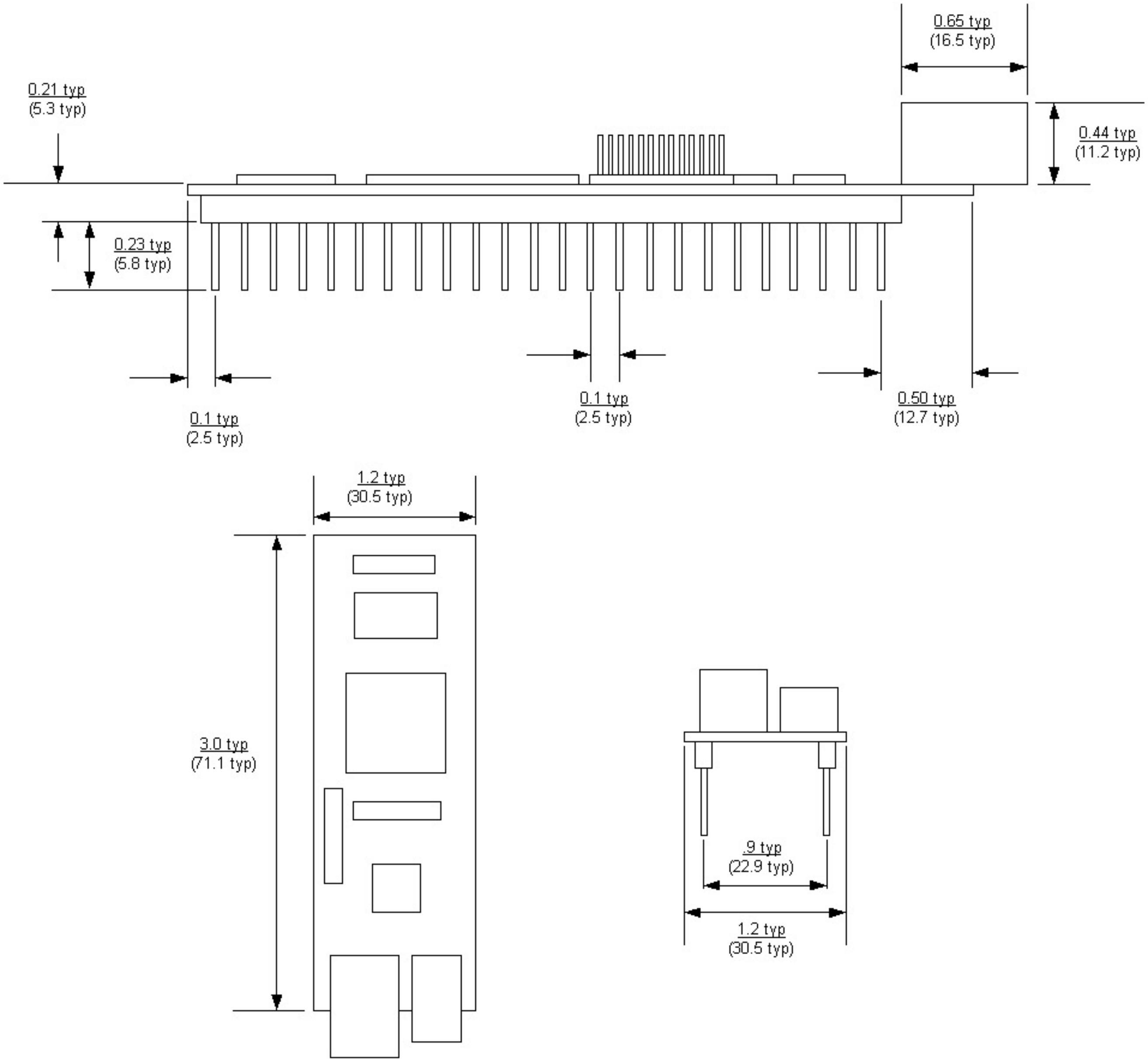
13.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



14.0 DISCLAIMER

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This document provides preliminary information that may be subject to change without notice.

15.0 CONTACT INFORMATION

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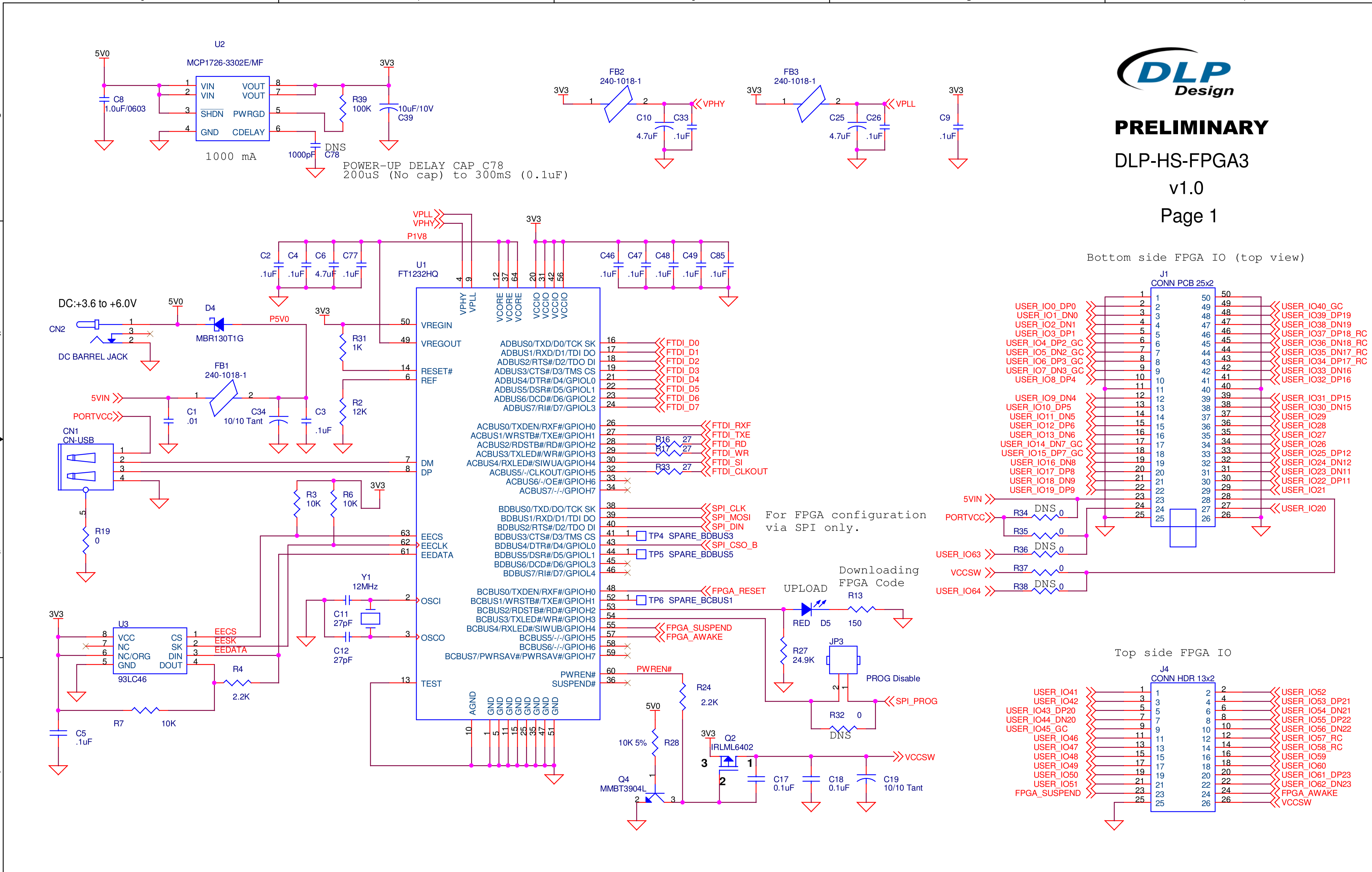
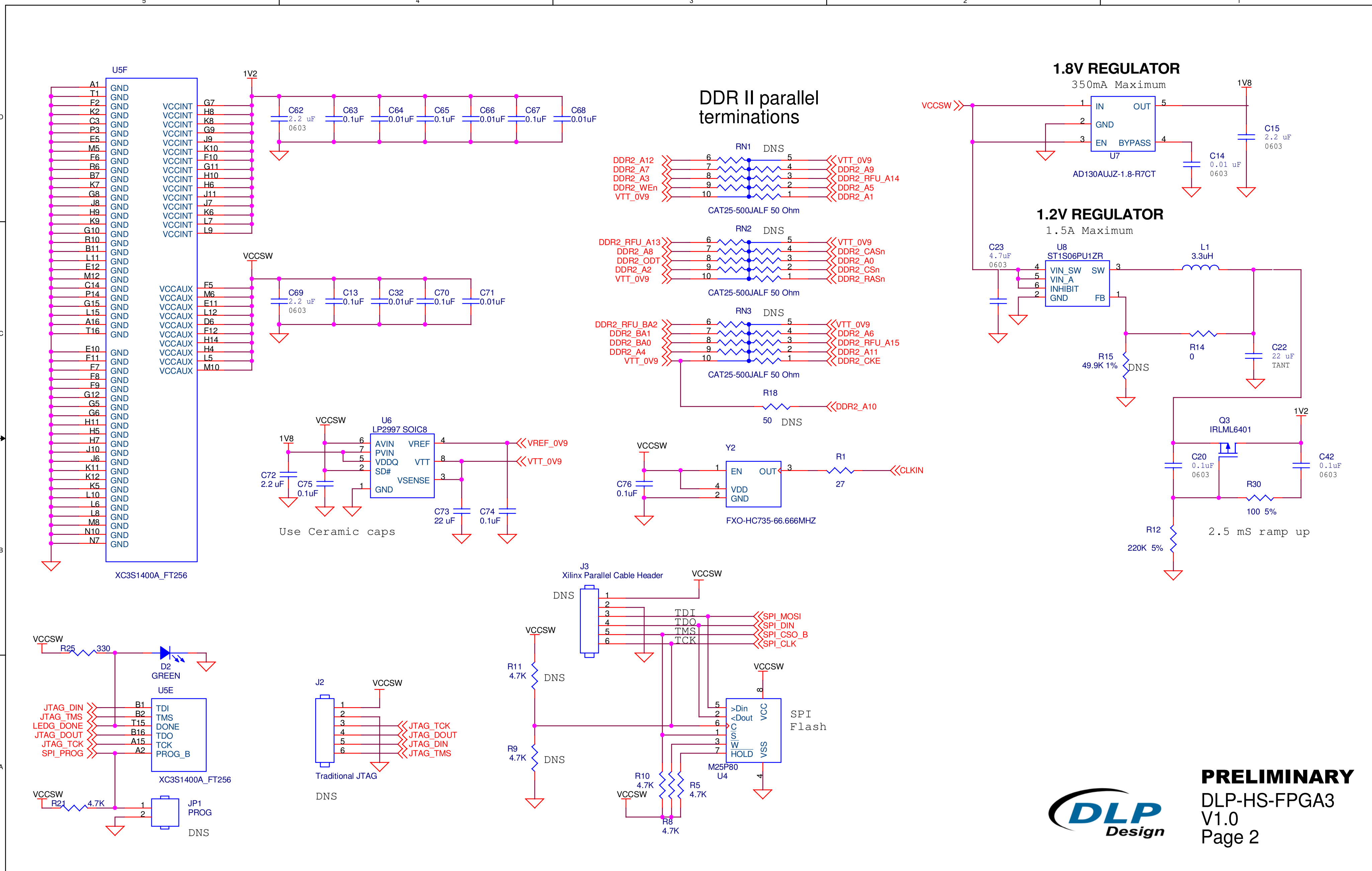

PRELIMINARY
DLP-HS-FPGA3
v1.0
Page 1
DLP Design
DC:+3.6 to +6.0V
1000 mA
POWER-UP DELAY CAP C78
200uS (No cap) to 300mS (0.1uF)
For FPGA configuration
via SPI only.
UPLOAD
Downloading
FPGA Code
PROG Disable
Bottom side FPGA IO (top view)
Top side FPGA IO
U1
FT1232HQ
U2
MCP1726-3302E/MF
U3
93LC46
J1
CONN PCB 25x2
J4
CONN HDR 13x2
CN1
CN-USB
CN2
DC BARREL JACK
Y1
12MHz
Q2
IRLML6402
Q4
MMBT3904L
D4
MBR130T1G



1.8V REGULATOR
350mA Maximum
U7
AD130AUZ-1.8-R7CT
1.2V REGULATOR
1.5A Maximum
U8
ST1S06PU1ZR
DDR II parallel terminations
RN1 DNS
RN2 DNS
RN3 DNS
CAT25-500JALF 50 Ohm
U5F
XC3S1400A_FT256
U5E
XC3S1400A_FT256
U6
LP2997 SOIC8
Use Ceramic caps
Y2
FXO-HC735-66.666MHZ
Q3
IRLML6401
2.5 mS ramp up
J3
Xilinx Parallel Cable Header
J2
Traditional JTAG
DNS
U4
M25P80
SPI Flash
JP1
PROG
DNS
D2
GREEN
VCCSW
1V2
1V8
CLKIN
VREF_0V9
VTT_0V9
SPI_MOSI
SPI_DIN
SPI_CSO_B
SPI_CLK
JTAG_DIN
JTAG_TMS
LEDG_DONE
JTAG_DOUT
JTAG_TCK
SPI_PROG
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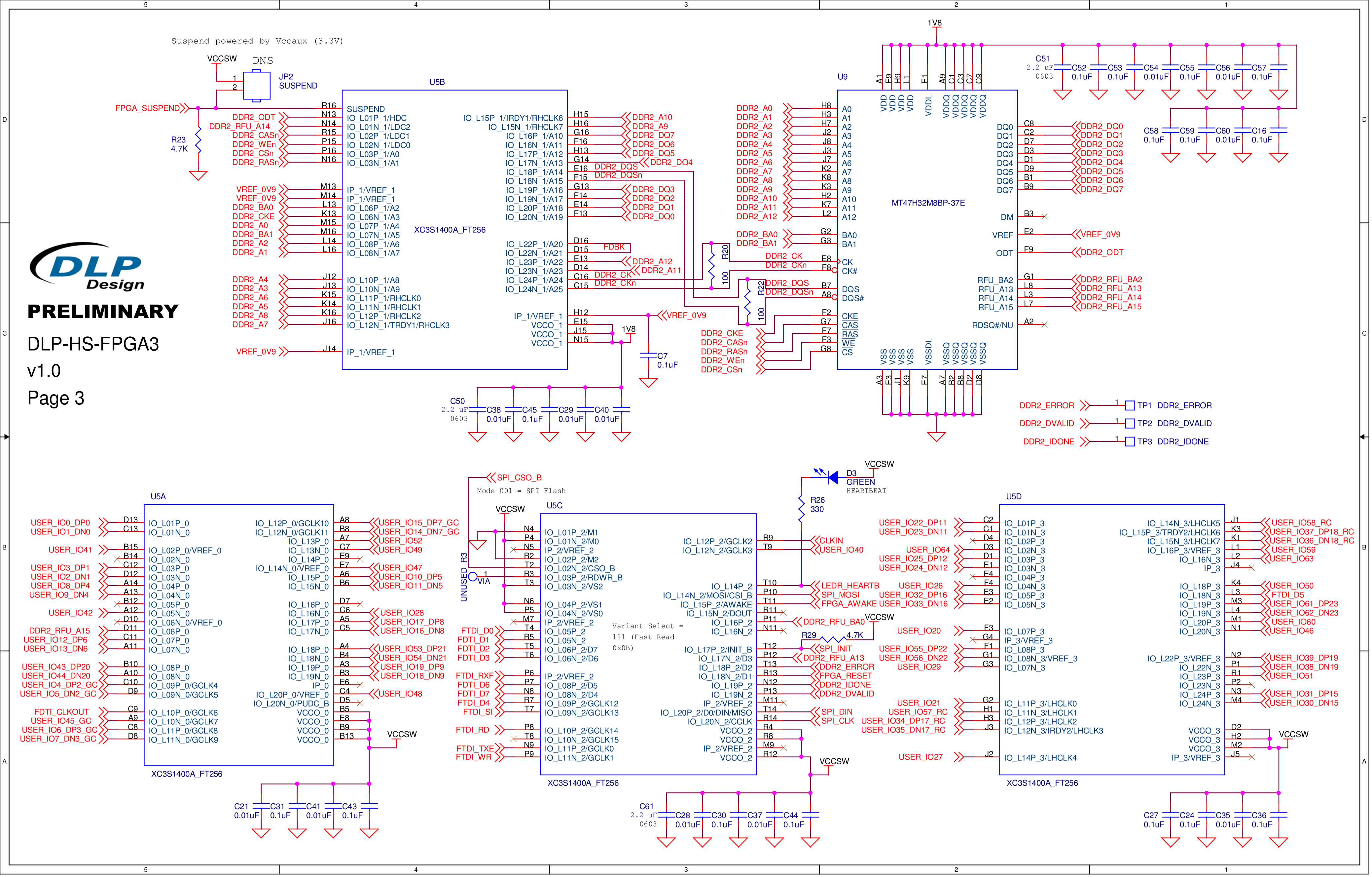
PRELIMINARY
DLP-HS-FPGA3
v1.0
Page 3
Suspend powered by Vccaux (3.3V)
DNS
JP2 SUSPEND
FPGA_SUSPEND
R23 4.7K
U5B
XC3S1400A_FT256
U9
MT47H32M8BP-37E
U5A
XC3S1400A_FT256
U5C
XC3S1400A_FT256
U5D
XC3S1400A_FT256
Mode 001 = SPI Flash
Variant Select = 111 (Fast Read 0x0B)
UNUSED R3
VIA
D3 GREEN HEARTBEAT
R26 330
R29 4.7K
R20 100
R22 100
TP1 DDR2_ERROR
TP2 DDR2_DVALID
TP3 DDR2_IDONE
VCCSW
1V8
VREF_0V9
SPI_CSO_B