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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

| | |
|---------------------------------|---|
| Product Status | Active |
| Programmable Type | In System Programmable (min 1K program/erase cycles) |
| Delay Time tpd(1) Max | 7 ns |
| Voltage Supply - Internal | 2.7V ~ 3.6V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | 1500 |
| Number of I/O | 40 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-FBGA, CSPBGA |
| Supplier Device Package | 48-CSBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcr3064xl-7cs48i |

Features

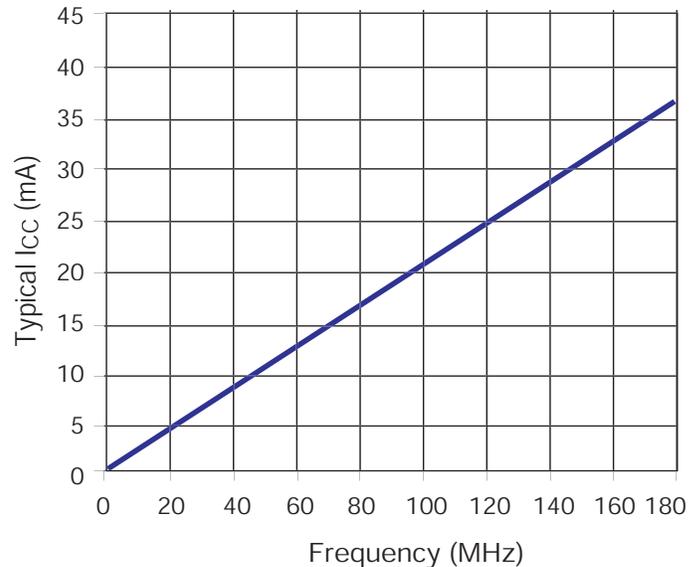
- Low power 3.3V 64 macrocell CPLD
- 5.5 ns pin-to-pin logic delays
- System frequencies up to 192 MHz
- 64 macrocells with 1,500 usable gates
- Available in small footprint packages
 - 44-pin VQFP (36 user I/O pins)
 - 48-ball CS BGA (40 user I/O pins)
 - 56-ball CP BGA (48 user I/O pins)
 - 100-pin VQFP (68 user I/O pins)
- Optimized for 3.3V systems
 - Ultra-low power operation
 - Typical Standby Current of 17 μ A at 25°C
 - 5V tolerant I/O pins with 3.3V core supply
 - Advanced 0.35 micron five layer metal EEPROM process
 - Fast Zero Power CMOS design technology
 - 3.3V PCI electrical specification compatible outputs (no internal clamp diode on any input or I/O, no minimum clock input capacitance)
- Advanced system features
 - In-system programming
 - Input registers
 - Predictable timing model
 - Up to 23 available clocks per function block
 - Excellent pin retention during design changes
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
 - Four global clocks
 - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V supply voltage at industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet ([DS012](#)) for architecture description

Description

The CoolRunner™ XPLA3 XCR3064XL device is a 3.3V, 64-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four function blocks provide 1,500 usable gates. Pin-to-pin propagation delays are as fast as 5.5 ns with a maximum system frequency of 192 MHz.

TotalCMOS Design Technique for Fast Zero Power

CoolRunner XPLA3 CPLDs offer a TotalCMOS solution, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to [Figure 1](#) and [Table 1](#) showing the I_{CC} vs. Frequency of our XCR3064XL TotalCMOS CPLD (data taken with four resettable up/down, 16-bit counters at 3.3V, 25°C).



DS017_01_062502

Figure 1: I_{CC} vs. Frequency at $V_{CC} = 3.3V, 25^{\circ}C$

Table 1: I_{CC} vs. Frequency ($V_{CC} = 3.3V, 25^{\circ}C$)

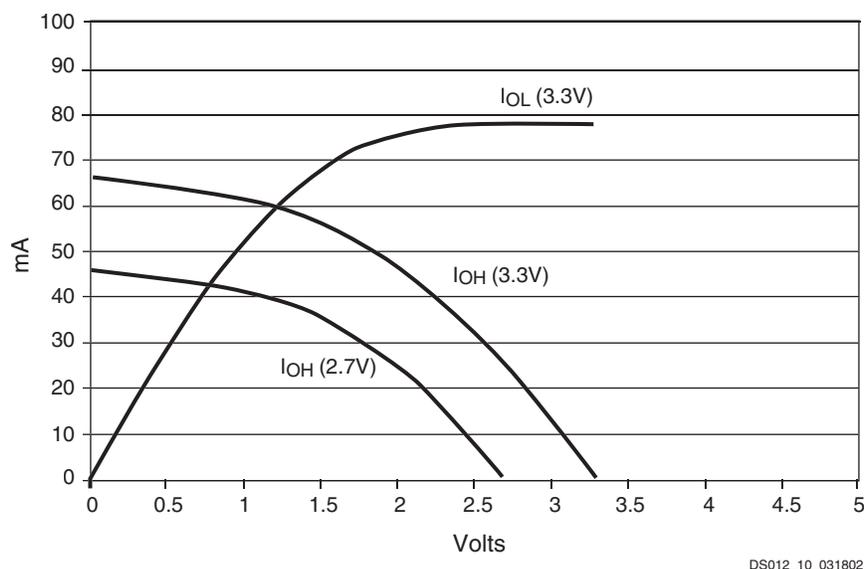
| Frequency (MHz) | 0 | 1 | 5 | 10 | 20 | 40 | 60 | 80 | 100 | 120 | 140 | 160 | 180 |
|-----------------------|-------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|
| Typical I_{CC} (mA) | 0.017 | 0.24 | 1.09 | 2.15 | 4.28 | 8.50 | 12.85 | 16.80 | 20.80 | 25.72 | 29.89 | 33.53 | 36.27 |

DC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter ⁽¹⁾ | Test Conditions | Typical | Min. | Max. | Unit |
|------------------|--|--|---------|--------------------|------|---------|
| $V_{OH}^{(2)}$ | Output High voltage | $V_{CC} = 3.0V$ to $3.6V$, $I_{OH} = -8$ mA | - | 2.4 | - | V |
| | | $V_{CC} = 2.7V$ to $3.0V$, $I_{OH} = -8$ mA | - | 2.0 | - | V |
| | | $I_{OH} = -500$ μA | - | 90% $V_{CC}^{(3)}$ | - | V |
| V_{OL} | Output Low voltage for 3.3V outputs | $I_{OL} = 8$ mA | - | - | 0.4 | V |
| $I_{IL}^{(4)}$ | Input leakage current | $V_{IN} = GND$ or V_{CC} to 5.5V | - | -10 | 10 | μA |
| $I_{IH}^{(4)}$ | I/O High-Z leakage current | $V_{IN} = GND$ or V_{CC} to 5.5V | - | -10 | 10 | μA |
| $I_{CCSB}^{(8)}$ | Standby current | $V_{CC} = 3.6V$ | 24.5 | - | 100 | μA |
| I_{CC} | Dynamic current ^(5,6) | $f = 1$ MHz | - | - | 0.75 | mA |
| | | $f = 50$ MHz | - | - | 15 | mA |
| C_{IN} | Input pin capacitance ⁽⁷⁾ | $f = 1$ MHz | - | - | 8 | pF |
| C_{CLK} | Clock input capacitance ⁽⁷⁾ | $f = 1$ MHz | - | - | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance ⁽⁷⁾ | $f = 1$ MHz | - | - | 10 | pF |

Notes:

1. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
2. See [Figure 2](#) for output drive characteristics of the XPLA3 family.
3. This parameter guaranteed by design and characterization, not by testing.
4. Typical leakage current is less than 1 μA .
5. See [Table 1](#), and [Figure 1](#) for typical values.
6. This parameter measured with a 16-bit, resettable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
7. Typical values, not tested.
8. Typical value at 70°C.



DS012_10_031802

Figure 2: Typical I/V Curve for the CoolRunner XPLA3 Family, 25°C

AC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter ^(1,2) | -6 | | -7 | | -10 | | Unit |
|------------------------------------|---|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| T _{PD1} | Propagation delay time (single p-term) | - | 5.5 | - | 7.0 | - | 9.1 | ns |
| T _{PD2} | Propagation delay time (OR array) ⁽³⁾ | - | 6.0 | - | 7.5 | - | 10.0 | ns |
| T _{CO} | Clock to output (global synchronous pin clock) | - | 4.0 | - | 5.0 | - | 6.5 | ns |
| T _{SUF} | Setup time (fast input register) | 2.5 | - | 2.5 | - | 3.0 | - | ns |
| T _{SU1} ⁽⁴⁾ | Setup time (single p-term) | 3.5 | - | 4.3 | - | 5.4 | - | ns |
| T _{SU2} | Setup time (OR array) | 4.0 | - | 4.8 | - | 6.3 | - | ns |
| T _H ⁽⁴⁾ | Hold time | 0 | - | 0 | - | 0 | - | ns |
| T _{WLH} ⁽⁴⁾ | Global Clock pulse width (High or Low) | 2.5 | - | 3.0 | - | 4.0 | - | ns |
| T _{PLH} ⁽⁴⁾ | P-term clock pulse width | 4.0 | - | 5.0 | - | 6.0 | - | ns |
| T _{APRPW} | Asynchronous preset/reset pulse width (High or Low) | 4.0 | - | 5.0 | - | 6.0 | - | ns |
| T _R ⁽⁴⁾ | Input rise time | - | 20 | - | 20 | - | 20 | ns |
| T _L ⁽⁴⁾ | Input fall time | - | 20 | - | 20 | - | 20 | ns |
| f _{SYSTEM} ⁽⁴⁾ | Maximum system frequency | - | 192 | - | 119 | - | 95 | MHz |
| T _{CONFIG} ⁽⁴⁾ | Configuration time ⁽⁵⁾ | - | 60 | - | 60 | - | 60 | μs |
| T _{INIT} ⁽⁴⁾ | ISP initialization time | - | 60 | - | 60 | - | 60 | μs |
| T _{POE} ⁽⁴⁾ | P-term OE to output enabled | - | 7.5 | - | 9.3 | - | 11.2 | ns |
| T _{POD} ⁽⁴⁾ | P-term OE to output disabled ⁽⁶⁾ | - | 7.5 | - | 9.3 | - | 11.2 | ns |
| T _{PCO} ⁽⁴⁾ | P-term clock to output | - | 7.0 | - | 8.3 | - | 10.7 | ns |
| T _{PAO} ⁽⁴⁾ | P-term set/reset to output valid | - | 8.0 | - | 9.3 | - | 11.2 | ns |

Notes:

1. Specifications measured with one output switching.
2. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
3. See [Figure 4](#) for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 6 mA at 3.6V.
6. Output C_L = 5 pF.

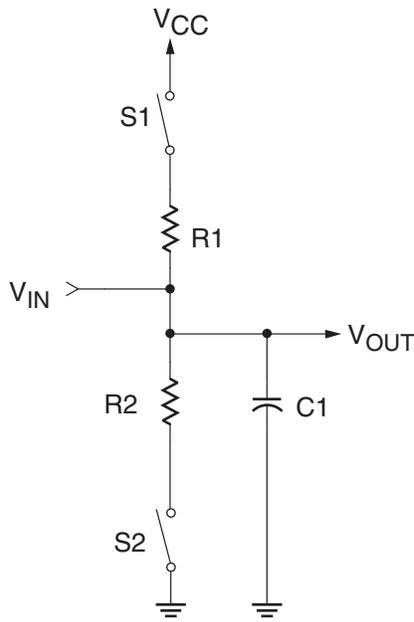
Internal Timing Parameters

| Symbol | Parameter ^(1, 2) | -6 | | -7 | | -10 | | Unit |
|---|--------------------------------------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Buffer Delays | | | | | | | | |
| T _{IN} | Input buffer delay | - | 1.3 | - | 1.6 | - | 2.2 | ns |
| T _{FIN} | Fast Input buffer delay | - | 2.3 | - | 3.0 | - | 3.1 | ns |
| T _{GCK} | Global Clock buffer delay | - | 0.8 | - | 1.0 | - | 1.3 | ns |
| T _{OUT} | Output buffer delay | - | 2.2 | - | 2.7 | - | 3.6 | ns |
| T _{EN} | Output buffer enable/disable delay | - | 4.2 | - | 5.0 | - | 5.7 | ns |
| Internal Register and Combinatorial Delays | | | | | | | | |
| T _{LDI} | Latch transparent delay | - | 1.3 | - | 1.6 | - | 2.0 | |
| T _{SUI} | Register setup time | 1.0 | - | 1.0 | - | 1.2 | - | ns |
| T _{HI} | Register hold time | 0.3 | - | 0.5 | - | 0.7 | - | ns |
| T _{ECSU} | Register clock enable setup time | 2.0 | - | 2.5 | - | 3.0 | - | ns |
| T _{ECHO} | Register clock enable hold time | 3.0 | - | 4.5 | - | 5.5 | - | ns |
| T _{COI} | Register clock to output delay | - | 1.0 | - | 1.3 | - | 1.6 | ns |
| T _{AOI} | Register async. S/R to output delay | - | 2.5 | - | 2.3 | - | 2.1 | ns |
| T _{RAI} | Register async. recovery | - | 4.0 | - | 5.0 | - | 6.0 | ns |
| T _{PTCK} | Product term clock delay | - | 2.5 | - | 2.7 | - | 3.3 | ns |
| T _{LOGI1} | Internal logic delay (single p-term) | - | 2.0 | - | 2.7 | - | 3.3 | ns |
| T _{LOGI2} | Internal logic delay (PLA OR term) | - | 2.5 | - | 3.2 | - | 4.2 | ns |
| Feedback Delays | | | | | | | | |
| T _F | ZIA delay | - | 0.7 | - | 2.9 | - | 3.5 | ns |
| Time Adders | | | | | | | | |
| T _{LOGI3} | Fold-back NAND delay | - | 2.0 | - | 2.5 | - | 3.0 | ns |
| T _{UDA} | Universal delay | - | 1.5 | - | 2.0 | - | 2.5 | ns |
| T _{SLEW} | Slew rate limited delay | - | 4.0 | - | 5.0 | - | 6.0 | ns |

Notes:

1. These parameters guaranteed by design and/or characterization, not testing.
2. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for timing model.

Switching Characteristics



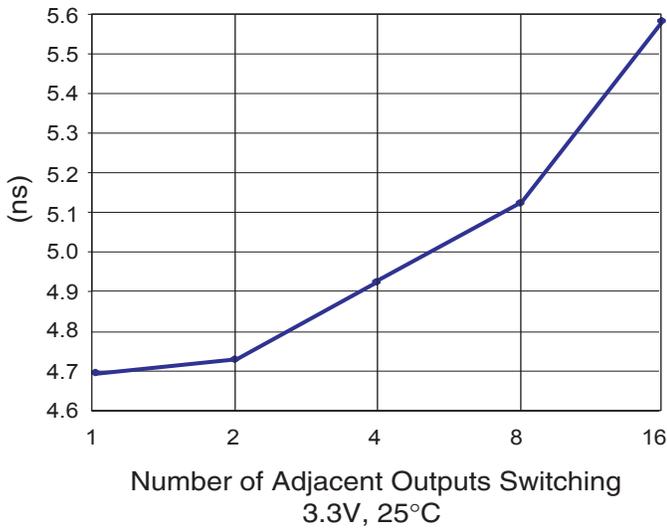
| Component | Values |
|-----------|--------|
| R1 | 390Ω |
| R2 | 390Ω |
| C1 | 35 pF |

| Measurement | S1 | S2 |
|-------------------------|--------|--------|
| T _{POE} (High) | Open | Closed |
| T _{POE} (Low) | Closed | Open |
| T _P | Closed | Closed |

Note: For T_{POD}, C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} - 300 mV.

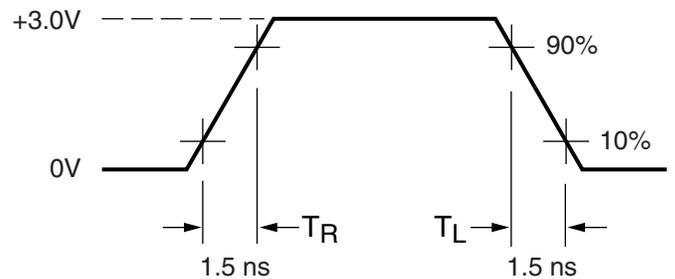
DS017_03_102401

Figure 3: AC Load Circuit



DS017_04_062502

Figure 4: Derating Curve for T_{PD2}, 3.3V, 25°C



Measurements:

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: Voltage Waveform

Pin Descriptions

Table 2: XCR3064XL User I/O Pins

| | PC44 ⁽¹⁾ | VQ44 | CS48 | CP56 | VQ100 |
|---------------------|---------------------|------|------|------|-------|
| Total User I/O Pins | 36 | 36 | 40 | 48 | 68 |

1. This is an obsolete package type. It remains here for legacy support only

Table 3: XCR3064XL I/O Pins

| Function Block | Macro-cell | PC44 ⁽¹⁾ | VQ44 | CS48 | CP56 | VQ100 |
|----------------|------------|---------------------|-------------------|-------------------|--------------------|-------------------|
| 1 | 1 | 41 | 35 | C5 | C8 | 85 |
| 1 | 2 | 40 | 34 | A6 | A8 | 84 |
| 1 | 3 | - | - | - | - | 83 |
| 1 | 4 | - | - | - | A9 | 81 |
| 1 | 5 | - | - | - | A5 | 80 |
| 1 | 6 | - | - | A7 | A10 | 79 |
| 1 | 7 | - | - | - | - | 76 |
| 1 | 8 | 39 | 33 | B6 | B10 | 75 |
| 1 | 9 | 38 ⁽²⁾ | 32 ⁽²⁾ | B7 ⁽²⁾ | C10 ⁽²⁾ | 73 ⁽²⁾ |
| 1 | 10 | 37 | 31 | D4 | D8 | 71 |
| 1 | 11 | 36 | 30 | C6 | E8 | 69 |
| 1 | 12 | - | - | - | - | 68 |
| 1 | 13 | - | - | - | - | 67 |
| 1 | 14 | 34 | 28 | D6 | F8 | 65 |
| 1 | 15 | 33 | 27 | D7 | E10 | 64 |
| 1 | 16 | - | - | - | - | 63 |
| 2 | 1 | 4 | 42 | A2 | C4 | 92 |
| 2 | 2 | 5 | 43 | A1 | C3 | 93 |
| 2 | 3 | 6 | 44 | C4 | A1 | 94 |
| 2 | 4 | - | - | - | - | 96 |
| 2 | 5 | - | - | - | B1 | 97 |
| 2 | 6 | - | - | - | - | 98 |
| 2 | 7 | - | - | - | A2 | 99 |
| 2 | 8 | - | - | B2 | A3 | 100 |
| 2 | 9 | 7 ⁽²⁾ | 1 ⁽²⁾ | B1 ⁽²⁾ | C1 ⁽²⁾ | 4 ⁽²⁾ |
| 2 | 10 | 8 | 2 | C2 | D1 | 6 |
| 2 | 11 | 9 | 3 | C1 | D3 | 8 |
| 2 | 12 | - | - | - | - | 9 |
| 2 | 13 | - | - | - | - | 10 |

Table 3: XCR3064XL I/O Pins

| Function Block | Macro-cell | PC44 ⁽¹⁾ | VQ44 | CS48 | CP56 | VQ100 |
|----------------|------------|---------------------|-------------------|-------------------|--------------------|-------------------|
| 2 | 14 | 11 | 5 | D3 | E3 | 12 |
| 2 | 15 | 12 | 6 | D1 | F1 | 13 |
| 2 | 16 | - | - | - | - | 14 |
| 3 | 1 | 32 ⁽²⁾ | 26 ⁽²⁾ | E5 ⁽²⁾ | F10 ⁽²⁾ | 62 ⁽²⁾ |
| 3 | 2 | 31 | 25 | E7 | G8 | 61 |
| 3 | 3 | - | - | - | - | 60 |
| 3 | 4 | 29 | 23 | F7 | H10 | 58 |
| 3 | 5 | - | - | - | - | 57 |
| 3 | 6 | - | - | - | - | 56 |
| 3 | 7 | - | - | F6 | K8 | 54 |
| 3 | 8 | - | - | - | K10 | 52 |
| 3 | 9 | 28 | 22 | G7 | K9 | 48 |
| 3 | 10 | 27 | 21 | G6 | J10 | 47 |
| 3 | 11 | 26 | 20 | F5 | H8 | 46 |
| 3 | 12 | 25 | 19 | G5 | H7 | 45 |
| 3 | 13 | 24 | 18 | F4 | H6 | 44 |
| 3 | 14 | - | - | - | - | 42 |
| 3 | 15 | - | - | - | K7 | 41 |
| 3 | 16 | - | - | - | - | 40 |
| 4 | 1 | 13 ⁽²⁾ | 7 ⁽²⁾ | D2 ⁽²⁾ | G1 ⁽²⁾ | 15 ⁽²⁾ |
| 4 | 2 | 14 | 8 | E1 | F3 | 16 |
| 4 | 3 | - | - | - | - | 17 |
| 4 | 4 | 16 | 10 | F1 | G3 | 19 |
| 4 | 5 | 17 | 11 | G1 | J1 | 20 |
| 4 | 6 | - | - | - | - | 21 |
| 4 | 7 | - | - | - | - | 23 |
| 4 | 8 | - | - | - | K1 | 25 |
| 4 | 9 | 18 | 12 | E4 | K4 | 29 |
| 4 | 10 | 19 | 13 | F2 | K2 | 30 |
| 4 | 11 | 20 | 14 | G2 | K3 | 31 |
| 4 | 12 | 21 | 15 | F3 | H3 | 32 |
| 4 | 13 | - | - | G3 | H4 | 33 |
| 4 | 14 | - | - | - | - | 35 |
| 4 | 15 | - | - | - | K5 | 36 |
| 4 | 16 | - | - | - | - | 37 |

Notes:

1. This is an obsolete package type. It remains here for legacy support only.
2. JTAG pins.

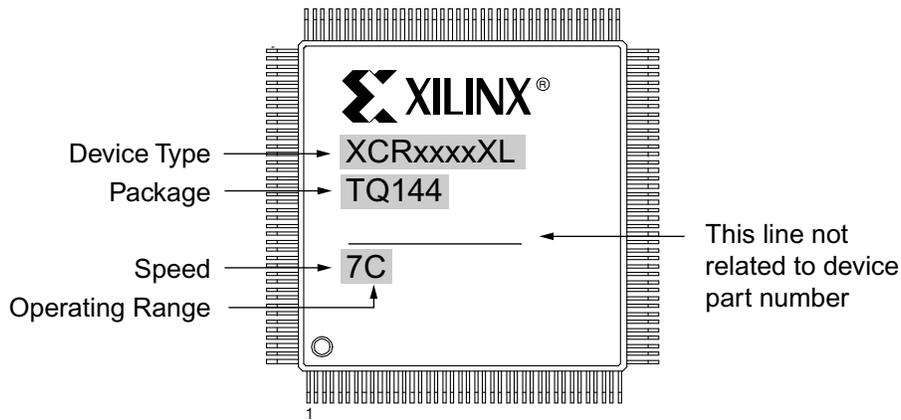
Table 4: XCR3064XL Global, JTAG, Port Enable, Power, and No Connect Pins

| Pin Type | PC44 ⁽¹⁾ | VQ44 | CS48 | CP56 | VQ100 |
|-----------------|---------------------|------------------|-------------------|-------------------|--|
| IN0 / CLK0 | 2 | 40 | A3 | C5 | 90 |
| IN1 / CLK1 | 1 | 39 | B4 | C6 | 89 |
| IN2 / CLK2 | 44 | 38 | A4 | C7 | 88 |
| IN3 / CLK3 | 43 | 37 | B5 | A6 | 87 |
| TCK | 32 | 26 | E5 | F10 | 62 |
| TDI | 7 | 1 | B1 | C1 | 4 |
| TDO | 38 | 32 | B7 | C10 | 73 |
| TMS | 13 | 7 | D2 | G1 | 15 |
| PORT_EN | 10 ⁽²⁾ | 4 ⁽²⁾ | C3 ⁽²⁾ | E1 ⁽²⁾ | 11 ⁽²⁾ |
| V _{CC} | 3, 15, 23, 35 | 9, 17, 29, 41 | B3, C7, E2, G4 | A4, D10, H1, H5 | 3, 18, 34, 39, 51, 66, 82, 91 |
| GND | 22, 30, 42 | 16, 24, 36 | A5, E3, E6 | A7, G10, K6 | 26, 38, 43, 59, 74, 86, 95 |
| No Connects | - | - | - | - | 1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78 |

Notes:

1. This is an obsolete package type. It remains here for legacy support only.
2. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet ([DS012](#)) for more information.

Device Part Marking



Sample package with part marking.

Notes:

1. Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
 - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 3064XL.
 - Line 2 = Not related to device part number.
 - Line 3 = Not related to device part number.
 - Line 4 = Package code, speed, operating temperature, three digits not related to device part number. Package codes: C1 = CS48, C2 = CSG48, C3 = CP56, C4 = CPG56.

Ordering Combination Information

| Device Ordering and Part Marking Number | Speed (pin-to-pin delay) | Pkg. Symbol | No. of Pins | Package Type | Operating Range ⁽¹⁾ |
|---|--------------------------|-------------|-------------|---|--------------------------------|
| XCR3064XL-6VQ44C | 6 ns | VQ44 | 44 | Very Thin Quad Flat Pack (VQFP) | C |
| XCR3064XL-6VQG44C | 6 ns | VQG44 | 44 | Very Thin Quad Flat Pack (VQFP); Pb-Free | C |
| XCR3064XL-6CS48C | 6 ns | CS48 | 48 | Chip Scale Package (CSP) | C |
| XCR3064XL-6CSG48C | 6 ns | CSG48 | 48 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-6CP56C | 6 ns | CP56 | 56 | Chip Scale Package (CSP) | C |
| XCR3064XL-6CPG56C | 6 ns | CPG56 | 56 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-6VQ100C | 6 ns | VQ100 | 100 | Very Thin Quad Flat Package (VQFP) | C |
| XCR3064XL-6VQG100C | 6 ns | VQG100 | 100 | Very Thin Quad Flat Package (VQFP); Pb-Free | C |
| XCR3064XL-7VQ44C | 7.5 ns | VQ44 | 44 | Very Thin Quad Flat Pack (VQFP) | C |
| XCR3064XL-7VQG44C | 7.5 ns | VQG44 | 44 | Very Thin Quad Flat Pack (VQFP); Pb-Free | C |
| XCR3064XL-7CS48C | 7.5 ns | CS48 | 48 | Chip Scale Package (CSP) | C |
| XCR3064XL-7CSG48C | 7.5 ns | CSG48 | 48 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-7CP56C | 7.5 ns | CP56 | 56 | Chip Scale Package (CSP) | C |
| XCR3064XL-7CPG56C | 7.5 ns | CPG56 | 56 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-7VQ100C | 7.5 ns | VQ100 | 100 | Very Thin Quad Flat Package (VQFP) | C |
| XCR3064XL-7VQG100C | 7.5 ns | VQG100 | 100 | Very Thin Quad Flat Package (VQFP); Pb-Free | C |
| XCR3064XL-7VQ44I | 7.5 ns | VQ44 | 44 | Very Thin Quad Flat Pack (VQFP) | I |
| XCR3064XL-7VQG44I | 7.5 ns | VQG44 | 44 | Very Thin Quad Flat Pack (VQFP); Pb-Free | I |
| XCR3064XL-7CS48I | 7.5 ns | CS48 | 48 | Chip Scale Package (CSP) | I |
| XCR3064XL-7CSG48I | 7.5 ns | CSG48 | 48 | Chip Scale Package (CSP); Pb-Free | I |
| XCR3064XL-7CP56I | 7.5 ns | CP56 | 56 | Chip Scale Package (CSP) | I |
| XCR3064XL-7CPG56I | 7.5 ns | CPG56 | 56 | Chip Scale Package (CSP); Pb-Free | I |
| XCR3064XL-7VQ100I | 7.5 ns | VQ100 | 100 | Very Thin Quad Flat Package (VQFP) | I |
| XCR3064XL-7VQG100I | 7.5 ns | VQG100 | 100 | Very Thin Quad Flat Package (VQFP); Pb-Free | I |
| XCR3064XL-10VQ44C | 10 ns | VQ44 | 44 | Very Thin Quad Flat Pack (VQFP) | C |
| XCR3064XL-10VQG44C | 10 ns | VQG44 | 44 | Very Thin Quad Flat Pack (VQFP); Pb-Free | C |
| XCR3064XL-10CS48C | 10 ns | CS48 | 48 | Chip Scale Package (CSP) | C |
| XCR3064XL-10CSG48C | 10 ns | CSG48 | 48 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-10CP56C | 10 ns | CP56 | 56 | Chip Scale Package (CSP) | C |
| XCR3064XL-10CPG56C | 10 ns | CPG56 | 56 | Chip Scale Package (CSP); Pb-Free | C |
| XCR3064XL-10VQ100C | 10 ns | VQ100 | 100 | Very Thin Quad Flat Package (VQFP) | C |
| XCR3064XL-10VQG100C | 10 ns | VQG100 | 100 | Very Thin Quad Flat Package (VQFP); Pb-Free | C |
| XCR3064XL-10VQ44I | 10 ns | VQ44 | 44 | Very Thin Quad Flat Pack (VQFP) | I |
| XCR3064XL-10VQG44I | 10 ns | VQG44 | 44 | Very Thin Quad Flat Pack (VQFP); Pb-Free | I |
| XCR3064XL-10CS48I | 10 ns | CS48 | 48 | Chip Scale Package (CSP) | I |
| XCR3064XL-10CSG48I | 10 ns | CSG48 | 48 | Chip Scale Package (CSP); Pb-Free | I |
| XCR3064XL-10CP56I | 10 ns | CP56 | 56 | Chip Scale Package (CSP) | I |

Ordering Combination Information (Continued)

| Device Ordering and Part Marking Number | Speed (pin-to-pin delay) | Pkg. Symbol | No. of Pins | Package Type | Operating Range ⁽¹⁾ |
|---|--------------------------|-------------|-------------|---|--------------------------------|
| XCR3064XL-10CPG56I | 10 ns | CPG56 | 56 | Chip Scale Package (CSP); Pb-Free | I |
| XCR3064XL-10VQ100I | 10 ns | VQ100 | 100 | Very Thin Quad Flat Package (VQFP) | I |
| XCR3064XL-10VQG100I | 10 ns | VQG100 | 100 | Very Thin Quad Flat Package (VQFP); Pb-Free | I |

Notes:

1. C = Commercial: $T_A = 0^\circ$ to $+70^\circ\text{C}$; I = Industrial: $T_A = -40^\circ$ to $+85^\circ\text{C}$

Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT <http://www.xilinx.com/warranty.htm>. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Additional Information

[CoolRunner XPLA3 CPLD Data Sheets and Application Notes](#)

[Device Packages](#)

[Device Package User Guide](#)

Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|--|
| 06/01/00 | 1.0 | Initial Xilinx release. |
| 08/30/00 | 1.1 | Added 48-ball CS BGA package. |
| 11/18/00 | 1.2 | Updated to full production data sheet; corrected note in Table 4 to read: "port enable pin is brought High". |
| 12/08/00 | 1.3 | Added PC44 package. |
| 04/11/01 | 1.4 | Added Typical I/V curve, Figure 2 ; added Table 2 : Total User I/O; changed V_{OH} spec. |
| 04/19/01 | 1.5 | Updated Typical I/V curve, Figure 2 : added voltage levels. |
| 01/08/02 | 1.6 | Moved I_{CC} vs. Freq Figure 1 and Table 1 to page 1. Added single p-term setup time (T_{SU1}) to AC Table, renamed T_{SU} to T_{SU2} for setup time through the OR array. Updated T_{SUF} and T_{FIN} spec to match software timing. Added T_{INIT} spec. Updated T_{CONFIG} spec. Updated T_{HI} spec to correct a typo. Updated AC Load Circuit diagram to more closely resemble true test conditions, added note for T_{POD} delay measurement. Updated note 5 in AC Characteristics table lowering typical current draw during configuration. |
| 04/02/02 | 1.7 | Updated the following specs based on characterization of product after move to UMC fabrication: V_{OH} , F_{SYSTEM} , T_{PCO} (added T_{PTCK} parameter), T_F and T_{LOGI3} . Added typical leakage current note to DC table. Also updated Typical I_{CC} vs. Frequency and Derating Curve for T_{PD2} (improved to 5.4 ns for 16 outputs switching) per new characterization data. |
| 01/27/03 | 1.8 | Corrected typical I_{CC} vs. Frequency (Figure 1) and Derating Curve for T_{PD2} (Figure 4). Updated F_{MAX} for -6 speed, I_{CC} @ f=1 MHz based on characterization of product after move to UMC fabrication. Updated Ordering Information format. |
| 07/15/03 | 1.9 | Updated Device Part Marking. Updated test conditions for I_{IL} and I_{IH} . |
| 08/21/03 | 2.0 | Updated Package Device Marking Pin 1 orientation. |
| 02/13/04 | 2.1 | Add soldering temperature. Add links to application notes and data sheets and packages. |
| 04/08/05 | 2.2 | Added I_{CCSB} Typical and T_{APRPW} specifications. Removed T_{SOL} specification. |
| 03/31/06 | 2.3 | Added Warranty Disclaimer. Added Pb-Free information to ordering table. |
| 09/15/08 | 2.4 | Added notes to Table 2 , Table 3 and Table 4 to indicate the PC44 package is obsolete. Removed part number references to the obsolete PC44C and PCG44C packages in the Ordering Combination Information . See Product Discontinuation Notice xcn07022.pdf . |