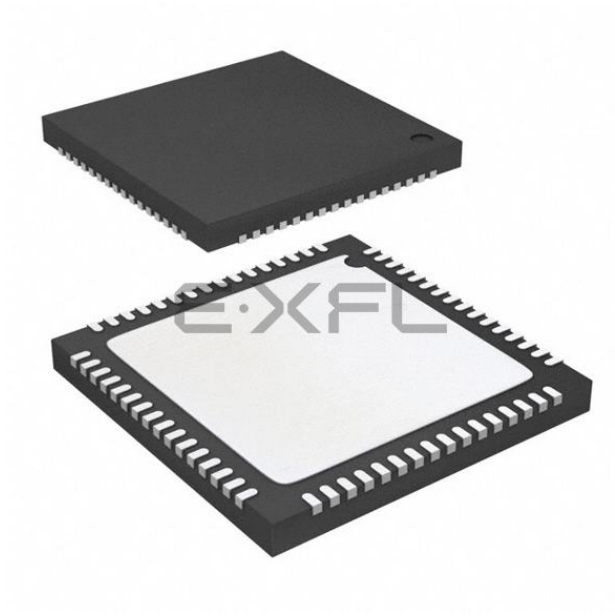

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PLA, POR, PWM, PSM, Temp Sensor, WDT
Number of I/O	28
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7128bcpz126

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 3.0 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz. All specifications T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity[3]		±0.7	±2.0	LSB	2.5 V internal reference 85°C to 125°C only
		±0.7	±1.5	LSB	2.5 V internal reference −40°C to +85°C
		±2.0		LSB	1.0 V external reference
Differential Nonlinearity[3]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		±0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[4]					
Offset Error			±5	LSB	
Offset Error Match		±1		LSB	
Gain Error			±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					F_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	
Crosstalk Between Channel 12 and Channel 13		−60		dB	
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode[5]			$V_{CM} \pm V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current			±15	µA	85°C to 125°C only
		±1	±3	µA	−40°C to +85°C
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±2.5	mV	Measured at T_A = 25°C
Reference Drop When DAC Enabled		9		mV	Reference drop when DAC enabled
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		80		dB	
Output Impedance		40		Ω	
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT[6]					
Input Voltage Range	0.625		AV_{DD}	V	
Input Impedance		38		kΩ	
DAC CHANNEL SPECIFICATIONS					
VDAC Output					R_L = 5 kΩ, C_L = 100 pF
Voltage Swing		$(0.33 \times V_{REF} \pm 0.2 \times V_{REF}) \times 1.33$			V_{REF} is the internal 2.5 V reference
I/V Output Resistance			7	Ω	V mode selected
Low-Pass Filter 3 dB Point		1		MHz	2-pole at 1.5 MHz and 2 MHz
Resolution		10		Bits	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Relative Accuracy		±2		LSB	
Differential Nonlinearity, +VE		0.35		LSB	
Differential Nonlinearity, −VE		−0.15		LSB	
Offset Error			−190	mV	
Gain Error			+150	mV	
Voltage Output Settling Time to 0.1%			5	µs	
Line Driver Output					As measured into a range of specified loads (see Figure 2) at LD1TX and LD2TX, unless otherwise noted
Total Harmonic Distortion		−52		dB	PLM operating at 691.2 kHz
Output Voltage Swing		±1.768		V rms	
COMMON MODE					
AC Mode		1.65		V	Each output has a common mode of 0.5 V × AV_{DD} and swings 0.5 V × V_{REF} above and below this; V_{REF} is the internal 2.5 V reference
DC Mode		1.5		V	Each output has a common mode of 0.5 V × V_{REF} and swings 0.6 V × V_{REF} above and below this; V_{REF} is the internal 2.5 V reference
DIFFERENTIAL INPUT IMPEDANCE	11	13		kΩ	Line driver buffer disabled
Leakage Current LD1TX, LD2TX			7	µA	Line driver buffer disabled
Short-Circuit Current		±50		mA	No protection diodes, max allowable current
Line Driver Tx Power-Up Time			20	µs	
COMPARATOR					
Input Offset Voltage		±15		mV	
Input Bias Current		1		µA	
Input Voltage Range	AGND		AV_{DD} − 1.2 V		
Input Capacitance		7		pF	
Hysteresis[3, 5]	2		15	mV	Hysteresis can be turned on or off via the CMPHYST bit in the CMPCON register
Response Time		1		µs	Response time can be modified via the CMPRES bits in the CMPCON register
TEMPERATURE SENSOR					
Voltage Output at 25°C		780		mV	
Voltage Temperature Coefficient		−1.3		mV/°C	
Accuracy		±3		°C	
POWER SUPPLY MONITOR (PSM)					
IOV_{DD} Trip Point Selection		2.79		V	Two selectable trip points
		3.07		V	
Power Supply Trip Point Accuracy		±2.5		%	Of the selected nominal trip point voltage
GLITCH IMMUNITY ON $\overline{RST}$ PIN[3]		50		µs	
WATCHDOG TIMER (WDT)					
Timeout Period	0			ms	
			512	sec	
FLASH/EE MEMORY[7, 8]					
Endurance	10,000			Cycles	
Data Retention	20			Years	T_J = 85°C
DIGITAL INPUTS					All digital inputs, including XCLKI and XCLKO
Logic 1 Input Current (Leakage Current)		±0.2	±1	µA	$V_{INH} = V_{DD}$ or V_{INH} = 5 V
Logic 0 Input Current (Leakage Current)		−40	−65	µA	V_{INL} = 0 V, except TDI
		−80	+125	µA	V_{INL} = 0 V, TDI Only
Input Capacitance		15		pF	

Table 6. SPI Master Mode Timing (PHASE Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			2 × t_{HCLK} + 2 × t_{UCLK}	ns
t_{DOSU}	Data output setup before SCLOCK edge			75	ns
t_{DSU}	Data input setup time before SCLOCK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLOCK rise time		5	12.5	ns
t_{SF}	SCLOCK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the PLLCON MMR, $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

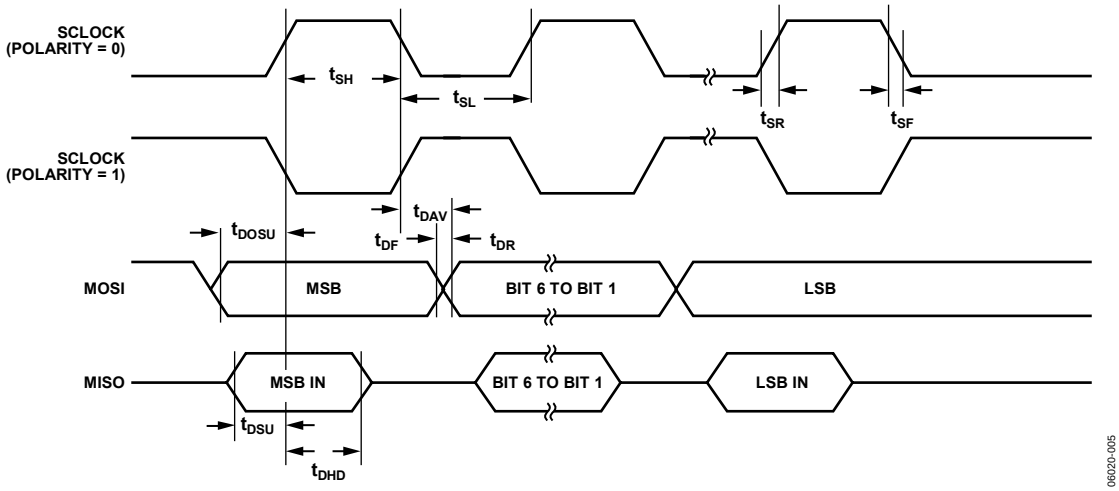

Figure 7. SPI Master Mode Timing (PHASE Mode = 0)

Pin No.	Mnemonic	Type[1]	Description
21	LV_{DD}	S	2.5 V Output of the On-Chip Voltage Regulator. Must be connected to a 0.47 µF capacitor to DGND.
22	DGND	S	Ground for Core Logic.
23	P3.0/PWM1	I/O	General-Purpose Input and Output Port 3.0/PWM1 Output.
24	P3.1/PWM2	I/O	General-Purpose Input and Output Port 3.1/PWM2 Output.
25	P3.2/PWM3	I/O	General-Purpose Input and Output Port 3.2/PWM3 Output.
26	P3.3/PWM4	I/O	General-Purpose Input and Output Port 3.3/PWM4 Output.
27	P0.3/ADC_{BUSY}/$\overline{TRST}$	I/O	General-Purpose Input and Output Port 3.3/ADC_{BUSY} Signal/JTAG Test Port Input, Test Reset. Debug and download access.
28	$\overline{RST}$	I	Reset Input (Active Low).
29	P3.4/PWM5	I/O	General-Purpose Input and Output Port 3.4/PWM5 Output.
30	P3.5/PWM6	I/O	General-Purpose Input and Output Port 3.5/PWM6 Output.
31	P0.4/IRQ0/$\overline{CONVST}$	I/O	General-Purpose Input and Output Port 0.5/External Interrupt Request 0, Active High/Start Conversion Input Signal for ADC.
32	P0.5/IRQ1/ADC_{BUSY}	I/O	General-Purpose Input and Output Port 0.6/External Interrupt Request 1, Active High/ADC_{BUSY} Signal.
33	P2.0/SPM9	I/O	General-Purpose Input and Output Port 2.0/Serial Port Mux Pin 9.
34	P0.7/SPM8/ECLK/XCLK	I/O	General-Purpose Input and Output Port 0.7/Serial Port Mux Pin 8/Output for the External Clock Signal/Input to the Internal Clock Generator Circuits.
35	XCLKO	O	Output from the Crystal Oscillator Inverter.
36	XCLKI	I	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
37	PV_{DD}	S	2.5 V PLL Supply. Must be connected to a 0.1 µF capacitor to DGND. Should be connected to 2.5 V LDO output.
38	DGND	S	Ground for PLL.
39	P1.7/SPM7	I/O	General-Purpose Input and Output Port 1.7/Serial Port Mux Pin 7.
40	P1.6/SPM6	I/O	General-Purpose Input and Output Port 1.6/Serial Port Mux Pin 6.
43	P4.0/S1	I/O	General-Purpose Input and Output Port 4.0/Quadrature Input 1.
44	P4.1/S2	I/O	General-Purpose Input and Output Port 4.1/Quadrature Input 2.
45	P1.5/SPM5	I/O	General-Purpose Input and Output Port 1.5/Serial Port Mux Pin 5.
46	P1.4/SPM4	I/O	General-Purpose Input and Output Port 1.4/Serial Port Mux Pin 4.
47	P1.3/SPM3	I/O	General-Purpose Input and Output Port 1.3/Serial Port Mux Pin 3.
48	P1.2/SPM2	I/O	General-Purpose Input and Output Port 1.2/Serial Port Mux Pin 2.
49	P1.1/SPM1	I/O	General-Purpose Input and Output Port 1.1/Serial Port Mux Pin 1.
50	P1.0/SPM0	I/O	General-Purpose Input and Output Port 1.0/Serial Port Mux Pin 0.
51	P4.2	I/O	General-Purpose Input and Output Port 4.2.
52	P4.3/ PWM_{TRIP}	I/O	General-Purpose Input and Output Port 4.3/PWM Safety Cutoff.
53	P4.4	I/O	General-Purpose Input and Output Port 4.4.
54	P4.5	I/O	General-Purpose Input and Output Port 4.5.
55	V_{REF}	I/O	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
56	DACGND	S	Ground for the DAC. Typically connected to AGND.
59	$DACV_{DD}$	S	Power Supply for the DAC. This must be supplied with 2.5 V. This can be connected to the LDO output.
60	ADC0	I	Single-Ended or Differential Analog Input 0.
61	ADC1	I	Single-Ended or Differential Analog Input 1.
62	ADC2/CMP0	I	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
63	ADC3/CMP1	I	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
64	ADC4	I	Single-Ended or Differential Analog Input 4.

[1] I = input, O = output, S = supply.

Pin No.	Mnemonic	Type[1]	Description
17	P4.6/SPM10/AD14	I/O	General-Purpose Input and Output Port 4.6/Serial Port Mux Pin 10/External Memory AD14.
18	P4.7/SPM11/AD15	I/O	General-Purpose Input and Output Port 4.7/Serial Port Mux Pin 11/External Memory AD15.
19	P0.0/$\overline{BM}$/CMP_{OUT}/MS0	I/O	General-Purpose Input and Output Port 0.0 /Boot Mode. The ADuC7129 enters download mode if $\overline{BM}$ is low at reset and executes code if $\overline{BM}$ is pulled high at reset through a 1 kΩ resistor/voltage comparator output/external memory MS0.
20	P0.6/T1/$\overline{MRST}$	O	General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/External Memory AE.
21	TCK	I	JTAG Test Port Input, Test Clock. Debug and download access.
22	TDO/P0.2/$\overline{BHE}$	O	JTAG Test Port Output, Test Data Out. Debug and download access/general-purpose input and output Port 0.2/External Memory $\overline{BHE}$.
23, 53, 67	IOGND	S	Ground for GPIO. Typically connected to DGND.
24, 54	IOV_{DD}	S	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
25	LV_{DD}	S	2.5 V Output of the On-Chip Voltage Regulator. Must be connected to a 0.47 µF capacitor to DGND.
26	DGND	S	Ground for Core Logic.
27	P3.0/PWM1/AD0	I/O	General-Purpose Input and Output Port 3.0/PWM1 Output/External Memory AD0.
28	P3.1/PWM2/AD1	I/O	General-Purpose Input and Output Port 3.1/PWM2 Output/External Memory AD1.
29	P3.2/PWM3/AD2	I/O	General-Purpose Input and Output Port 3.2/PWM3 Output/External Memory AD2.
30	P3.3/PWM4/AD3	I/O	General-Purpose Input and Output Port 3.3/PWM4 Output//External Memory AD3.
31	P2.4/MS0	I/O	General-Purpose Input and Output Port 2.4/Memory Select 0.
32	P0.3/ADC_{BUSY}/$\overline{TRST}$/A16	I/O	General-Purpose Input and Output Port 3.3/ADC_{BUSY} Signal/JTAG Test Port Input, Test Reset. Debug and download access/External Memory A16.
33	P2.5/MS1	I/O	General-Purpose Input and Output Port 2.5/Memory Select 1.
34	P2.6/MS2	I/O	General-Purpose Input and Output Port 2.6/Memory Select 2.
35	$\overline{RST}$	I	Reset Input (Active Low).
36	P3.4/PWM5/AD4	I/O	General-Purpose Input and Output Port 3.4/PWM5 Output/External Memory AD4.
37	P3.5/PWM6/AD5	I/O	General-Purpose Input and Output Port 3.5/PWM6 Output/External Memory AD5.
38	P0.4/IRQ0/$\overline{CONVST}$/MS1	I/O	General-Purpose Input and Output Port 0.5/External Interrupt Request 0, Active High/Start Conversion Input Signal for ADC/External Memory MS1.
39	P0.5/IRQ1/ADC_{BUSY}	I/O	General-Purpose Input and Output Port 0.6/External Interrupt Request 1, Active High/ADC_{BUSY} Signal.
40	P2.0/SPM9	I/O	General-Purpose Input and Output Port 2.0/Serial Port Mux Pin 9.
41	P0.7/SPM8/ECLK/XCLK	I/O	General-Purpose Input and Output Port 0.7/Serial Port Mux Pin 8/Output for the External Clock Signal/Input to the Internal Clock Generator Circuits.
42	XCLKO	O	Output from the Crystal Oscillator Inverter.
43	XCLKI	I	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
44	PV_{DD}	S	2.5 V PLL Supply. Must be connected to a 0.1 µF capacitor to DGND. Should be connected to 2.5 V LDO output.
45	DGND	S	Ground for PLL.
46	P3.6/AD6	I/O	General-Purpose Input and Output Port 3.6/External Memory AD6.
47	P3.7/AD7	I/O	General-Purpose Input and Output Port 3.7/External Memory AD7.
48	P2.7/MS3	I/O	General-Purpose Input and Output Port 2.7/Memory Select 3.
49	P2.1/$\overline{WS}$	I/O	General-Purpose Input and Output Port 2.1/Memory Write Select.
50	P2.2/$\overline{RS}$	I/O	General-Purpose Input and Output Port 2.1/Memory Read Select.
51	P1.7/SPM7	I/O	General-Purpose Input and Output Port 1.7/Serial Port Mux Pin 7.
52	P1.6/SPM6	I/O	General-Purpose Input and Output Port 1.6/Serial Port Mux Pin 6.
55	P4.0/S1/AD8	I/O	General-Purpose Input and Output Port 4.0/Quadrature Input 1/External Memory AD8.
56	P4.1/S2/AD9	I/O	General-Purpose Input and Output Port 4.1/Quadrature Input 2/External Memory AD9.
57	P1.5/SPM5	I/O	General-Purpose Input and Output Port 1.5/Serial Port Mux Pin 5.
58	P1.4/SPM4	I/O	General-Purpose Input and Output Port 1.4/Serial Port Mux Pin 4.
59	P1.3/SPM3	I/O	General-Purpose Input and Output Port 1.3/Serial Port Mux Pin 3.
60	P1.2/SPM2	I/O	General-Purpose Input and Output Port 1.2/Serial Port Mux Pin 2.
61	P1.1/SPM1	I/O	General-Purpose Input and Output Port 1.1/Serial Port Mux Pin 1.
62	P1.0/SPM0	I/O	General-Purpose Input and Output Port 1.0/Serial Port Mux Pin 0.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal to (*Noise* + *Distortion*) = (6.02 N + 1.76) dB

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes for the output to settle to within a 1 LSB level for a full-scale input change.

MEMORY ORGANIZATION

The ADuC7128/ADuC7129 incorporate three separate blocks of memory: 8 kB of SRAM and two 64 kB of on-chip Flash/EE memory. There are 126 kB of on-chip Flash/EE memory available to the user, and the remaining 2 kB are reserved for the factory-configured boot page. These two blocks are mapped as shown in Figure 29.

Note that by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE Memory section.

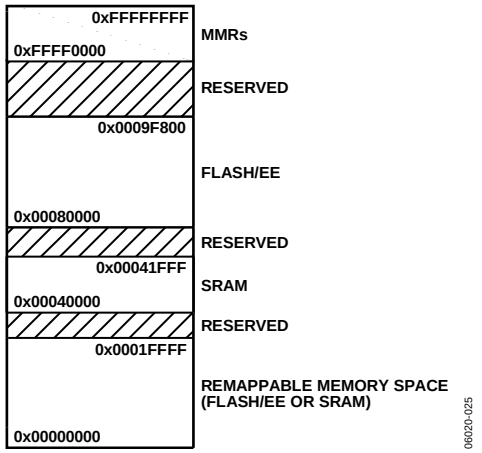

Figure 29. Physical Memory Map

MEMORY ACCESS

The ARM7 core sees memory as a linear array of 2^{32} byte locations where the different blocks of memory are mapped as outlined in Figure 29.

The ADuC7128/ADuC7129 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address.

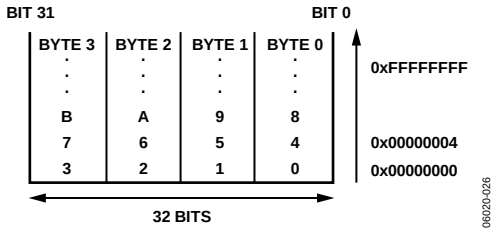

Figure 30. Little Endian Format

FLASH/EE MEMORY

The 128 kB of Flash/EE is organized as two banks of 32 k × 16 bits. In the first block, 31 k × 16 bits are user space and 1 k × 16 bits is reserved for the factory-configured boot page. The page size of this Flash/EE memory is 512 bytes.

The second 64 kB block is organized in a similar manner. It is arranged in 32 k × 16 bits. All of this is available as user space.

The 126 kB of Flash/EE is available to the user as code and nonvolatile data memory. There is no distinction between data and program as ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, meaning that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. Therefore, it is recommended that Thumb mode be used when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode (see the Execution Time from SRAM and FLASH/EE section).

SRAM

The 8 kB of SRAM are available to the user, organized as 2 k × 32 bits, that is, 2 k words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array (see the Execution Time from SRAM and FLASH/EE section).

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers except the core registers reside in the MMR area. All shaded locations shown in Figure 31 are unoccupied or reserved locations and should not be accessed by user software. See Table 12 through Table 31 for a full MMR memory map.

The access time reading or writing a MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: advanced high performance bus (AHB) used for system modules, and advanced peripheral bus (APB) used for lower performance peripherals. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7128/ADuC7129 are on the APB except the Flash/EE memory and the GPIOs.

FEE1DAT Register

Name	Address	Default Value	Access
FEE1DAT	0xFFFF0E8C	0xXXXX	R/W

FEE1DAT is a 16-bit data register.

FEE1ADR Register

Name	Address	Default Value	Access
FEE1ADR	0xFFFF0E90	0x0000	R/W

FEE1ADR is a 16-bit address register.

FEE1SGN Register

Name	Address	Default Value	Access
FEE1SGN	0xFFFF0E98	0xFFFFFF	R

FEE1SGN is a 24-bit code signature.

FEE1PRO Register

Name	Address	Default Value	Access
FEE1PRO	0xFFFF0E9C	0x00000000	R/W

FEE1PRO provides protection following subsequent reset MMR. It requires a software key (see Table 45).

FEE1HID Register

Name	Address	Default Value	Access
FEE1HID	0xFFFF0EA0	0xFFFFFFFF	R/W

FEE1HID provides immediate protection MMR. It does not require any software keys (see Table 45).

FEE0STA Register

Name	Address	Default Value	Access
FEE0STA	0xFFFF0E00	0x0000	R/W

FEE1STA Register

Name	Address	Default Value	Access
FEE1STA	0xFFFF0E80	0x0000	R/W

FEE0MOD Register

Name	Address	Default Value	Access
FEE0MOD	0xFFFF0E04	0x80	R/W

FEE1MOD Register

Name	Address	Default Value	Access
FEE1MOD	0xFFFF0E84	0x80	R/W

FEE0CON Register

Name	Address	Default Value	Access
FEE0CON	0xFFFF0E08	0x0000	R/W

FEE1CON Register

Name	Address	Default Value	Access
FEE1CON	0xFFFF0E88	0x0000	R/W

DDSFRQ Register

Name	Address	Default Value	Access
DDSFRQ	0xFFFF0694	0x00000000	R/W

Table 54. DDSFRQ MMR Bit Designations

Bit	Description
31:0	Frequency select word (FSW)

The DDS frequency is controlled via the DDSFRQ MMR. This MMR contains a 32-bit word (FSW) that controls the frequency according to the following formula:

$$Frequency = \frac{FSW \times 20.8896 \text{ MHz}}{2^{32}}$$

DDSPHS Register

Name	Address	Default Value	Access
DDSPHS	0xFFFF0698	0x00000000	R/W

Table 55. DDSPHS MMR Bit Designations

Bit	Description
31:12	Reserved
11:0	Phase

The DDS phase offset is controlled via the DDSPHS MMR. This MMR contains a 12-bit value that controls the phase of the DDS output according to the following formula:

$$Phase\ Offset = \frac{2 \times \pi \times Phase}{2^{12}}$$

POWER SUPPLY MONITOR

The power supply monitor on the ADuC7128/ADuC7129 indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register (see Table 56). If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is cleared immediately once CMP goes high. Note that if the interrupt generated is exited before CMP goes high (IOV_{DD} is above the trip point), no further interrupts are generated until CMP returns high. The user should ensure that code execution remains within the ISR until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to the low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

The PSM does not operate correctly when using JTAG debug. It should be disabled in JTAG debug mode.

COMPARATOR

The ADuC7128/ADuC7129 integrate an uncommitted voltage comparator. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or the internal reference. The output of the comparator can be configured to generate a system interrupt, can be routed directly to the programmable logic array, can start an ADC conversion, or can be on an external pin, CMP_{OUT}.

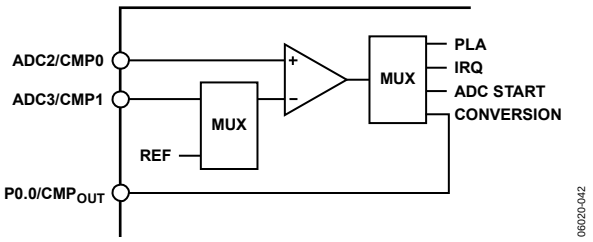

Figure 46. Comparator

Hysteresis

Figure 47 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

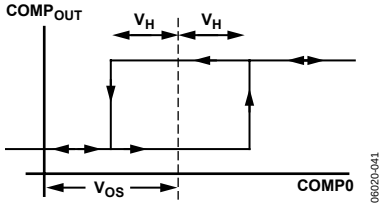

Figure 47. Comparator Hysteresis Transfer Function

Table 56. PSMCON MMR Bit Designations

Bit	Name	Description
3	CMP	Comparator Bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates the IOV_{DD} supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip Point Selection Bit. 0 = 2.79 V 1 = 3.07 V
1	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.
0	PSMI	Power Supply Monitor Interrupt Bit. This bit is set high by the MicroConverter if CMP is low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. Once CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A write of 0 has no effect. There is no timeout delay. PSMI can be cleared immediately once CMP goes high.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, described in Table 57.

Table 57. CMPCON MMR Bit Designations

Bit	Value	Name	Description
15:11			Reserved.
10		CMPEN	Comparator Enable Bit. Set by user to enable the comparator. Cleared by user to disable the comparator. Note: A comparator interrupt is generated on the enable of the comparator. This should be cleared in the user software.
9:8		CMPIN	Comparator Negative Input Select Bits.
	00		AVDD/2.
	01		ADC3 input.
	10		$V_{REF} \times 0.6$.
	11		Reserved.
7:6		CMPOC	Comparator Output Configuration Bits.
	00		IRQ and PLA connections disabled.
	01		IRQ and PLA connections disabled.
	10		PLA connections enabled.
	11		IRQ connections enabled.
5		CMPOL	Comparator Output Logic State Bit. When low, the comparator output is high when the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high when the positive input is below the negative input.
4:3		CMPRES	Response Time.
	00		5 µs response time typical for large signals (2.5 V differential). 17 µs response time typical for small signals (0.65 mV differential).
	01		Reserved.
	10		Reserved.
	11		3 µs response time typical for any signal type.
2		CMPHYST	Comparator Hysteresis Bit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1		CMPORI	Comparator Output Rising Edge Interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0		CMPOFI	Comparator Output Falling Edge Interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user.

GPxDAT Register

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W
GP3DAT	0xFFFF0D50	0x000000XX	R/W
GP4DAT	0xFFFF0D60	0x000000XX	R/W

GPxDAT is a Port x configuration and data register. It configures the direction of the GPIO pins of Port x, sets the output value for the pins configured as output, and receives and stores the input value of the pins configured as input.

Table 73. GPxDAT MMR Bit Designations

Bit	Description
31:24	Direction of the Data. Set to 1 by user to configure the GPIO pins as outputs. Cleared to 0 by user to configure the GPIO pins as inputs.
23:16	Port x Data Output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x Data Input (Read Only).

GPxSET Register

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W
GP3SET	0xFFFF0D54	0x000000XX	W
GP4SET	0xFFFF0D64	0x000000XX	W

GPxSET is a data set Port x register.

Table 74. GPxSET MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x Set Bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

GPxCLR Register

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W
GP3CLR	0xFFFF0D58	0x000000XX	W
GP4CLR	0xFFFF0D68	0x000000XX	W

GPxCLR is a data clear Port x register.

Table 75. GPxCLR MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x Clear Bit. Set to 1 by user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

SERIAL PORT MUX

The serial port mux multiplexes the serial port peripherals (two I^2Cs, an SPI, and two UARTs) and the programmable logic array (PLA) to a set of 10 GPIO pins. Each pin must be configured to its specific I/O function as described in Table 76.

Table 76. SPM Configuration

Pin	GPIO (00)	UART (01)	UART/I2C/SPI (10)	PLA (11)
SPM0	P1.0	SIN0	I2C0SCL	PLAI[0]
SPM1	P1.1	SOUT0	I2C0SDA	PLAI[1]
SPM2	P1.2	RTS0	I2C1SCL	PLAI[2]
SPM3	P1.3	CTS0	I2C1SDA	PLAI[3]
SPM4	P1.4	RI0	SPICLK	PLAI[4]
SPM5	P1.5	DCD0	SPIMISO	PLAI[5]
SPM6	P1.6	DSR0	SPIMOSI	PLAI[6]
SPM7	P1.7	DTR0	SPICSL	PLAO[0]
SPM8	P0.7	ECLK	SIN0	PLAO[4]
SPM9	P2.0[1]	PWMSYNC	SOUT0	PLAO[5]
SPM10	P2.2[1]	RTS1	RS	PLAO[7]
SPM11	P2.3[1]	CTS1	AE	
SPM12	P2.4[1]	RI1	MS0	
SPM13	P2.5[1]	DCD1	MS1	
SPM14	P2.6[1]	DSR1	MS2	
SPM15	P2.7[1]	DTR1	MS3	
SPM16	P4.6	SIN1	AD14	PLAO[14]
SPM17	P4.7	SOUT1	AD15	PLAO[15]

[1] Available only on the 80-lead ADuC7129.

Table 76 details the mode for each of the SPMUX GPIO pins. This configuration has to be performed via the GP0CON, GP1CON and GP2CON MMRs. By default these pins are configured as GPIOs.

UART SERIAL INTERFACE

The ADuC7128/ADuC7129 contain two identical UART blocks. Although only UART0 is described here, UART1 functions in exactly the same way.

The UART peripheral is a full-duplex universal asynchronous receiver/transmitter, fully compatible with the 16450 serial port standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The UART includes a fractional divider for baud rate generation and has a network-addressable mode. The UART function is made available on 10 pins of the ADuC7128/ADuC7129 (see Table 77).

Table 80. COMxCON0 MMR Bit Designations

Bit	Value	Name	Description
7		DLAB	Divisor Latch Access. Set by user to enable access to COMxDIV0 and COMxDIV1 registers. Cleared by user to disable access to COMxDIV0 and COMxDIV1 and enable access to COMxRX and COMxTX.
6		BRK	Set Break. Set by user to force SOUT to 0. Cleared to operate in normal mode.
5		SP	Stick Parity. Set by user to force parity to defined values. 1 if EPS = 1 and PEN = 1 0 if EPS = 0 and PEN = 1
4		EPS	Even Parity Select Bit. Set for even parity. Cleared for odd parity.
3		PEN	Parity Enable Bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2		STOP	Stop Bit. Set by user to transmit 1.5 stop bits if the word length is 5 bits or 2 stop bits if the word length is 6 bits, 7 bits, or 8 bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate 1 stop bit in the transmitted data.
1:0		WLS	Word Length Select.
	00		5 bits.
	01		6 bits.
	10		7 bits.
	11		8 bits.

Table 81. COMxSTA0 MMR Bit Designations

Bit	Name	Description
7	RSVD	Reserved.
6	TEMT	COMxTX Empty Status Bit. Set automatically if COMxTX is empty. Cleared automatically when writing to COMxTX.
5	THRE	COMxTX and COMxRX Empty. Set automatically if COMxTX and COMxRX are empty. Cleared automatically when one of the registers receives data.
4	BI	Break Error. Set when SIN is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing Error. Set when stop bit invalid. Cleared automatically.
2	PE	Parity Error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun Error. Set automatically if data is overwritten before it is read. Cleared automatically.
0	DR	Data Ready. Set automatically when COMxRX is full. Cleared by reading COMxRX.

I2CxSRX Register

Name	Address	Default Value	Access
I2C0SRX	0xFFFF0808	0x00	R
I2C1SRX	0xFFFF0908	0x00	R

I2CxSRX is a receive register for the slave channel.

I2CxSTX Register

Name	Address	Default Value	Access
I2C0STX	0xFFFF080C	0x00	W
I2C1STX	0xFFFF090C	0x00	W

I2CxSTX is a transmit register for the slave channel.

I2CxMRX Register

Name	Address	Default Value	Access
I2C0MRX	0xFFFF0810	0x00	R
I2C1MRX	0xFFFF0910	0x00	R

I2CxMRX is a receive register for the master channel.

I2CxMTX Register

Name	Address	Default Value	Access
I2C0MTX	0xFFFF0814	0x00	W
I2C1MTX	0xFFFF0914	0x00	W

I2CxMTX is a transmit register for the master channel.

I2CxCNT Register

Name	Address	Default Value	Access
I2C0CNT	0xFFFF0818	0x00	R/W
I2C1CNT	0xFFFF0918	0x00	R/W

I2CxCNT is a master receive data count register. If a master read transfer sequence is initiated, the I2CxCNT register denotes the number of bytes (−1) to be read from the slave device. By default this counter is 0, which corresponds to the expected one byte.

I2CxADR Register

Name	Address	Default Value	Access
I2C0ADR	0xFFFF081C	0x00	R/W
I2C1ADR	0xFFFF091C	0x00	R/W

I2CxADR is a master address byte register. The I2CxADR value is the device address that the master wants to communicate with. It is automatically transmitted at the start of a master transfer sequence if there is no valid data in the I2CxMTX register when the master enable bit is set.

I2CxBYT Register

Name	Address	Default Value	Access
I2C0BYT	0xFFFF0824	0x00	R/W
I2C1BYT	0xFFFF0924	0x00	R/W

I2CxBYT is a broadcast byte register.

I2CxALT Register

Name	Address	Default Value	Access
I2C0ALT	0xFFFF0828	0x00	R/W
I2C1ALT	0xFFFF0928	0x00	R/W

I2CxALT is a hardware general call ID register used in slave mode.

I2CxCFG Register

Name	Address	Default Value	Access
I2C0CFG	0xFFFF082C	0x00	R/W
I2C1CFG	0xFFFF092C	0x00	R/W

I2CxCFG is a configuration register.

Table 94. I2C0CFG MMR Bit Designations

Bit	Description
31:15	Reserved. These bits should be written by the user as 0.
14	Enable Stop Interrupt. Set by user to generate an interrupt upon receiving a stop condition and after receiving a valid start condition and matching address. Cleared by user to disable the generation of an interrupt upon receiving a stop condition.
13	Reserved. This bit should be written by the user as 0.
12	Reserved. This bit should be written by the user as 0.
11	Enable Stretch SCL. Holds SCL low. Set by user to stretch the SCL line. Cleared by user to disable stretching of the SCL line.
10	Reserved. This bit should be written by the user as 0.
9	Slave Tx FIFO Request Interrupt Enable. Cleared by user to generate an interrupt request just after the negative edge of the clock for the R/W bit. This allows the user to input data into the slave Tx FIFO if it is empty. At 400 kSPS, and with the core clock running at 41.78 MHz, the user has 45 clock cycles to take appropriate action, taking interrupt latency into account. Set by user to disable the slave Tx FIFO request interrupt.
8	General Call Status Bit Clear. Set by user to clear the general call status bits. Cleared automatically by hardware after the general call status bits have been cleared.

Bit	Description
7	Master Serial Clock Enable Bit. Set by user to enable generation of the serial clock in master mode. Cleared by user to disable serial clock in master mode.
6	Loop-Back Enable Bit. Set by user to internally connect the transition to the reception to test user software. Cleared by user to operate in normal mode.
5	Start Back-Off Disable Bit. Set by user in multimaster mode. If losing arbitration, the master immediately tries to retransmit. Cleared by user to enable start back-off. After losing arbitration, the master waits before trying to retransmit.
4	Hardware General Call Enable. When this bit and Bit 3 are set, and have received a general call (Address 0x00) and a data byte, the device checks the contents of the I2C0ALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7128/ADuC7129 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2C0ALT register should always be written to a 1, as per the I²C January 2000 specification.
3	General Call Enable Bit. Set this bit to enable the slave device to acknowledge an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of slave address by hardware) as the data byte, the I²C interface resets as per the I²C January 2000 specification. This command can be used to reset an entire I²C system. The general call interrupt status bit sets on any general call. The user must take corrective action by setting up the I²C interface after a reset. If it receives a 0x04 (write programmable part of slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
2	Reserved.
1	Master Enable Bit. Set by user to enable the master I²C channel. Cleared by user to disable the master I²C channel.
0	Slave Enable Bit. Set by user to enable the slave I²C channel. A slave transfer sequence is monitored for the device address in I2C0ID0, I2C0ID1, I2C0ID2, and I2C0ID3. If the device address is recognized, the part participates in the slave transfer sequence. Cleared by user to disable the slave I²C channel.

I2CxDIV Register

Name	Address	Default Value	Access
I2C0DIV	0xFFFF0830	0x1F1F	R/W
I2C1DIV	0xFFFF0930	0x1F1F	R/W

I2CxDIV are the clock divider registers.

I2CxIDx Register

Name	Address	Default Value	Access
I2C0ID0	0xFFFF0838	0x00	R/W
I2C0ID1	0xFFFF083C	0x00	R/W
I2C0ID2	0xFFFF0840	0x00	R/W
I2C0ID3	0xFFFF0844	0x00	R/W
I2C1ID0	0xFFFF0938	0x00	R/W
I2C1ID1	0xFFFF093C	0x00	R/W
I2C1ID2	0xFFFF0940	0x00	R/W
I2C1ID3	0xFFFF0944	0x00	R/W

I2CxID0, I2CxID1, I2CxID2, and I2CxID3 are slave address device ID registers of I2Cx.

I2CxSSC Register

Name	Address	Default Value	Access
I2C0SSC	0xFFFF0848	0x01	R/W
I2C1SSC	0xFFFF0948	0x01	R/W

I2CxSSC is an 8-bit start/stop generation counter. It holds off SDA low for start and stop conditions.

I2CxFIF Register

Name	Address	Default Value	Access
I2C0FIF	0xFFFF084C	0x0000	R
I2C1FIF	0xFFFF094C	0x0000	R

I2CxFIF is a FIFO status register.

Table 95. I2C0FIF MMR Bit Designations

Bit	Value	Description
15:10		Reserved.
9		Master Transmit FIFO Flush. Set by user to flush the master Tx FIFO. Cleared automatically once the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8		Slave Transmit FIFO Flush. Set by user to flush the slave Tx FIFO. Cleared automatically once the slave Tx FIFO is flushed.
7:6		Master Rx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
5:4		Master Tx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
3:2		Slave Rx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
1:0		Slave Tx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO full.

PROGRAMMABLE LOGIC ARRAY (PLA)

The ADuC7128/ADuC7129 integrate a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving a total of 16 PLA elements.

A PLA element contains a two input look-up table that can be configured to generate any logic output function based on two inputs and a flip-flop as represented in Figure 54.

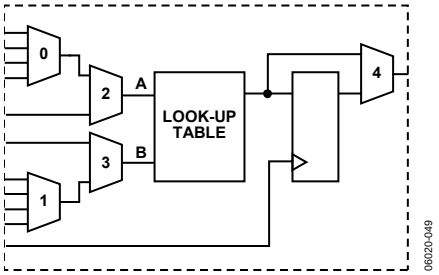

Figure 54. PLA Element

In total, 30 GPIO pins are available on the ADuC7128/ADuC7129 for the PLA. These include 16 input pins and 14 output pins. They need to be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs and the output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONVST}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The interconnection between the two blocks is supported by connecting the output of Element 7 of Block 1 fed back to the Input 0 of Mux 0 of Element 0 of Block 0, and the output of Element 7 of Block 0 is fed back to the Input 0 of Mux 0 of Element 0 of Block 1.

The Timer0 interface consists of six MMRs, shown in Table 108.

Table 108. Timer0 Interface MMRs

Name	Description
T0LD	A 16-bit register that holds the 16-bit value loaded into the counter. Available only in 16-bit mode.
T0CAP	A 16-bit register that holds the 16-bit value captured by an enabled IRQ event. Available only in 16-bit mode.
T0VAL0/ T0VAL1	TOVAL0 is a 16 bit register that holds the 16 least significant bits (LSBs). T0VAL1 is a 32-bit register that holds the 32 most significant bits (MSBs). T0VAL0 and T0VAL1 are read only. In 16-bit mode, 16-bit T0VAL0 is used. In 48-bit mode, both 16-bit T0VAL0 and 32-bit T0VAL1 are used.
T0ICLR	An 8-bit register. Writing any value to this register clears the interrupt. Available only in 16-bit mode.
T0CON	The configuration MMR (see Table 109).

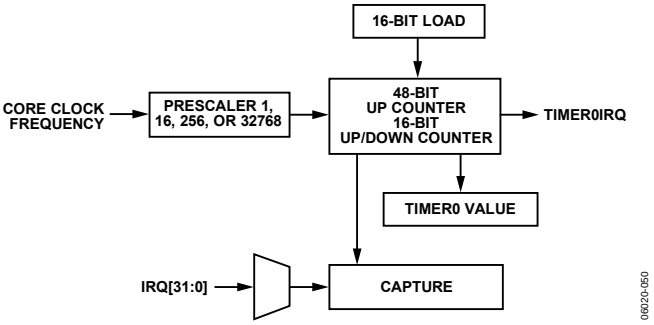

Figure 55. Timer0 Block Diagram

Timer0 Value Register

Name	Address	Default Value	Access
T0VAL0	0xFFFF0304	0x00	R
T0VAL1	0xFFFF0308	0x00	R

T0VAL0 and T0VAL1 are 16-bit and 32-bit registers that hold the 16 least significant bits and 32 most significant bits, respectively. T0VAL0 and T0VAL1 are read-only. In 16-bit mode, 16-bit T0VAL0 is used. In 48-bit mode, both 16-bit T0VAL0 and 32-bit T0VAL1 are used.

Timer0 Capture Register

Name	Address	Default Value	Access
T0CAP	0xFFFF0314	0x00	R

This is a 16-bit register that holds the 16-bit value captured by an enabled IRQ event; available only in 16-bit mode.

Timer0 Control Register

Name	Address	Default Value	Access
T0CON	0xFFFF030C	0x00	R/W

The 17-bit MMR configures the mode of operation of Timer0.

Table 109. T0CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved.
17		Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12		Event Select Range, 0 to 31. The events are as described in the Timers section.
11		Reserved.
10:9		Reserved.
8		Count Up. Available only in 16-bit mode. Set by user for timer 0 to count up. Cleared by user for timer 0 to count down (default).
7		Timer0 Enable Bit. Set by user to enable Timer0. Cleared by user to disable Timer0 (default).
6		Timer0 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5		Reserved.
4		Timer0 Mode of Operation.
	0	16-bit operation (default).
	1	48-bit operation.
3:0		Prescaler.
	0000	Source clock/1 (default).
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

Timer0 Load Register

Name	Address	Default Value	Access
T0LD	0xFFFF0300	0x00	R/W

T0LD is a 16-bit register that holds the 16-bit value that is loaded into the counter; available only in 16-bit mode.

Timer0 Clear Register

Name	Address	Default Value	Access
T0ICLR	0xFFFF0310	0x00	W

This 8-bit, write-only MMR is written (with any value) by user code to refresh (reload) Timer0.

Table 113. T2CON MMR Bit Designations

Bit	Value	Description
31:11		Reserved.
10:9		Clock Source Select.
	00	Core Clock (Default).
	01	Internal 32.768 kHz Oscillator.
	10	External 32.768 kHz Watch Crystal.
	11	External 32.768 kHz Watch Crystal.
8		Count Up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down (default).
7		Timer2 Enable Bit. Set by user to enable Timer2. Cleared by user to disable Timer2 (default).
6		Timer2 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256. This setting should be used in conjunction with Timer2 formats 1,0 and 1,1.
	1111	Source Clock/32,768.

TIMER4—GENERAL-PURPOSE TIMER

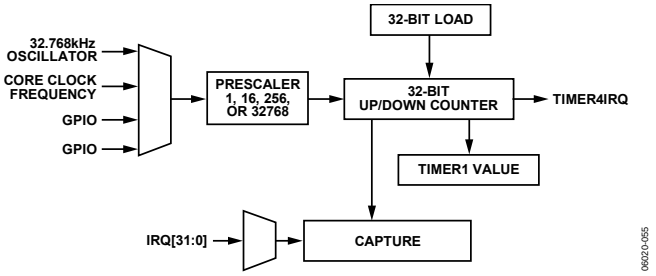

Figure 60. Timer4 Block Diagram

Timer4 is a 32-bit, general-purpose count down or count up timer with a programmable prescalar. The prescalar source can be the 32 kHz oscillator, the core clock, or one of two external GPIOs. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 42 ns when operating at CD zero, the core is operating at 41.78 MHz, and with a prescalar of 1 (ignoring external GPIO).

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer4 has a capture register (T4CAP), which can be triggered by a selected IRQ source initial assertion. Once triggered, the current timer value is copied to T4CAP, and the timer keeps running. This feature can be used to determine the assertion of an event with increased accuracy.

The Timer4 interface consists of five MMRs.

Table 116. Timer4 Interface MMRs

Name	Description
T4LD	A 32-bit register. Holds 32-bit unsigned integers.
T4VAL	A 32-bit register. Holds 32-bit unsigned integers. This register is read only.
T4CAP	A 32-bit register. Holds 32-bit unsigned integers. This register is read only.
T4ICLR	An 8-bit register. Writing any value to this register clears the Timer1 interrupt.
T4CON	The configuration MMR (see Table 117).

Note that if the part is in a low power mode and Timer4 is clocked from the GPIO or oscillator source, Timer4 continues to operate.

Timer4 reloads the value from T4LD either when Timer 4 overflows, or immediately when T4ICLR is written.

Timer4 Load Register

Name	Address	Default Value	Access
T4LD	0xFFFF0380	0x00000	R/W

T4LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer4 Clear Register

Name	Address	Default Value	Access
T4ICLR	0xFFFF038C	0x00	W

This 8-bit, write only MMR is written (with any value) by user code to refresh (reload) Timer4.

Timer4 Value Register

Name	Address	Default Value	Access
T4VAL	0xFFFF0384	0x0000	R

T4VAL is a 32-bit register that holds the current value of Timer4.

Timer4 Capture Register

Name	Address	Default Value	Access
T4CAP	0xFFFF0390	0x00	R

This is a 32-bit register that holds the 32-bit value captured by an enabled IRQ event.

Timer4 Control Register

Name	Address	Default Value	Access
T4CON	0xFFFF0388	0x0000	R/W

This 32-bit MMR configures the mode of operation of Timer4.

EXTERNAL MEMORY INTERFACING

The ADuC7129 is the only model in the series that features an external memory interface. The external memory interface requires a larger number of pins. This is why it is only available on larger pin count packages. The XMCFG MMR must be set to 1 to use the external port.

Although 32-bit addresses are supported internally, only the lower 16 bits of the address are on external pins.

The memory interface can address up to four 128 kB regions of asynchronous memory (SRAM and/or EEPROM).

The pins required for interfacing to an external memory are shown in Table 118.

Table 118. External Memory Interfacing Pins

Pin	Function
AD[15:0]	Address/Data Bus.
A16	Extended Addressing for 8-Bit Memory Only.
MS[3:0]	Memory Select.
WR ($\overline{WR}$)	Write Strobe.
RS ($\overline{RS}$)	Read Strobe.
AE	Address Latch Enable.
$\overline{BHE}$, $\overline{BLE}$	Byte Write Capability.

There are four external memory regions available, as described in Table 119. Associated with each region are the MS[3:0] pins. These signals allow access to the particular region of external memory. The size of each memory region can be 128 kB maximum, 64 k × 16, or 128 k × 8. To access 128 kB with an 8-bit memory, an extra address line (A16) is provided. (See the example in Figure 61). The four regions are configured independently.

Table 119. Memory Regions

Address Start	Address End	Contents
0x10000000	0x1000FFFF	External Memory 0
0x20000000	0x2000FFFF	External Memory 1
0x30000000	0x3000FFFF	External Memory 2
0x40000000	0x4000FFFF	External Memory 3

Each external memory region can be controlled through three MMRs: XMCFG, XMxCON, and XMxPAR.

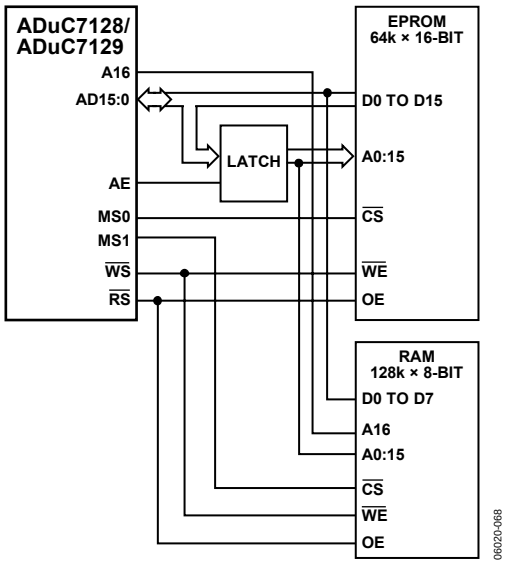

Figure 61. Interfacing to External EPROM/RAM

XMCFG Register

Name	Address	Default Value	Access
XMCFG	0xFFFFF000	0x00	R/W

XMCFG is set to 1 to enable external memory access. This must be set to 1 before any port pins function as external memory access pins. The port pins must also be individually enabled via the GPxCON MMR.

XMxCON Registers

Name	Address	Default Value	Access
XM0CON	0xFFFFF010	0x00	R/W
XM1CON	0xFFFFF014	0x00	R/W
XM2CON	0xFFFFF018	0x00	R/W
XM3CON	0xFFFFF01C	0x00	R/W

XMxCON registers are the control registers for each memory region. They allow the enabling/disabling of a memory region and control the data bus width of the memory region.

Table 120. XMxCON MMR Bit Designations

Bit	Description
1	Data Bus Width Select. Set by the user to select a 16-bit data bus. Cleared by the user to select an 8-bit data bus.
0	Memory Region Enable. Set by the user to enable memory region. Cleared by the user to disable the memory region.

XMxPAR Registers

Name	Address	Default Value	Access
XM0PAR	0xFFFFF020	0x70FF	R/W
XM1PAR	0xFFFFF024	0x70FF	R/W
XM2PAR	0xFFFFF028	0x70FF	R/W
XM3PAR	0xFFFFF02C	0x70FF	R/W

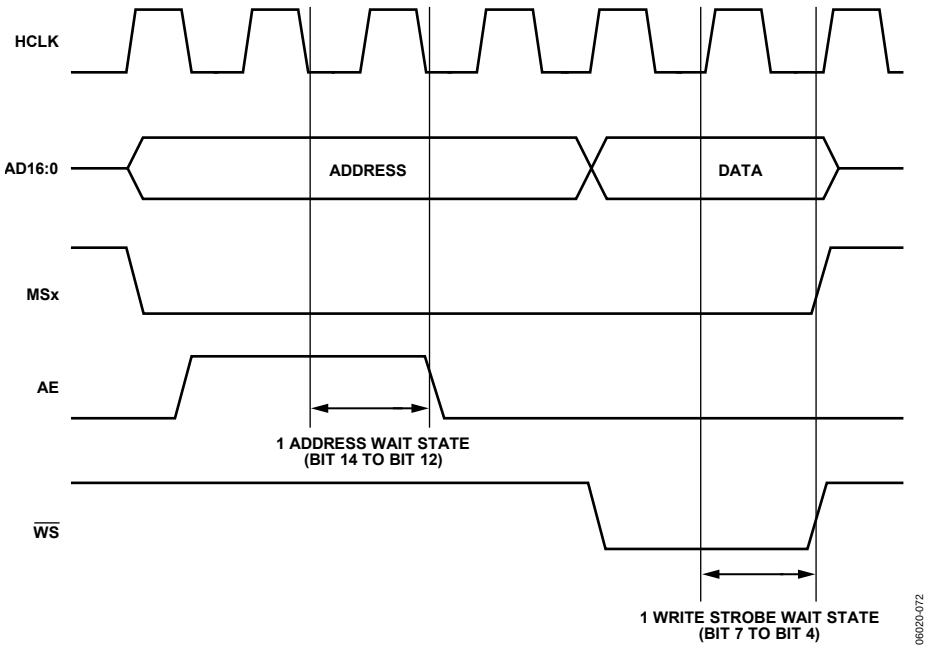

Figure 65. External Memory Write Cycle with Wait States