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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PLA, POR, PWM, PSM, Temp Sensor, WDT
Number of I/O	28
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7128bstz126

GENERAL DESCRIPTION

The ADuC7128/ADuC7129 are fully integrated, 1 MSPS, 12-bit data acquisition systems incorporating a high performance, multi-channel analog-to-digital converter (ADC), DDS with line driver, 16-/32-bit MCU, and Flash/EE memory on a single chip.

The ADC consists of up to 14 single-ended inputs. The ADC can operate in single-ended or differential input modes. The ADC input voltage is 0 to V_{REF}. Low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set.

The ADuC7128/ADuC7129 integrate a differential line driver output. This line driver transmits a sine wave whose values are calculated by an on-chip DDS or a voltage output determined by the DACDAT MMR.

The devices operate from an on-chip oscillator and PLL, generating an internal high frequency clock of 41.78 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated.

The microcontroller core is an ARM7TDMI®, 16-/32-bit reduced instruction set computer (RISC), offering up to 41 MIPS peak performance. There are 126 kB of nonvolatile Flash/EE provided on-chip, as well as 8 kB of SRAM. The ARM7TDMI core views all memory and registers as a single linear array.

On-chip factory firmware supports in-circuit serial download via the UART serial interface port, and nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ development system supporting this MicroConverter® family.

The parts operate from 3.0 V to 3.6 V and are specified over an industrial temperature range of −40°C to +125°C. When operating at 41.78 MHz, the power dissipation is 135 mW. The line driver output, if enabled, consumes an additional 30 mW.

Line Driver Load

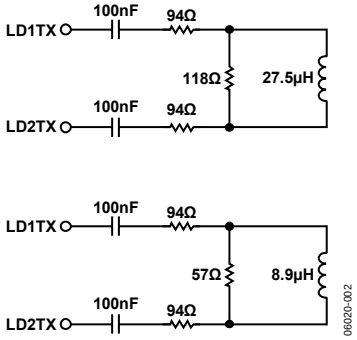

Figure 2. Line Driver Load Minimum (Top) and Maximum (Bottom)

Table 3. External Memory Read Cycle

Parameter	Min	Typ	Max	Unit
CLK	1/MD Clock	ns typ × (CDPOWCON[2:0] + 1)		
$t_{MS\_AFTER\_CLKH}$	4		8	ns
$t_{ADDR\_AFTER\_CLKH}$	4		16	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]) × CLK		
$t_{RD\_L\_AFTER\_AE\_L}$		½ CLK + (! XMxPAR[10]+ ! XMxPAR[9]) × CLK		
$t_{RD\_H\_AFTER\_CLKH}$	0		4	ns
t_{RD}		(XMxPAR[3:0] + 1) × CLK		
$t_{DATA\_BEFORE\_RD\_H}$	16			ns
$t_{DATA\_AFTER\_RD\_H}$	8	+ (! XMxPAR[9]) × CLK		
$t_{RELEASE\_WS\_AFTER\_RD\_H}$		1 × CLK		

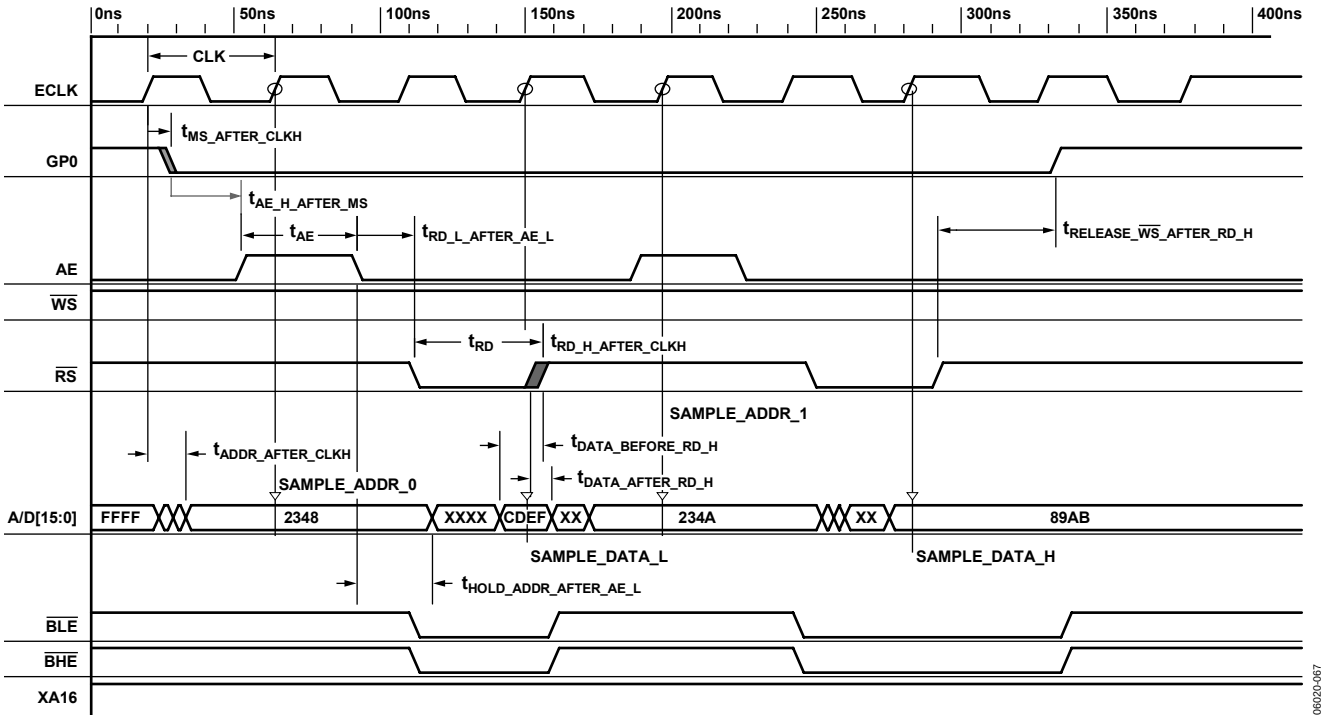

Figure 4. External Memory Read Cycle

Table 7. SPI Slave Mode Timing (PHASE Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{CS}	CS to SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{SL}	SCLOCK low pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{SH}	SCLOCK high pulse width[2]		$(SPIDIV + 1) \times t_{HCLK}$		ns
t_{DAV}	Data output valid after SCLOCK edge			$2 \times t_{HCLK} + 2 \times t_{UCLK}$	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLOCK rise time		5	12.5	ns
t_{SF}	SCLOCK fall time		5	12.5	ns
t_{SFS}	CS high after SCLOCK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.
[2] t_{HCLK} depends on the clock divider or CD bits in the PLLCON MMR, $t_{HCLK} = t_{UCLK}/2^{CD}$.

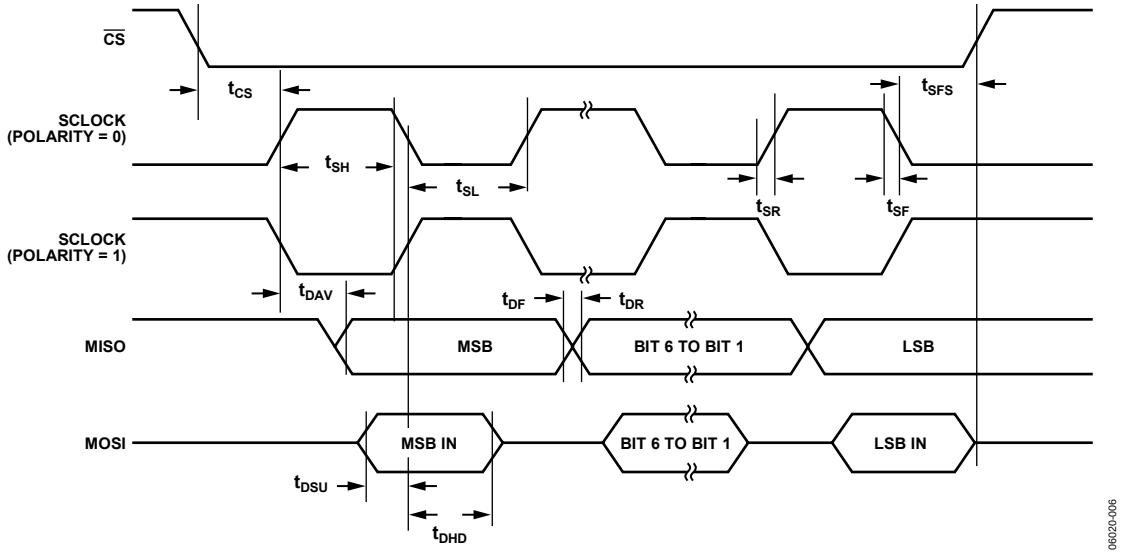

Figure 8. SPI Slave Mode Timing (PHASE Mode = 1)

Pin No.	Mnemonic	Type[1]	Description
17	P4.6/SPM10/AD14	I/O	General-Purpose Input and Output Port 4.6/Serial Port Mux Pin 10/External Memory AD14.
18	P4.7/SPM11/AD15	I/O	General-Purpose Input and Output Port 4.7/Serial Port Mux Pin 11/External Memory AD15.
19	P0.0/$\overline{BM}$/CMP_{OUT}/MS0	I/O	General-Purpose Input and Output Port 0.0 /Boot Mode. The ADuC7129 enters download mode if $\overline{BM}$ is low at reset and executes code if $\overline{BM}$ is pulled high at reset through a 1 kΩ resistor/voltage comparator output/external memory MS0.
20	P0.6/T1/$\overline{MRST}$	O	General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output/External Memory AE.
21	TCK	I	JTAG Test Port Input, Test Clock. Debug and download access.
22	TDO/P0.2/$\overline{BHE}$	O	JTAG Test Port Output, Test Data Out. Debug and download access/general-purpose input and output Port 0.2/External Memory $\overline{BHE}$.
23, 53, 67	IOGND	S	Ground for GPIO. Typically connected to DGND.
24, 54	IOV_{DD}	S	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
25	LV_{DD}	S	2.5 V Output of the On-Chip Voltage Regulator. Must be connected to a 0.47 µF capacitor to DGND.
26	DGND	S	Ground for Core Logic.
27	P3.0/PWM1/AD0	I/O	General-Purpose Input and Output Port 3.0/PWM1 Output/External Memory AD0.
28	P3.1/PWM2/AD1	I/O	General-Purpose Input and Output Port 3.1/PWM2 Output/External Memory AD1.
29	P3.2/PWM3/AD2	I/O	General-Purpose Input and Output Port 3.2/PWM3 Output/External Memory AD2.
30	P3.3/PWM4/AD3	I/O	General-Purpose Input and Output Port 3.3/PWM4 Output//External Memory AD3.
31	P2.4/MS0	I/O	General-Purpose Input and Output Port 2.4/Memory Select 0.
32	P0.3/ADC_{BUSY}/$\overline{TRST}$/A16	I/O	General-Purpose Input and Output Port 3.3/ADC_{BUSY} Signal/JTAG Test Port Input, Test Reset. Debug and download access/External Memory A16.
33	P2.5/MS1	I/O	General-Purpose Input and Output Port 2.5/Memory Select 1.
34	P2.6/MS2	I/O	General-Purpose Input and Output Port 2.6/Memory Select 2.
35	$\overline{RST}$	I	Reset Input (Active Low).
36	P3.4/PWM5/AD4	I/O	General-Purpose Input and Output Port 3.4/PWM5 Output/External Memory AD4.
37	P3.5/PWM6/AD5	I/O	General-Purpose Input and Output Port 3.5/PWM6 Output/External Memory AD5.
38	P0.4/IRQ0/$\overline{CONVST}$/MS1	I/O	General-Purpose Input and Output Port 0.5/External Interrupt Request 0, Active High/Start Conversion Input Signal for ADC/External Memory MS1.
39	P0.5/IRQ1/ADC_{BUSY}	I/O	General-Purpose Input and Output Port 0.6/External Interrupt Request 1, Active High/ADC_{BUSY} Signal.
40	P2.0/SPM9	I/O	General-Purpose Input and Output Port 2.0/Serial Port Mux Pin 9.
41	P0.7/SPM8/ECLK/XCLK	I/O	General-Purpose Input and Output Port 0.7/Serial Port Mux Pin 8/Output for the External Clock Signal/Input to the Internal Clock Generator Circuits.
42	XCLKO	O	Output from the Crystal Oscillator Inverter.
43	XCLKI	I	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
44	PV_{DD}	S	2.5 V PLL Supply. Must be connected to a 0.1 µF capacitor to DGND. Should be connected to 2.5 V LDO output.
45	DGND	S	Ground for PLL.
46	P3.6/AD6	I/O	General-Purpose Input and Output Port 3.6/External Memory AD6.
47	P3.7/AD7	I/O	General-Purpose Input and Output Port 3.7/External Memory AD7.
48	P2.7/MS3	I/O	General-Purpose Input and Output Port 2.7/Memory Select 3.
49	P2.1/$\overline{WS}$	I/O	General-Purpose Input and Output Port 2.1/Memory Write Select.
50	P2.2/$\overline{RS}$	I/O	General-Purpose Input and Output Port 2.1/Memory Read Select.
51	P1.7/SPM7	I/O	General-Purpose Input and Output Port 1.7/Serial Port Mux Pin 7.
52	P1.6/SPM6	I/O	General-Purpose Input and Output Port 1.6/Serial Port Mux Pin 6.
55	P4.0/S1/AD8	I/O	General-Purpose Input and Output Port 4.0/Quadrature Input 1/External Memory AD8.
56	P4.1/S2/AD9	I/O	General-Purpose Input and Output Port 4.1/Quadrature Input 2/External Memory AD9.
57	P1.5/SPM5	I/O	General-Purpose Input and Output Port 1.5/Serial Port Mux Pin 5.
58	P1.4/SPM4	I/O	General-Purpose Input and Output Port 1.4/Serial Port Mux Pin 4.
59	P1.3/SPM3	I/O	General-Purpose Input and Output Port 1.3/Serial Port Mux Pin 3.
60	P1.2/SPM2	I/O	General-Purpose Input and Output Port 1.2/Serial Port Mux Pin 2.
61	P1.1/SPM1	I/O	General-Purpose Input and Output Port 1.1/Serial Port Mux Pin 1.
62	P1.0/SPM0	I/O	General-Purpose Input and Output Port 1.0/Serial Port Mux Pin 0.

Pin No.	Mnemonic	Type[1]	Description
63	P4.2/AD10	I/O	General-Purpose Input and Output Port 4.2/External Memory AD10.
64	P4.3/PWM_{TRIP}/AD11	I/O	General-Purpose Input and Output Port 4.3/PWM Safety Cutoff/External Memory AD11.
65	P4.4/AD12	I/O	General-Purpose Input and Output Port 4.4/External Memory AD12.
66	P4.5/AD13	I/O	General-Purpose Input and Output Port 4.5/External Memory AD13.
68	REFGND	S	Ground for V_{REF}. Typically connected to DGND.
69	V_{REF}	I/O	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
70	DACGND	S	Ground for the DAC. Typically connected to AGND.
71, 72	AGND	S	Analog Ground.
75	$DACV_{DD}$	S	Power Supply for the DAC. This must be supplied with 2.5 V. It can be connected to the LDO output.
76	ADC11	I	Single-Ended or Differential Analog Input 11.
77	ADC0	I	Single-Ended or Differential Analog Input 0.
78	ADC1	I	Single-Ended or Differential Analog Input 1.
79	ADC2/CMP0	I	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
80	ADC3/CMP1	I	Single-Ended or Differential Analog Input 3/Comparator Negative Input.

[1] I = input, O = output, S = supply.

ADC CIRCUIT OVERVIEW

The analog-to-digital converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 3.0 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, differential track-and-hold, on-chip reference, and ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of the following three modes:

- Fully differential mode, for small and balanced signals
- Single-ended mode, for any single-ended signals
- Pseudo differential mode, for any single-ended signals, taking advantage of the common mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 to V_{REF} when operating in single-ended mode or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage V_{CM}, in the range 0 V to AV_{DD} and with a maximum amplitude of 2 V_{REF} (see Figure 32).

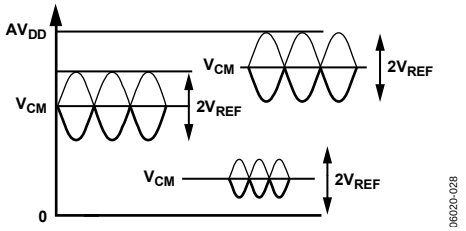

Figure 32. Examples of Balanced Signals for Fully Differential Mode

A high precision, low drift, and factory-calibrated 2.5 V reference is provided on-chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in software. An external $\overline{\text{CONVST}}$ pin, an output generated from the on-chip PLA, a Timer0, or a Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

If the signal has not been deasserted by the time the ADC conversion is complete, a second conversion begins automatically.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

ADC TRANSFER FUNCTION

Pseudo Differential Mode and Single-Ended Mode

In pseudo differential or single-ended mode, the input range is 0 to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = FS/4096 or
2.5 V/4096 = 0.61 mV or
610 μV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs, …, FS – 3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 33.

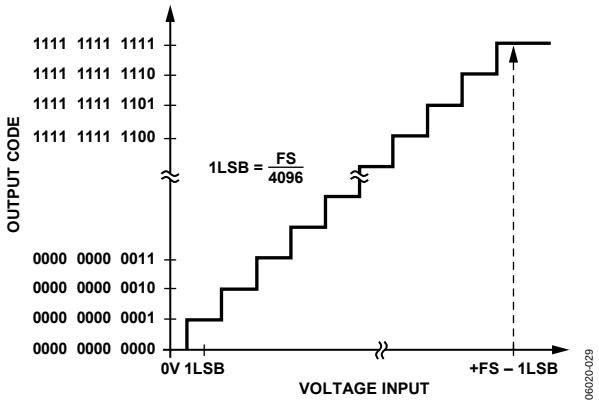

Figure 33. ADC Transfer Function in Pseudo Differential Mode or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins (that is, $V_{IN+} - V_{IN-}$). The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p ($2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals ($V_{IN+} + V_{IN-}$)/2, and is, therefore, the voltage upon which the two inputs are centered. This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 V_{REF}/4096 or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by one to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs, …, FS – 3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 34.

Table 41. FEExSTA MMR Bit Designations

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash/EE Interrupt Status Bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEExMOD register is set. Cleared when reading FEExSTA register.
2	Flash/EE Controller Busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command Fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading FEExSTA register.
0	Command Complete. Set by MicroConverter when a command is complete. Cleared automatically when reading FEExSTA register.

Table 42. FEExMOD MMR Bit Designations

Bit	Description
7:5	Reserved.
4	Flash/EE Interrupt Enable. Set by user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by user to disable the Flash/EE interrupt
3	Erase/Write Command Protection. Set by user to enable the erase and write commands. Cleared to protect the Flash/EE memory against erase/write command.
2	Reserved. Should always be set to 0 by the user.
1:0	Flash/EE Wait States. Both Flash/EE blocks must have the same wait state value for any change to take effect.

Table 43. Command Codes in FEExCON

Code	Command	Description
0x00[1]	Null	Idle State.
0x01[1]	Single read	Load FEExDAT with the 16-bit data indexed by FEExADR.
0x02[1]	Single write	Write FEExDAT at the address pointed by FEExADR. This operation takes 50 µs.
0x03[1]	Erase/Write	Erase the page indexed by FEExADR and write FEExDAT at the location pointed by FEExADR. This operation takes 20 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEExADR to the data in FEExDAT. The result of the comparison is returned in FEExSTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEExADR.
0x06[1]	Mass erase	Erase user space. The 2 kB of kernel are protected in Block 0. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Gives a signature of the 64 kB of Flash/EE in the 24-bit FEExSIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can be run only once. The value of FEExPRO is saved and can be removed only with a mass erase (0x06) or with the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No Operation, Interrupt Generated.

[1] The FEExCON register always reads 0x07 immediately after execution of any of these commands.

Table 44. FEE0PRO and FEE0HID MMR Bit Designations

Bit	Description
31	Read Protection. Cleared by user to protect Block 0. Set by user to allow reading Block 0.
30:0	Write Protection for Page 123 to Page 120, for Page 119 to Page 116, and for Page 3 to Page 0. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.

Table 45. FEE1PRO and FEE1HID MMR Bit Designations

Bit	Description
31	Read Protection. Cleared by user to protect Block 1. Set by user to allow reading Block 1.
30	Write Protection for Page 127 to Page 120. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.
31:0	Write Protection for Page 119 to Page 116 and for Page 3 to Page 0. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.

EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE), one cycle to execute the instruction and two cycles to get the 32-bit data from Flash/EE. A control flow instruction, such as a branch instruction, takes one cycle to fetch, but it also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 23 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD bit = 0). In addition, some dead times are needed before accessing data for any value of CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter and then four cycles are needed to fill the pipeline. A data processing instruction involving only core registers doesn't require any extra clock cycles, but if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data and two cycles to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 46.

Table 46. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N	$2 \times N$	N
STR	2/1	1	2×20 µs	1
STRH	2/1	1	20 µs	1
STRM/POP	2/1	N	$2 \times N \times 20$ µs	N

With $1 < N \leq 16$, N is the number of bytes of data to load or store in the multiple load/store instruction. The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles plus 40 µs.

DDSFRQ Register

Name	Address	Default Value	Access
DDSFRQ	0xFFFF0694	0x00000000	R/W

Table 54. DDSFRQ MMR Bit Designations

Bit	Description
31:0	Frequency select word (FSW)

The DDS frequency is controlled via the DDSFRQ MMR. This MMR contains a 32-bit word (FSW) that controls the frequency according to the following formula:

$$Frequency = \frac{FSW \times 20.8896 \text{ MHz}}{2^{32}}$$

DDSPHS Register

Name	Address	Default Value	Access
DDSPHS	0xFFFF0698	0x00000000	R/W

Table 55. DDSPHS MMR Bit Designations

Bit	Description
31:12	Reserved
11:0	Phase

The DDS phase offset is controlled via the DDSPHS MMR. This MMR contains a 12-bit value that controls the phase of the DDS output according to the following formula:

$$Phase\ Offset = \frac{2 \times \pi \times Phase}{2^{12}}$$

POWER SUPPLY MONITOR

The power supply monitor on the ADuC7128/ADuC7129 indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register (see Table 56). If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is cleared immediately once CMP goes high. Note that if the interrupt generated is exited before CMP goes high (IOV_{DD} is above the trip point), no further interrupts are generated until CMP returns high. The user should ensure that code execution remains within the ISR until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to the low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

The PSM does not operate correctly when using JTAG debug. It should be disabled in JTAG debug mode.

COMPARATOR

The ADuC7128/ADuC7129 integrate an uncommitted voltage comparator. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or the internal reference. The output of the comparator can be configured to generate a system interrupt, can be routed directly to the programmable logic array, can start an ADC conversion, or can be on an external pin, CMP_{OUT}.

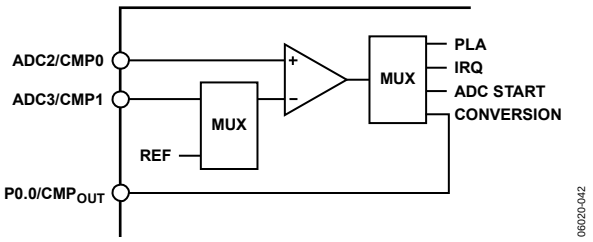

Figure 46. Comparator

Hysteresis

Figure 47 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

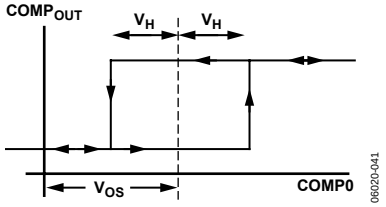

Figure 47. Comparator Hysteresis Transfer Function

Table 56. PSMCON MMR Bit Designations

Bit	Name	Description
3	CMP	Comparator Bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates the IOV_{DD} supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip Point Selection Bit. 0 = 2.79 V 1 = 3.07 V
1	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.
0	PSMI	Power Supply Monitor Interrupt Bit. This bit is set high by the MicroConverter if CMP is low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. Once CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A write of 0 has no effect. There is no timeout delay. PSMI can be cleared immediately once CMP goes high.

DIGITAL PERIPHERALS

PWM GENERAL OVERVIEW

The ADuC7128/ADuC7129 integrate a six channel PWM interface. The PWM outputs can be configured to drive an H-bridge or can be used as standard PWM outputs. On power up, the PWM outputs default to H-bridge mode. This ensures that the motor is turned off by default. In standard PWM mode, the outputs are arranged as three pairs of PWM pins. Users have control over the period of each pair of outputs and over the duty cycle of each individual output.

Table 63. PWM MMRs

Name	Description
PWMCON1	PWM Control
PWM1COM1	Compare Register 1 for PWM Outputs 1 and 2
PWM1COM2	Compare Register 2 for PWM Outputs 1 and 2
PWM1COM3	Compare Register 3 for PWM Outputs 1 and 2
PWM1LEN	Frequency Control for PWM Outputs 1 and 2
PWM2COM1	Compare Register 1 for PWM Outputs 3 and 4
PWM2COM2	Compare Register 2 for PWM Outputs 3 and 4
PWM2COM3	Compare Register 3 for PWM Outputs 3 and 4
PWM2LEN	Frequency Control for PWM Outputs 3 and 4
PWM3COM1	Compare Register 1 for PWM Outputs 5 and 6
PWM3COM2	Compare Register 2 for PWM Outputs 5 and 6
PWM3COM3	Compare Register 3 for PWM Outputs 5 and 6
PWM3LEN	Frequency Control for PWM Outputs 5 and 6
PWMCON2	PWM Convert Start Control
PWMICLR	PWM Interrupt Clear

In all modes, the PWMxCOMx MMRs controls the point at which the PWM outputs change state. An example of the first pair of PWM outputs (PWM1 and PWM2) is shown in Figure 49.

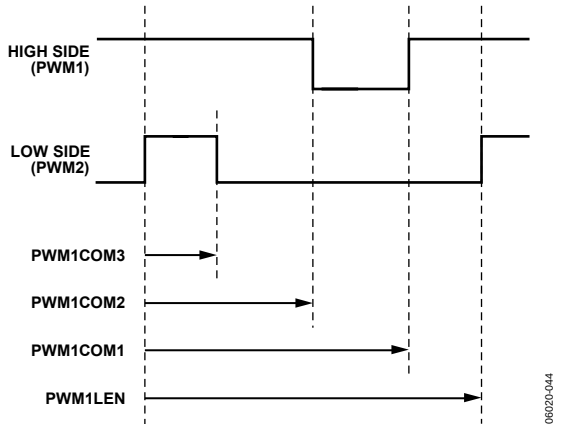

Figure 49. PWM Timing

The PWM clock is selectable via PWMCON1 with one of the following values: UCLK/2, 4, 8, 16, 32, 64, 128, or 256. The length of a PWM period is defined by PWMxLEN.

The PWM waveforms are set by the count value of the 16-bit timer and the compare registers contents as shown with the PWM1 and PWM2 waveforms above.

The low-side waveform, PWM2, goes high when the timer count reaches PWM1LEN, and it goes low when the timer count reaches the value held in PWM1COM3 or when the high-side waveform PWM1 goes low.

The high-side waveform, PWM1, goes high when the timer count reaches the value held in PWM1COM1, and it goes low when the timer count reaches the value held in PWM1COM2.

Table 64. PWMCON1 MMR Bit Designations

Bit	Name	Description
14	SYNC	Enables PWM Synchronization. Set to 1 by the user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the SYNC pin. Cleared by user to ignore transitions on the SYNC pin.
13	PWM6INV	Set to 1 by the user to invert PWM6. Cleared by user to use PWM6 in normal mode.
12	PWM4NV	Set to 1 by the user to invert PWM4. Cleared by user to use PWM4 in normal mode.
11	PWM2INV	Set to 1 by the user to invert PWM2. Cleared by user to use PWM2 in normal mode.
10	PWMTRIP	Set to 1 by the user to enable PWM trip interrupt. When the PWMTRIP input is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1. Set to 1 by the user to enable PWM outputs. Cleared by user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 65. If not in H-Bridge mode, this bit has no effect.
8	PWMCP2	PWM Clock Prescaler Bits.
7	PWMCP1	Sets UCLK divider.

GPxDAT Register

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W
GP3DAT	0xFFFF0D50	0x000000XX	R/W
GP4DAT	0xFFFF0D60	0x000000XX	R/W

GPxDAT is a Port x configuration and data register. It configures the direction of the GPIO pins of Port x, sets the output value for the pins configured as output, and receives and stores the input value of the pins configured as input.

Table 73. GPxDAT MMR Bit Designations

Bit	Description
31:24	Direction of the Data. Set to 1 by user to configure the GPIO pins as outputs. Cleared to 0 by user to configure the GPIO pins as inputs.
23:16	Port x Data Output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x Data Input (Read Only).

GPxSET Register

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W
GP3SET	0xFFFF0D54	0x000000XX	W
GP4SET	0xFFFF0D64	0x000000XX	W

GPxSET is a data set Port x register.

Table 74. GPxSET MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x Set Bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

GPxCLR Register

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W
GP3CLR	0xFFFF0D58	0x000000XX	W
GP4CLR	0xFFFF0D68	0x000000XX	W

GPxCLR is a data clear Port x register.

Table 75. GPxCLR MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x Clear Bit. Set to 1 by user to clear bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data out.
15:0	Reserved.

SERIAL PORT MUX

The serial port mux multiplexes the serial port peripherals (two I^2Cs, an SPI, and two UARTs) and the programmable logic array (PLA) to a set of 10 GPIO pins. Each pin must be configured to its specific I/O function as described in Table 76.

Table 76. SPM Configuration

Pin	GPIO (00)	UART (01)	UART/I2C/SPI (10)	PLA (11)
SPM0	P1.0	SIN0	I2C0SCL	PLAI[0]
SPM1	P1.1	SOUT0	I2C0SDA	PLAI[1]
SPM2	P1.2	RTS0	I2C1SCL	PLAI[2]
SPM3	P1.3	CTS0	I2C1SDA	PLAI[3]
SPM4	P1.4	RI0	SPICLK	PLAI[4]
SPM5	P1.5	DCD0	SPIMISO	PLAI[5]
SPM6	P1.6	DSR0	SPIMOSI	PLAI[6]
SPM7	P1.7	DTR0	SPICSL	PLAO[0]
SPM8	P0.7	ECLK	SIN0	PLAO[4]
SPM9	P2.0[1]	PWMSYNC	SOUT0	PLAO[5]
SPM10	P2.2[1]	RTS1	RS	PLAO[7]
SPM11	P2.3[1]	CTS1	AE	
SPM12	P2.4[1]	RI1	MS0	
SPM13	P2.5[1]	DCD1	MS1	
SPM14	P2.6[1]	DSR1	MS2	
SPM15	P2.7[1]	DTR1	MS3	
SPM16	P4.6	SIN1	AD14	PLAO[14]
SPM17	P4.7	SOUT1	AD15	PLAO[15]

[1] Available only on the 80-lead ADuC7129.

Table 76 details the mode for each of the SPMUX GPIO pins. This configuration has to be performed via the GP0CON, GP1CON and GP2CON MMRs. By default these pins are configured as GPIOs.

UART SERIAL INTERFACE

The ADuC7128/ADuC7129 contain two identical UART blocks. Although only UART0 is described here, UART1 functions in exactly the same way.

The UART peripheral is a full-duplex universal asynchronous receiver/transmitter, fully compatible with the 16450 serial port standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The UART includes a fractional divider for baud rate generation and has a network-addressable mode. The UART function is made available on 10 pins of the ADuC7128/ADuC7129 (see Table 77).

I²C-COMPATIBLE INTERFACES

The ADuC7128/ADuC7129 support two fully licensed I²C interfaces. The I²C interfaces are both implemented as full hardware master and slave interfaces. Because the two I²C interfaces are identical, only I²C0 is described in detail. Note that the two masters and slaves have individual interrupts.

Note that when configured as an I²C master device, the ADuC7128/ADuC7129 cannot generate a repeated start condition.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system. These pins require external pull-up resistors. Typical pull-up values are 10 kΩ.

The I²C bus peripheral addresses in the I²C bus system are programmed by the user. This ID can be modified any time a transfer is not in progress. The user can configure the interface to respond to four slave addresses.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the master does not lose arbitration and the slave acknowledges, then the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

The I²C peripheral master and slave functionality are independent and can be simultaneously active. A slave is activated when a transfer has been initiated on the bus.

If it is not addressed, it remains inactive until another transfer is initiated. This also allows a master device, which has lost arbitration, to respond as a slave in the same cycle.

Serial Clock Generation

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2C0DIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} is the clock before the clock divider.
DIVH is the high period of the clock.
DIVL is the low period of the clock.

Thus, for 100 kHz operation

DIVH = *DIVL* = 0xCF

and for 400 kHz

DIVH = 0x28 *DIVL* = 0x3C.

The I2CxDIV register corresponds to DIVH:DIVL.

Slave Addresses

Register I2C0ID0, Register I2C0ID1, Register I2C0ID2, and Register I2C0ID3 contain the device IDs. The device compares the four I2C0IDx registers to the address byte. The seven most significant bits of either ID register must be identical to that of the seven most significant bits of the first address byte received to be correctly addressed. The LSB of the ID registers, transfer direction bit, is ignored in the process of address recognition.

I²C REGISTERS

The I²C peripheral interface consists of 18 MMRs that are discussed in this section.

I2CxMSTA Register

Name	Address	Default Value	Access
I2C0MSTA	0xFFFF0800	0x00	R
I2C1MSTA	0xFFFF0900	0x00	R

I2CxMSTA is a status register for the master channel.

Table 92. I2C0MSTA MMR Bit Designations

Bit	Description
7	Master Transmit FIFO Flush. Set by user to flush the master Tx FIFO. Cleared automatically once the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
6	Master Busy. Set automatically if the master is busy. Cleared automatically.
5	Arbitration Loss. Set in multimaster mode if another master has the bus. Cleared when the bus becomes available.
4	No Acknowledge. Set automatically if there is no acknowledge of the address by the slave device. Cleared automatically by reading the I2C0MSTA register.
3	Master Receive IRQ. Set after receiving data. Cleared automatically by reading the I2C0MRX register.
2	Master Transmit IRQ. Set at the end of a transmission. Cleared automatically by writing to the I2C0MTX register.
1	Master Transmit FIFO Underflow. Set automatically if the master transmit FIFO is underflowing. Cleared automatically by writing to the I2C0MTX register.
0	Master TX FIFO Not Full. Set automatically if the slave transmit FIFO is not full. Cleared automatically by writing twice to the I2C0STX register.

Table 99. PLACLK MMR Bit Designations

Bit	Value	Description
7		Reserved.
6:4		Block 1 Clock Source Selection.
	000	GPIO Clock on P0.5.
	001	GPIO Clock on P0.0.
	010	GPIO Clock on P0.7.
	011	HCLK.
	100	OCLK.
	101	Timer1 Overflow.
	110	Timer4 Overflow.
	Other	Reserved.
3		Reserved.
2:0		Block 0 Clock Source Selection.
	000	GPIO Clock on P0.5.
	001	GPIO Clock on P0.0.
	010	GPIO Clock on P0.7.
	011	HCLK.
	100	OCLK.
	101	Timer1 Overflow.
	110	Timer4 Overflow.
	Other	Reserved.

Table 100. PLAIRQ MMR Bit Designations

Bit	Value	Description
15:13		Reserved.
12		PLA IRQ1 Enable Bit Set by user to enable IRQ1 output from PLA Cleared by user to disable IRQ1 output from PLA
11:8		PLA IRQ1 Source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	…	
	1111	PLA Element 15.
7:5		Reserved.
4		PLA IRQ0 Enable Bit. Set by user to enable IRQ0 output from PLA. Cleared by user to disable IRQ0 output from PLA.
3:0		PLA IRQ0 Source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	…	
	1111	PLA Element 15.

Table 101. PLAADC MMR Bit Designations

Bit	Value	Description
31:5		Reserved.
4		ADC Start Conversion Enable Bit. Set by user to enable ADC start conversion from PLA. Cleared by user to disable ADC start conversion from PLA.
3:0		ADC Start Conversion Source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	…	
	1111	PLA Element 15.

Table 102. PLADIN MMR Bit Designations

Bit	Description
31:16	Reserved.
15:0	Input Bit from Element 15 to Element 0.

Table 103. PLAOUT MMR Bit Designations

Bit	Description
31:16	Reserved.
15:0	Output Bit from Element 15 to Element 0.

Table 111. T1CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved. Should be set to 0 by the user.
17		Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12		Event Select Range, 0 to 31. The events are as described in the introduction to the timers.
11:9		Clock Select.
	000	Core Clock (Default).
	001	32.768 kHz Oscillator.
	010	P1.0.
	011	P0.6.
8		Count Up. Set by user for Timer1 to count up. Cleared by user for Timer1 to count down (default).
7		Timer1 Enable Bit. Set by user to enable Timer1. Cleared by user to disable Timer1 (default).
6		Timer1 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256.
	1111	Source Clock/32768.

Table 113. T2CON MMR Bit Designations

Bit	Value	Description
31:11		Reserved.
10:9		Clock Source Select.
	00	Core Clock (Default).
	01	Internal 32.768 kHz Oscillator.
	10	External 32.768 kHz Watch Crystal.
	11	External 32.768 kHz Watch Crystal.
8		Count Up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down (default).
7		Timer2 Enable Bit. Set by user to enable Timer2. Cleared by user to disable Timer2 (default).
6		Timer2 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256. This setting should be used in conjunction with Timer2 formats 1,0 and 1,1.
	1111	Source Clock/32,768.

Table 117. T4CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved. Set by user to 0.
17		Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12		Event Select Range, 0 to 31. The events are as described in the Timers section.
11:9		Clock Select.
	000	Core Clock (Default).
	001	32.768 kHz Oscillator.
	010	P4.6.
	011	P4.7.
8		Count Up. Set by user for Timer4 to count up. Cleared by user for Timer4 to count down (default).
7		Timer4 Enable Bit. Set by user to enable Timer4. Cleared by user to disable Timer4 (default).
6		Timer4 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256.
	1111	Source Clock/32,768.

EXTERNAL MEMORY INTERFACING

The ADuC7129 is the only model in the series that features an external memory interface. The external memory interface requires a larger number of pins. This is why it is only available on larger pin count packages. The XMCFG MMR must be set to 1 to use the external port.

Although 32-bit addresses are supported internally, only the lower 16 bits of the address are on external pins.

The memory interface can address up to four 128 kB regions of asynchronous memory (SRAM and/or EEPROM).

The pins required for interfacing to an external memory are shown in Table 118.

Table 118. External Memory Interfacing Pins

Pin	Function
AD[15:0]	Address/Data Bus.
A16	Extended Addressing for 8-Bit Memory Only.
MS[3:0]	Memory Select.
WR ($\overline{WR}$)	Write Strobe.
RS ($\overline{RS}$)	Read Strobe.
AE	Address Latch Enable.
$\overline{BHE}$, $\overline{BLE}$	Byte Write Capability.

There are four external memory regions available, as described in Table 119. Associated with each region are the MS[3:0] pins. These signals allow access to the particular region of external memory. The size of each memory region can be 128 kB maximum, 64 k × 16, or 128 k × 8. To access 128 kB with an 8-bit memory, an extra address line (A16) is provided. (See the example in Figure 61). The four regions are configured independently.

Table 119. Memory Regions

Address Start	Address End	Contents
0x10000000	0x1000FFFF	External Memory 0
0x20000000	0x2000FFFF	External Memory 1
0x30000000	0x3000FFFF	External Memory 2
0x40000000	0x4000FFFF	External Memory 3

Each external memory region can be controlled through three MMRs: XMCFG, XMxCON, and XMxPAR.

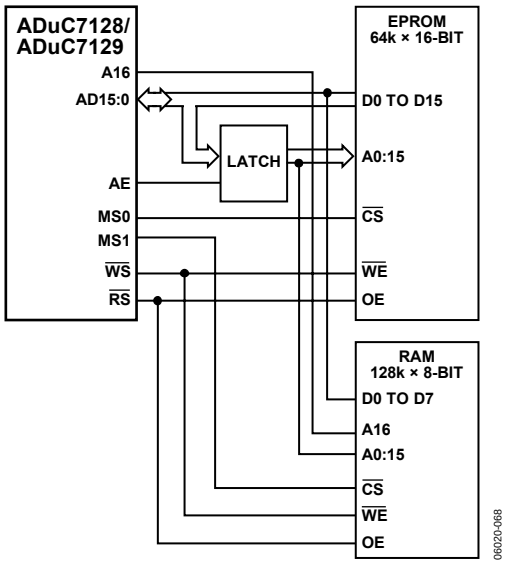

Figure 61. Interfacing to External EPROM/RAM

XMCFG Register

Name	Address	Default Value	Access
XMCFG	0xFFFFF000	0x00	R/W

XMCFG is set to 1 to enable external memory access. This must be set to 1 before any port pins function as external memory access pins. The port pins must also be individually enabled via the GPxCON MMR.

XMxCON Registers

Name	Address	Default Value	Access
XM0CON	0xFFFFF010	0x00	R/W
XM1CON	0xFFFFF014	0x00	R/W
XM2CON	0xFFFFF018	0x00	R/W
XM3CON	0xFFFFF01C	0x00	R/W

XMxCON registers are the control registers for each memory region. They allow the enabling/disabling of a memory region and control the data bus width of the memory region.

Table 120. XMxCON MMR Bit Designations

Bit	Description
1	Data Bus Width Select. Set by the user to select a 16-bit data bus. Cleared by the user to select an 8-bit data bus.
0	Memory Region Enable. Set by the user to enable memory region. Cleared by the user to disable the memory region.

XMxPAR Registers

Name	Address	Default Value	Access
XM0PAR	0xFFFFF020	0x70FF	R/W
XM1PAR	0xFFFFF024	0x70FF	R/W
XM2PAR	0xFFFFF028	0x70FF	R/W
XM3PAR	0xFFFFF02C	0x70FF	R/W

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7128/ADuC7129. For LV_{DD} below 2.45 V, the internal POR holds the ADuC7128/ADuC7129 in reset. As LV_{DD} rises above 2.45 V, an internal timer times out for typically 64 ms before the part is released from reset. The user must ensure that the power supply, IOV_{DD}, has reached a stable 3.0 V minimum level by this time. On power-down, the internal POR holds the ADuC7128/ADuC7129 in reset until LV_{DD} has dropped below 2.45 V. Figure 72 illustrates the operation of the internal POR in detail.

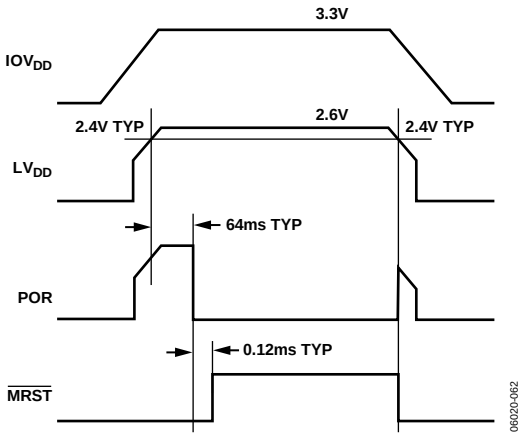

Figure 72. Internal Power-On Reset Operation

OUTLINE DIMENSIONS

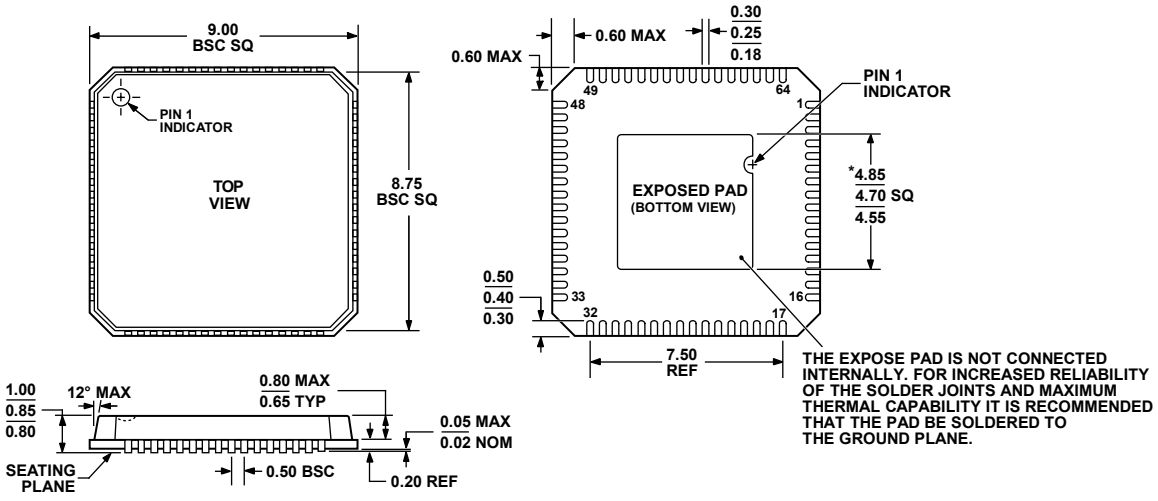

Figure 73. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

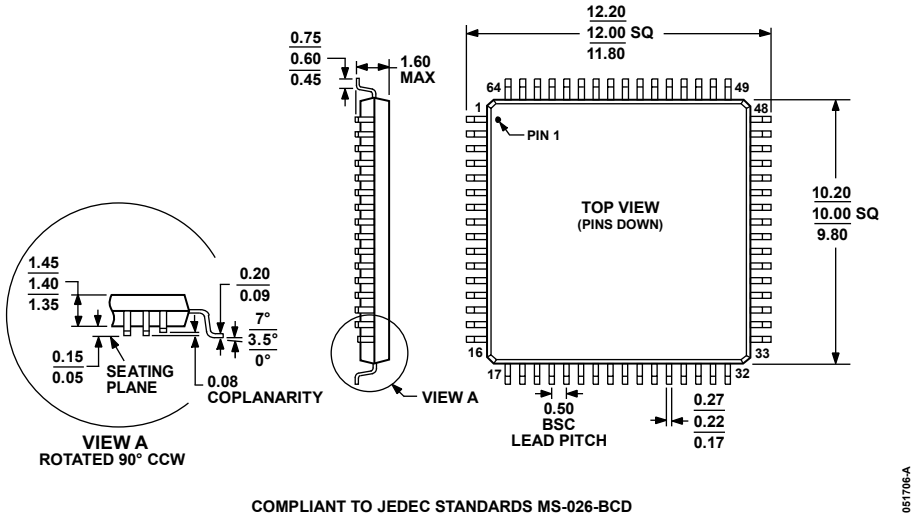

Figure 74. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters