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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, POR, PWM, PSM, Temp Sensor, WDT
Number of I/O	38
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7129bstz126-rl

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REVISION HISTORY

4/07—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 3.0 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz. All specifications T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity[3]		±0.7	±2.0	LSB	2.5 V internal reference 85°C to 125°C only
		±0.7	±1.5	LSB	2.5 V internal reference −40°C to +85°C
		±2.0		LSB	1.0 V external reference
Differential Nonlinearity[3]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		±0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[4]					
Offset Error			±5	LSB	
Offset Error Match		±1		LSB	
Gain Error			±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					F_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	
Crosstalk Between Channel 12 and Channel 13		−60		dB	
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode[5]			$V_{CM} \pm V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current			±15	µA	85°C to 125°C only
		±1	±3	µA	−40°C to +85°C
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±2.5	mV	Measured at T_A = 25°C
Reference Drop When DAC Enabled		9		mV	Reference drop when DAC enabled
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		80		dB	
Output Impedance		40		Ω	
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT[6]					
Input Voltage Range	0.625		AV_{DD}	V	
Input Impedance		38		kΩ	
DAC CHANNEL SPECIFICATIONS					
VDAC Output					R_L = 5 kΩ, C_L = 100 pF
Voltage Swing		$(0.33 \times V_{REF} \pm 0.2 \times V_{REF}) \times 1.33$			V_{REF} is the internal 2.5 V reference
I/V Output Resistance			7	Ω	V mode selected
Low-Pass Filter 3 dB Point		1		MHz	2-pole at 1.5 MHz and 2 MHz
Resolution		10		Bits	

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

Parameter	Min	Typ	Max	Unit
CLK		UCLK		
$t_{MS\_AFTER\_CLKH}$	0		4	ns
$t_{ADDR\_AFTER\_CLKH}$	4		8	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10]) × CLK		
$t_{HOLD\_ADDR\_BEFORE\_WR\_L}$		(!XMxPAR[8]) × CLK		
$t_{WR\_L\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK		
$t_{DATA\_AFTER\_WR\_L}$	8		12	ns
t_{WR}		(XMxPAR[7:4] + 1) × CLK		
$t_{WR\_H\_AFTER\_CLKH}$	0		4	ns
$t_{HOLD\_DATA\_AFTER\_WR\_H}$		(!XMxPAR[8]) × CLK		
$t_{BEN\_AFTER\_AE\_L}$		½ CLK		
$t_{RELEASE\_MS\_AFTER\_WR\_H}$		(!XMxPAR[8] + 1) × CLK		

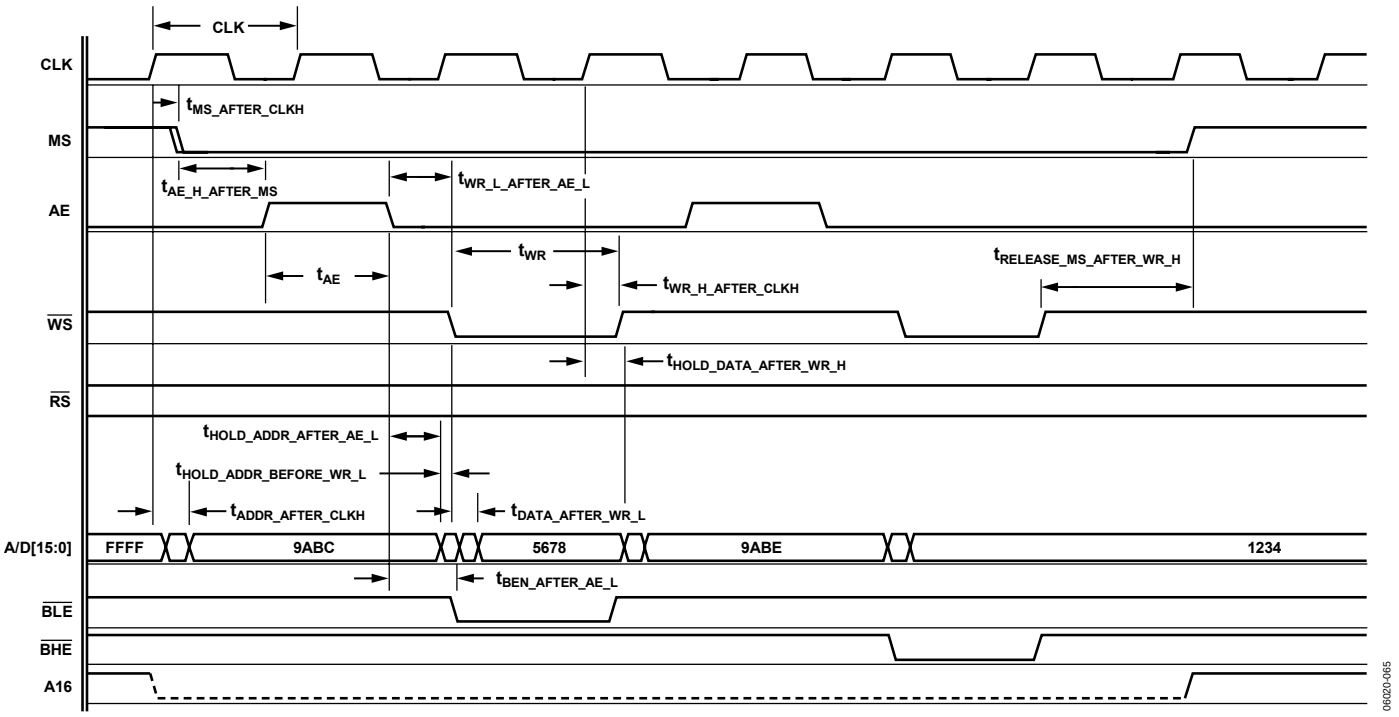

Figure 3. External Memory Write Cycle

ABSOLUTE MAXIMUM RATINGS

DV_{DD} = IOV_{DD}, AGND = REFGND = DACGND = GND_{REF}.
T_A = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Output to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	24°C/W
64-Lead LQFP	47°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

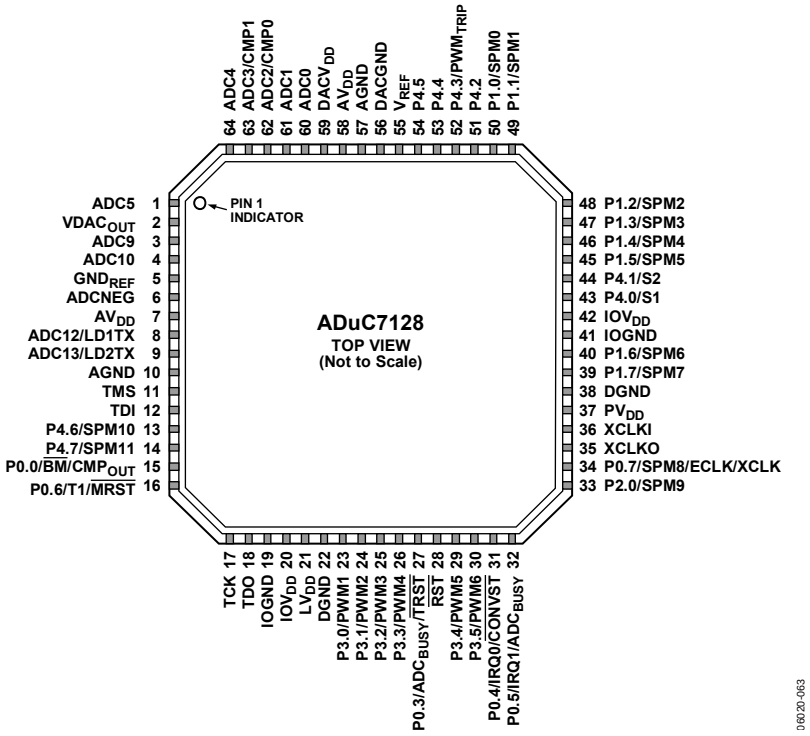

Figure 10. ADuC7128 Pin Configuration

Table 10. ADuC7128 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	ADC5	I	Single-Ended or Differential Analog Input 5/Line Driver Input.
2	$VDAC_{OUT}$	O	Output from DAC Buffer.
3	ADC9	I	Single-Ended or Differential Analog Input 9.
4	ADC10	I	Single-Ended or Differential Analog Input 10.
5	GND_{REF}	S	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
6	ADCNEG	I	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
7, 58	AV_{DD}	S	Analog Power.
8	ADC12/LD1TX	I/O	Single-Ended or Differential Analog Input 12/DAC Differential Negative Output.
9	ADC13/LD2TX	I/O	Single-Ended or Differential Analog Input 13/DAC Differential Positive Output.
10, 57	AGND	S	Analog Ground. Ground reference point for the analog circuitry.
11	TMS	I	JTAG Test Port Input, Test Mode Select. Debug and download access.
12	TDI	I	JTAG Test Port Input, Test Data In. Debug and download access.
13	P4.6/SPM10	I/O	General-Purpose Input and Output Port 4.6/Serial Port Mux Pin 10.
14	P4.7/SPM11	I/O	General-Purpose Input and Output Port 4.7/Serial Port Mux Pin 11.
15	$P0.0/\overline{BM}/CMP_{OUT}$	I/O	General-Purpose Input and Output Port 0.0/Boot Mode. The ADuC7128 enters download mode if $\overline{BM}$ is low at reset and executes code if $\overline{BM}$ is pulled high at reset through a 1 kΩ resistor/voltage comparator output.
16	$P0.6/T1/\overline{MRST}$	O	General-Purpose Output Port 0.6/Timer1 Input/Power-On Reset Output.
17	TCK	I	JTAG Test Port Input, Test Clock. Debug and download access.
18	TDO	O	JTAG Test Port Output, Test Data Out. Debug and download access.
19, 41	IOGND	S	Ground for GPIO. Typically connected to DGND.
20, 42	IOV_{DD}	S	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.

Pin No.	Mnemonic	Type[1]	Description
21	LV_{DD}	S	2.5 V Output of the On-Chip Voltage Regulator. Must be connected to a 0.47 µF capacitor to DGND.
22	DGND	S	Ground for Core Logic.
23	P3.0/PWM1	I/O	General-Purpose Input and Output Port 3.0/PWM1 Output.
24	P3.1/PWM2	I/O	General-Purpose Input and Output Port 3.1/PWM2 Output.
25	P3.2/PWM3	I/O	General-Purpose Input and Output Port 3.2/PWM3 Output.
26	P3.3/PWM4	I/O	General-Purpose Input and Output Port 3.3/PWM4 Output.
27	P0.3/ADC_{BUSY}/$\overline{TRST}$	I/O	General-Purpose Input and Output Port 3.3/ADC_{BUSY} Signal/JTAG Test Port Input, Test Reset. Debug and download access.
28	$\overline{RST}$	I	Reset Input (Active Low).
29	P3.4/PWM5	I/O	General-Purpose Input and Output Port 3.4/PWM5 Output.
30	P3.5/PWM6	I/O	General-Purpose Input and Output Port 3.5/PWM6 Output.
31	P0.4/IRQ0/$\overline{CONVST}$	I/O	General-Purpose Input and Output Port 0.5/External Interrupt Request 0, Active High/Start Conversion Input Signal for ADC.
32	P0.5/IRQ1/ADC_{BUSY}	I/O	General-Purpose Input and Output Port 0.6/External Interrupt Request 1, Active High/ADC_{BUSY} Signal.
33	P2.0/SPM9	I/O	General-Purpose Input and Output Port 2.0/Serial Port Mux Pin 9.
34	P0.7/SPM8/ECLK/XCLK	I/O	General-Purpose Input and Output Port 0.7/Serial Port Mux Pin 8/Output for the External Clock Signal/Input to the Internal Clock Generator Circuits.
35	XCLKO	O	Output from the Crystal Oscillator Inverter.
36	XCLKI	I	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
37	PV_{DD}	S	2.5 V PLL Supply. Must be connected to a 0.1 µF capacitor to DGND. Should be connected to 2.5 V LDO output.
38	DGND	S	Ground for PLL.
39	P1.7/SPM7	I/O	General-Purpose Input and Output Port 1.7/Serial Port Mux Pin 7.
40	P1.6/SPM6	I/O	General-Purpose Input and Output Port 1.6/Serial Port Mux Pin 6.
43	P4.0/S1	I/O	General-Purpose Input and Output Port 4.0/Quadrature Input 1.
44	P4.1/S2	I/O	General-Purpose Input and Output Port 4.1/Quadrature Input 2.
45	P1.5/SPM5	I/O	General-Purpose Input and Output Port 1.5/Serial Port Mux Pin 5.
46	P1.4/SPM4	I/O	General-Purpose Input and Output Port 1.4/Serial Port Mux Pin 4.
47	P1.3/SPM3	I/O	General-Purpose Input and Output Port 1.3/Serial Port Mux Pin 3.
48	P1.2/SPM2	I/O	General-Purpose Input and Output Port 1.2/Serial Port Mux Pin 2.
49	P1.1/SPM1	I/O	General-Purpose Input and Output Port 1.1/Serial Port Mux Pin 1.
50	P1.0/SPM0	I/O	General-Purpose Input and Output Port 1.0/Serial Port Mux Pin 0.
51	P4.2	I/O	General-Purpose Input and Output Port 4.2.
52	P4.3/ PWM_{TRIP}	I/O	General-Purpose Input and Output Port 4.3/PWM Safety Cutoff.
53	P4.4	I/O	General-Purpose Input and Output Port 4.4.
54	P4.5	I/O	General-Purpose Input and Output Port 4.5.
55	V_{REF}	I/O	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
56	DACGND	S	Ground for the DAC. Typically connected to AGND.
59	$DACV_{DD}$	S	Power Supply for the DAC. This must be supplied with 2.5 V. This can be connected to the LDO output.
60	ADC0	I	Single-Ended or Differential Analog Input 0.
61	ADC1	I	Single-Ended or Differential Analog Input 1.
62	ADC2/CMP0	I	Single-Ended or Differential Analog Input 2/Comparator Positive Input.
63	ADC3/CMP1	I	Single-Ended or Differential Analog Input 3/Comparator Negative Input.
64	ADC4	I	Single-Ended or Differential Analog Input 4.

[1] I = input, O = output, S = supply.

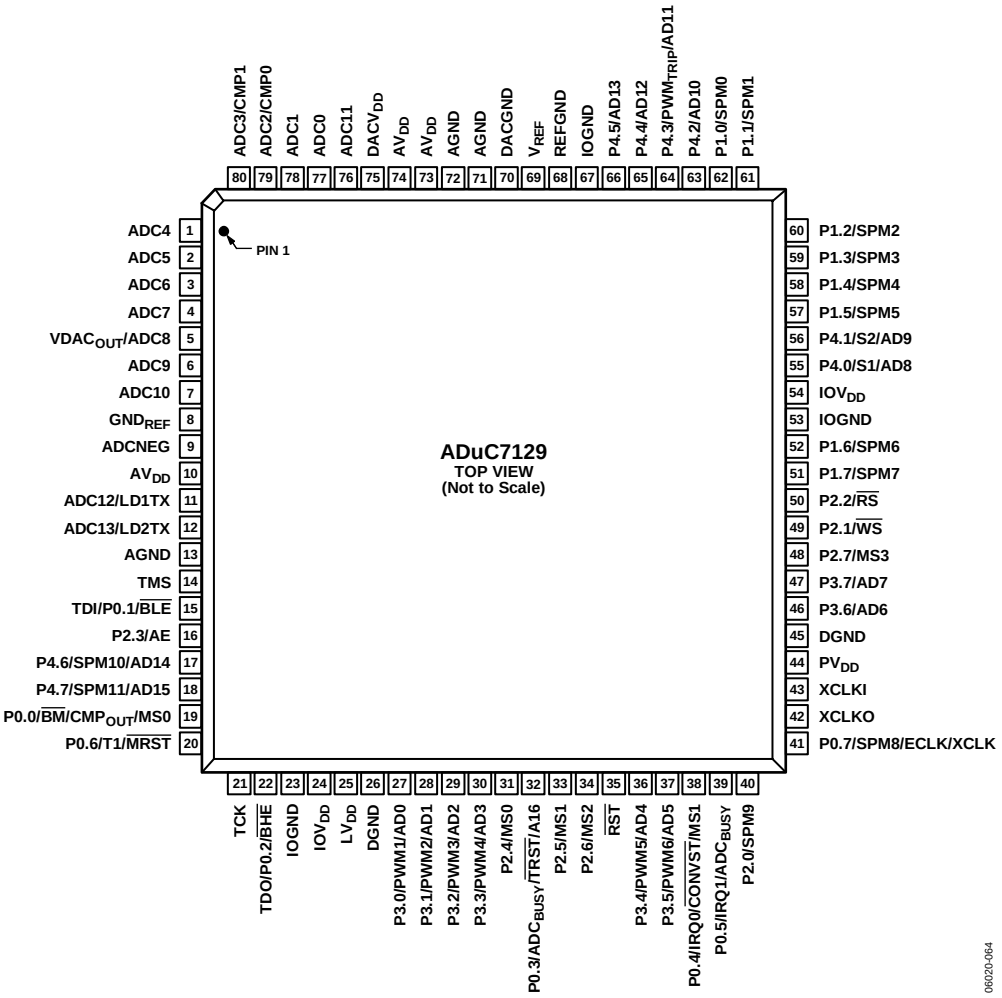

Figure 11. ADuC7129 Pin Configuration

Table 11. ADuC7129 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	ADC4	I	Single-Ended or Differential Analog Input 4.
2	ADC5	I	Single-Ended or Differential Analog Input 5.
3	ADC6	I	Single-Ended or Differential Analog Input 6.
4	ADC7	I	Single-Ended or Differential Analog Input 7.
5	$VDAC_{OUT}$/ADC8	I	Output from DAC Buffer/Single-Ended or Differential Analog Input 8.
6	ADC9	I	Single-Ended or Differential Analog Input 9.
7	ADC10	I	Single-Ended or Differential Analog Input 10.
8	GND_{REF}	S	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
9	ADCNEG	I	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
10, 73, 74	AV_{DD}	S	3.3 V Analog Supply.
11	ADC12/LD1TX	I/O	Single-Ended or Differential Analog Input 12/DAC Differential Negative Output.
12	ADC13/LD2TX	I/O	Single-Ended or Differential Analog Input 13/DAC Differential Positive Output.
13	AGND	S	Analog Ground. Ground reference point for the analog circuitry.
14	TMS	I	JTAG Test Port Input, Test Mode Select. Debug and download access.
15	TDI/P0.1/$\overline{BLE}$	I/0	JTAG Test Port Input, Test Data In. Debug and download access/general-purpose input and output Port 0.1/External Memory $\overline{BLE}$.
16	P2.3/AE	I/O	General-Purpose Input and Output Port 2.3/AE Output.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, that is, +½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal to (*Noise* + *Distortion*) = (6.02 N + 1.76) dB

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes for the output to settle to within a 1 LSB level for a full-scale input change.

FEE1DAT Register

Name	Address	Default Value	Access
FEE1DAT	0xFFFF0E8C	0xXXXX	R/W

FEE1DAT is a 16-bit data register.

FEE1ADR Register

Name	Address	Default Value	Access
FEE1ADR	0xFFFF0E90	0x0000	R/W

FEE1ADR is a 16-bit address register.

FEE1SGN Register

Name	Address	Default Value	Access
FEE1SGN	0xFFFF0E98	0xFFFFFF	R

FEE1SGN is a 24-bit code signature.

FEE1PRO Register

Name	Address	Default Value	Access
FEE1PRO	0xFFFF0E9C	0x00000000	R/W

FEE1PRO provides protection following subsequent reset MMR. It requires a software key (see Table 45).

FEE1HID Register

Name	Address	Default Value	Access
FEE1HID	0xFFFF0EA0	0xFFFFFFFF	R/W

FEE1HID provides immediate protection MMR. It does not require any software keys (see Table 45).

FEE0STA Register

Name	Address	Default Value	Access
FEE0STA	0xFFFF0E00	0x0000	R/W

FEE1STA Register

Name	Address	Default Value	Access
FEE1STA	0xFFFF0E80	0x0000	R/W

FEE0MOD Register

Name	Address	Default Value	Access
FEE0MOD	0xFFFF0E04	0x80	R/W

FEE1MOD Register

Name	Address	Default Value	Access
FEE1MOD	0xFFFF0E84	0x80	R/W

FEE0CON Register

Name	Address	Default Value	Access
FEE0CON	0xFFFF0E08	0x0000	R/W

FEE1CON Register

Name	Address	Default Value	Access
FEE1CON	0xFFFF0E88	0x0000	R/W

DACEN Register

Name	Address	Default Value	Access
DACEN	0xFFFF06B8	0x00	R/W

Table 50. DACEN MMR Bit Designations

Bit	Description
7:1	Reserved.
0	Set to 1 by the user to enable DAC mode. Set to 0 by the user to enable DDS mode.

DACDAT Register

Name	Address	Default Value	Access
DACDAT	0xFFFF06B4	0x0000	R/W

Table 51. DACDAT MMR Bit Designations

Bit	Description
15:10	Reserved.
9:0	10-bit data for DAC.

The DACDAT MMR controls the output of the DAC. The data written to this register is a ±9-bit signed value. This means that 0x0000 represents midscale, 0x0200 represents zero scale, and 0x01FF represents full scale.

DACEN and DACDAT require key access. To write to these MMRs, use the sequences shown in Table 52.

Table 52. DACEN and DACDAT Write Sequences

DACEN	DACDAT
DACKEY0 = 0x07	DACKEY0 = 0x07
DACEN = user value	DACDAT = user value
DACKEY1 = 0xB9	DACKEY1 = 0xB9

DDS

The DDS is used to generate a digital sine wave signal for the DAC on the ADuC7128/ADuC7129. It can be enabled into a free running mode by the user.

Both the phase and frequency can be controlled.

Table 53. DDSCON MMR Bit Designations

Bit	Description	
7:6	Reserved.	
5	DDS Output Enable. Set by user to enable the DDS output. This has an effect only if the DDS is selected in DACCON. Cleared by user to disable the DDS output.	
4	Reserved.	
3:0	Binary Divide Control.	
	DIV	**Scale Ratio**
	0000	0.000
	0001	0.125
	0010	0.250
	0011	0.375
	0100	0.500
	0101	0.625
	0110	0.750
	0111	0.875
	1xxx	1.000

Table 58. Operating Modes

Mode	Core	Peripherals	PLL	XTAL/T2/T3	XIRQ	Start-Up/Power-On Time
Active	On	On	On	On	On	130 ms at CD = 0
Pause		On	On	On	On	24 ns at CD = 0; 3.06 µs at CD = 7
Nap			On	On	On	24 ns at CD = 0; 3.06 µs at CD = 7
Sleep				On	On	1.58 ms
Stop					On	1.7 ms

Table 59. Typical Current Consumption at 25°C

PC[2:0]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
000	Active	33.1	21.2	13.8	10	8.1	7.2	6.7	6.45
001	Pause	22.7	13.3	8.5	6.1	4.9	4.3	4	3.85
010	Nap	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8
011	Sleep	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
100	Stop	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

MMRs and Keys

To prevent accidental programming, a certain sequence must be followed when writing in the PLLCON and POWCON registers (see Table 60).

PLLKEYx Register

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

PLLCON Register

Name	Address	Default Value	Access
PLLCON	0xFFFF0414	0x21	R/W

POWKEYx Register

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

POWCON Register

Name	Address	Default Value	Access
POWCON	0xFFFF0408	0x0003	R/W

Table 60. PLLCON and POWCON Write Sequence

PLLCON	POWCON
PLLKEY1 = 0xAA	POWKEY1 = 0x01
PLLCON = 0x01	POWCON = user value
PLLKEY2 = 0x55	POWKEY2 = 0xF4

Table 61. PLLCON MMR Bit Designations

Bit	Value	Name	Description
7:6			Reserved.
5		OSEL	32 kHz PLL Input Selection. Set by user to use the internal 32 kHz oscillator. Set by default. Cleared by user to use the external 32 kHz crystal.
4:2			Reserved.
1:0		MDCLK	Clocking Modes.
	00		Reserved.
	01		PLL. Default configuration.
	10		Reserved.
	11		External clock on P0.7 pin.

Table 62. POWCON MMR Bit Designations

Bit	Value	Name	Description
7			Reserved.
6:4		PC	Operating Modes.
	000		Active mode.
	001		Pause mode.
	010		Nap.
	011		Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the ADuC7128/ADuC7129.
	100		Stop mode.
	Others		Reserved.
3		RSVD	Reserved.
2:0		CD	CPU Clock Divider Bits.
	000		41.779200 MHz.
	001		20.889600 MHz.
	010		10.444800 MHz.
	011		5.222400 MHz.
	100		2.611200 MHz.
	101		1.305600 MHz.
	110		654.800 kHz.
	111		326.400 kHz.

Bit	Name	Description
6	PWMCP0	2. 4. 8. 16. 32. 64. 128. 256.
5	POINV	Set to 1 by the user to invert all PWM outputs. Cleared by user to use PWM outputs as normal.
4	HOFF	High Side Off. Set to 1 by the user to force PWM1 and PWM3 outputs high. This also forces PWM2 and PWM4 low. Cleared by user to use the PWM outputs as normal.
3	LCOMP	Load Compare Registers. Set to 1 by the user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by user to use the values previously stored in the internal compare registers.
2	DIR	Direction Control. Set to 1 by the user to enable PWM1 and PWM2 as the output signals while PWM3 and PWM4 are held low. Cleared by user to enable PWM3 and PWM4 as the output signals while PWM1 and PWM2 are held low.
1	HMODE	Enables H-bridge mode. Set to 1 by the user to enable H-Bridge mode and Bit 1 to Bit 5 of PWMCON1. Cleared by user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by the user to enable all PWM outputs. Cleared by user to disable all PWM outputs.

In H-bridge mode, HMODE = 1. See Table 65 to determine the PWM outputs.

Table 65. PWM Output Selection

PWMCOM1 MMR				PWM Outputs			
ENA	HOFF	POINV	DIR	PWM1	PWM2	PWMR3	PWM4
0	0	x	x	1	1	1	1
x	1	x	x	1	0	1	0
1	0	0	0	0	0	HS[1]	LS[1]
1	0	0	1	HS[1]	LS[1]	0	0
1	0	1	0	HS[1]	LS[1]	1	1
1	0	1	1	1	1	HS[1]	LS[1]

[1] HS = high side, LS = low side.

On power-up, PWMCON1 defaults to 0x12 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (see Table 66).

Table 66. Compare Register

Name	Address	Default Value	Access
PWM1COM1	0xFFFF0F84	0x00	R/W
PWM1COM2	0xFFFF0F88	0x00	R/W
PWM1COM3	0xFFFF0F8C	0x00	R/W
PWM2COM1	0xFFFF0F94	0x00	R/W
PWM2COM2	0xFFFF0F98	0x00	R/W
PWM2COM3	0xFFFF0F9C	0x00	R/W
PWM3COM1	0xFFFF0FA4	0x00	R/W
PWM3COM2	0xFFFF0FA8	0x00	R/W
PWM3COM3	0xFFFF0FAC	0x00	R/W

The PWM trip interrupt can be cleared by writing any value to the PWMICLR MMR. Note that when using the PWM trip interrupt, the PWM interrupt should be cleared before exiting the ISR. This prevents generation of multiple interrupts.

PWM CONVERT START CONTROL

The PWM can be configured to generate an ADC convert start signal after the active low side signal goes high. There is a programmable delay between when the low-side signal goes high and the convert start signal is generated.

This is controlled via the PWMCON2 MMR. If the delay selected is higher than the width of the PWM pulse, the interrupt remains low.

Table 67. PWMCON2 MMR Bit Designations

Bit	Value	Name	Description
7		CSEN	Set to 1 by the user to enable the PWM to generate a convert start signal. Cleared by user to disable the PWM convert start signal.
6:4		RSVD	Reserved. This bit should be set to 0 by the user.
3:0		CSD3	Convert Start Delay. Delays the convert start signal by a number of clock pulses.
		CSD2	
		CSD1	
		CSD0	
	0000		4 clock pulses.
	0001		8 clock pulses.
	0010		12 clock pulses.
	0011		16 clock pulses.
	0100		20 clock pulses.
	0101		24 clock pulses.
	0110		28 clock pulses.
	0111		32 clock pulses.
	1000		36 clock pulses.
	1001		40 clock pulses.
	1010		44 clock pulses.
	1011		48 clock pulses.
	1100		52 clock pulses.
	1101		56 clock pulses.
	1110		60 clock pulses.
	1111		64 clock pulses.

When calculating the time from the convert start delay to the start of an ADC conversion, the user needs to take account of internal delays. The example below shows the case for a delay of four clocks. One additional clock is required to pass the convert start signal to the ADC logic. Once the ADC logic receives the convert start signal an ADC conversion begins on the next ADC clock edge (see Figure 50).

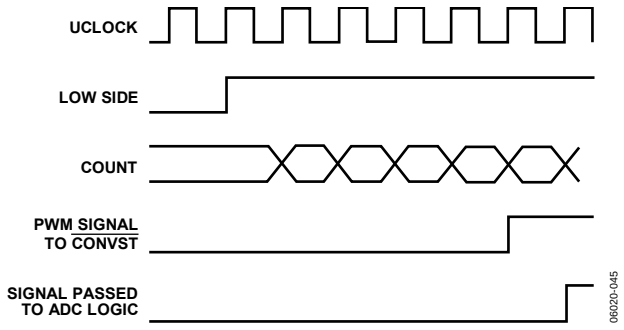

Figure 50. ADC Conversion

Quadrature Encoder

A quadrature encoder is used to determine both the speed and direction of a rotating shaft. In its most common form, there are two digital outputs, S1 and S2. As the shaft rotates, both S1 and S2 toggle; however, they are 90° out of phase. The leading output determines the direction of rotation. The time between each transition indicates the speed of rotation.

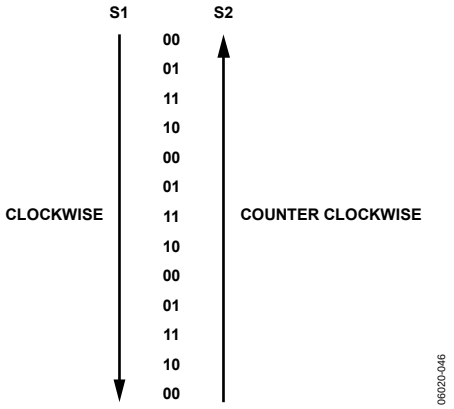

Figure 51. Quadrate Encoder Input Values

The quadrature encoder takes the incremental input shown in Figure 51 and increments or decrements a counter depending on the direction and speed of the rotating shaft.

On the ADuC7128/ADuC7129, the internal counter is clocked on the rising edge of the S1 input, and the S2 input indicates the direction of rotation/count. The counter increments when S2 is high and decrements when it is low.

In addition, if the software has prior knowledge of the direction of rotation, one input can be ignored (S2) and the other can act as a clock (S1).

For additional flexibility, all inputs can be internally inverted prior to use.

The quadrature encoder operates asynchronously from the system clock.

Input Filtering

Filtering can be applied to the S1 input by setting the FILTEN bit in QENCON. S1 normally acts as the clock to the counter; however, the filter can be used to ignore positive edges on S1 unless there has been a high or a low pulse on S2 between two positive edges on S1 (see Figure 52).

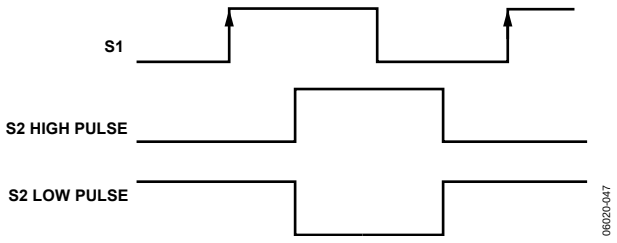

Figure 52. S1 Input Filtering

QENCLR Register

Name	Address	Default Value	Access
QENCLR	0xFFFF0F14	0x00000000	R/W

Writing any value to the QENCLR register clears the QENVAL register to 0x0000. The bits in this register are undefined.

QENSET Register

Name	Address	Default Value	Access
QENSET	0xFFFF0F18	0x00000000	R/W

Writing any value to the QENSET register loads the QENVAL register with the value in QENDAT. The bits in this register are undefined.

Note that the interrupt conditions are OR'ed together to form one interrupt to the interrupt controller. The interrupt service routine should check the QENSTA register to find out the cause of the interrupt.

- The S1 and S2 inputs appear as the QENS1 and QENS2 inputs in the GPIO list.
- The motor speed can be measured by using the capture facility in Timer0 or Timer1.
- An overflow of either timer can be checked by using an ISR or by checking IRQSIG.

The counter with the quadrature encoder is gray encoded to ensure reliable data transfer across clock boundaries. When an underflow or overflow occur, the count value does not jump to the other end of the scale; instead, the direction of count changes. When this happens, the value in QENDAT is subtracted from the value derived from the gray count.

When the value in QENDAT changes, the value read back from QENVAL changes. However, the gray encoded value does not change. This only occurs after an underflow or overflow. If the value in QENDAT changes, there must be a write to QENSET or QENCLR to ensure a valid number is read back from QENVAL.

GENERAL-PURPOSE I/O

The ADuC7128/ADuC7129 provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. In general, many of the GPIO pins have multiple functions (see Table 70). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ) and their drive capability is 1.6 mA. Note that a maximum of 20 GPIO can drive 1.6 mA at the same time. The following GPIOs have programmable pull-up: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports: Port 0 to Port 4. Each port is controlled by four or five MMRs, with x representing the port number.

GPxCON Register

Name	Address	Default Value	Access
GP0CON	0xFFFF0D00	0x00000000	R/W
GP1CON	0xFFFF0D04	0x00000000	R/W
GP2CON	0xFFFF0D08	0x00000000	R/W
GP3CON	0xFFFF0D0C	0x11111111	R/W
GP4CON	0xFFFF0D10	0x00000000	R/W

Note that the kernel changes P0.6 from its default configuration at reset ($\overline{\text{MRST}}$) to GPIO mode. If $\overline{\text{MRST}}$ is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if $\overline{\text{MRST}}$ is required for power-down, it can be reconfigured in GP0CON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7128/ADuC7129 enter a power-saving mode, the GPIO pins retain their state.

GPxCON is the Port x control register, and it selects the function of each pin of Port x, as described in Table 70.

Table 70. GPIO Pin Function Designations

Port	Pin	Configuration			
		00	01	10	11
0	P0.0	GPIO	CMP	MS0	PLAI[7]
	P0.1[1]	GPIO		BLE	-
	P0.2[1]	GPIO		BHE	
	P0.3	GPIO	$\overline{TRST}$	A16	ADC_{BUSY}
	P0.4	GPIO/IRQ0	$\overline{CONVST}$	MS1	PLAO[1]
	P0.5	GPIO/IRQ1	ADC_{BUSY}	PLM_COMP	PLAO[2]
	P0.6	GPIO/T1	$\overline{MRST}$	AE	PLAO[3]
	P0.7	GPIO	ECLK/XCLK[2]	SIN0	PLAO[4]
1	P1.0	GPIO/T1	SIN0	SCL0	PLAI[0]
	P1.1	GPIO	SOUT0	SDA0	PLAI[1]
	P1.2	GPIO	RTS0	SCL1	PLAI[2]
	P1.3	GPIO	CTS0	SDA1	PLAI[3]
	P1.4	GPIO/IRQ2	RI0	CLK	PLAI[4]
	P1.5	GPIO/IRQ3	DCD0	MISO	PLAI[5]
	P1.6	GPIO	DSR0	MOSI	PLAI[6]
	P1.7	GPIO	DTR0	CSL	PLAO[0]
2	P2.0	GPIO	SYNC	SOUT	PLAO[5]
	P2.1[1]	GPIO		WS	PLAO[6]
	P2.2[1]	GPIO	RTS1	RS	PLAO[7]
	P2.3[1]	GPIO	CTS1	AE	
	P2.4[1]	GPIO	RI1	MS0	
	P2.5[1]	GPIO	DCD1	MS1	
	P2.6[1]	GPIO	DSR1	MS2	
	P2.7[1]	GPIO	DTR1	MS3	
3	P3.0	GPIO	PWM1	AD0	PLAI[8]
	P3.1	GPIO	PWM2	AD1	PLAI[9]
	P3.2	GPIO	PWM3	AD2	PLAI[10]
	P3.3	GPIO	PWM4	AD3	PLAI[11]
	P3.4	GPIO	PWM5	AD4	PLAI[12]
	P3.5	GPIO	PWM6	AD5	PLAI[13]
	P3.6[1]	GPIO	PWM1	AD6	PLAI[14]
	P3.7[1]	GPIO	PWM3	AD7	PLAI[15]
4	P4.0	GPIO	QENS1	AD8	PLAO[8]
	P4.1	GPIO	QENS2	AD9	PLAO[9]
	P4.2	GPIO	RSVD	AD10	PLAO[10]
	P4.3	GPIO	Trip (Shutdown)	AD11	PLAO[11]
	P4.4	GPIO	PLMIN	AD12	PLAO[12]
	P4.5	GPIO	PLMOUT	AD13	PLAO[13]
	P4.6	GPIO	SIN1	AD14	PLAO[14]
	P4.7	GPIO	SOUT1	AD15	PLAO[15]

[1] Available only on the 80-lead ADuC7129.
[2] When configured in Mode 1, PO.7 is ECLK by default, or core clock output. To configure it as a clock ouput, the MDCLK bits in PLLCON must be set to 11.

Table 71. GPxCON MMR Bit Designations

Bit	Description
31:30	Reserved
29:28	Select function of Px.7 pin
27:26	Reserved
25:24	Select function of Px.6 pin
23:22	Reserved
21:20	Select function of Px.5 pin
19:18	Reserved
17:16	Select function of Px.4 pin
15:14	Reserved
13:12	Select function of Px.3 pin
11:10	Reserved
9:8	Select function of Px.2 pin
7:6	Reserved
5:4	Select function of Px.1 pin
3:2	Reserved
1:0	Select function of Px.0 pin

GPxPAR Register

Name	Address	Default Value	Access
GP0PAR	0xFFFF0D2C	0x20000000	R/W
GP1PAR	0xFFFF0D3C	0x00000000	R/W
GP3PAR	0xFFFF0D5C	0x00222222	R/W
GP4PAR	0xFFFF0D6C	0x00000000	R/W

GPxPAR programs the parameters for Port 0, Port 1, Port 3, and Port 4. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 72. GPxPAR MMR Bit Designations

Bit	Description
31:29	Reserved
28	Pull-up disable Px.7 pin
27:25	Reserved
24	Pull-up disable Px.6 pin
23:21	Reserved
20	Pull-up disable Px.5 pin
19:17	Reserved
16	Pull-up disable Px.4 pin
15:13	Reserved
12	Pull-up disable Px.3 pin
11:9	Reserved
8	Pull-up disable Px.2 pin
7:5	Reserved
4	Pull-up disable Px.1 pin
3:1	Reserved
0	Pull-up disable Px.0 pin

SPIRX Register

Name	Address	Default Value	Access
SPIRX	0xFFFF0A04	0x00	R

SPIRX is an 8-bit read-only receive register.

SPITX Register

Name	Address	Default Value	Access
SPITX	0xFFFF0A08	0x00	W

SPITX is an 8-bit write-only transmit register.

SPIDIV Register

Name	Address	Default Value	Access
SPIDIV	0xFFFF0A0C	0x1B	R/W

SPIDIV is an 8-bit serial clock divider register.

SPICON Register

Name	Address	Default Value	Access
SPICON	0xFFFF0A10	0x0000	R/W

SPICON is a 16-bit control register.

Table 91. SPICON MMR Bit Designations

Bit	Description
15:13	Reserved.
12	Continuous Transfer Enable. Set by user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the TX register. $\overline{CS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until TX is empty. Cleared by user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period.
11	Loopback Enable. Set by user to connect MISO to MOSI and test software. Cleared by user to be in normal mode.
10	Slave Output Enable. Set by user to enable the slave output. Cleared by user to disable slave output.
9	Slave Select Input Enable. Set by user in master mode to enable the output.
8	SPIRX Overflow Overwrite Enable. Set by user, the valid data in the RX register is overwritten by the new serial byte received. Cleared by user, the new serial byte received is discarded.
7	SPITX Underflow Mode. Set by user to transmit 0. Cleared by user to transmit the previous data.
6	Transfer and Interrupt Mode (Master Mode). Set by user to initiate transfer with a write to the SPITX register. Interrupt occurs when TX is empty. Cleared by user to initiate transfer with a read of the SPIRX register. Interrupt occurs when RX is full.
5	LSB First Transfer Enable Bit. Set by user, the LSB is transmitted first. Cleared by user, the MSB is transmitted first.
4	Reserved. Should be set to 0.
3	Serial Clock Polarity Mode Bit. Set by user, the serial clock idles high. Cleared by user, the serial clock idles low.
2	Serial Clock Phase Mode Bit. Set by user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by user, the serial clock pulses at the end of each serial bit transfer.
1	Master Mode Enable Bit. Set by user to enable master mode. Cleared by user to enable slave mode.
0	SPI Enable Bit. Set by user to enable the SPI. Cleared to disable the SPI.

Table 113. T2CON MMR Bit Designations

Bit	Value	Description
31:11		Reserved.
10:9		Clock Source Select.
	00	Core Clock (Default).
	01	Internal 32.768 kHz Oscillator.
	10	External 32.768 kHz Watch Crystal.
	11	External 32.768 kHz Watch Crystal.
8		Count Up. Set by user for Timer2 to count up. Cleared by user for Timer2 to count down (default).
7		Timer2 Enable Bit. Set by user to enable Timer2. Cleared by user to disable Timer2 (default).
6		Timer2 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256. This setting should be used in conjunction with Timer2 formats 1,0 and 1,1.
	1111	Source Clock/32,768.

Table 117. T4CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved. Set by user to 0.
17		Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12		Event Select Range, 0 to 31. The events are as described in the Timers section.
11:9		Clock Select.
	000	Core Clock (Default).
	001	32.768 kHz Oscillator.
	010	P4.6.
	011	P4.7.
8		Count Up. Set by user for Timer4 to count up. Cleared by user for Timer4 to count down (default).
7		Timer4 Enable Bit. Set by user to enable Timer4. Cleared by user to disable Timer4 (default).
6		Timer4 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256.
	1111	Source Clock/32,768.

The XMxPAR are registers that define the protocol used for accessing the external memory for each memory region.

Table 121. XMxPAR MMR Bit Designations

Bit	Description
15	Enable Byte Write Strobe. This bit is only used for two, 8-bit memory sharing the same memory region. Set by user to gate the AD0 output with the WS output. This allows byte write capability without using $\overline{BHE}$ and $\overline{BLE}$ signals. Cleared by user to use $\overline{BHE}$ and $\overline{BLE}$ signals.
14:12	Number of Wait States on the Address Latch Enable Strobe.
11	Reserved.
10	Extra Address Hold Time. Set by the user to disable extra hold time. Cleared by the user to enable one clock cycle of hold on the address in read and write.
9	Extra Bus Transition Time on Read. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the read select ($\overline{RS}$).
8	Extra Bus Transition Time on Write. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the write select ($\overline{WS}$).
7:4	Number of Write Wait States. Select the number of wait states added to the length of the $\overline{WS}$ pulse. 0x0 is 1 clock cycle; 0xF is 16 clock cycles (default value).
3:0	Number of Read Wait States. Select the number of wait states added to the length of the $\overline{RS}$ pulse. 0x0 is 1 clock cycle; 0xF is 16 clock cycles (default value).

TIMING DIAGRAMS

Figure 62 through Figure 65 show the timing for a read cycle (see Figure 62), a read cycle with address hold and bus turn cycles (see Figure 63), a write cycle with address hold and write hold cycles (see Figure 64), and a write cycle with wait states (see Figure 65).

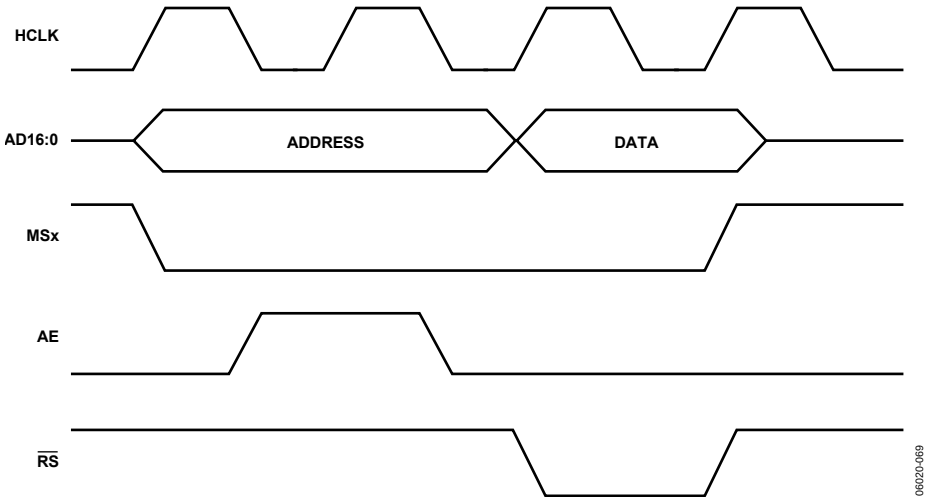

Figure 62. External Memory Read Cycle

DEVELOPMENT TOOLS

An entry level, low cost development system is available for the ADuC7128/ADuC7129. This system consists of the following PC-based (Windows® compatible) hardware and software development tools.

Hardware

- ADuC7128/ADuC7129 evaluation board
- Serial port programming cable
- JTAG emulator

Software

- Integrated development environment, incorporating assembler, compiler, and nonintrusive JTAG-based debugger
- Serial downloader software
- Example code

Miscellaneous

- CD-ROM documentation

IN-CIRCUIT SERIAL DOWNLOADER

The serial downloader is a Windows application that allows the user to serially download an assembled program to the on-chip program Flash/EE memory via the serial port on a standard PC.