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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	PLA, POR, PWM, PSM, Temp Sensor, WDT
Number of I/O	38
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7129bstz126

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 3.0 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz. All specifications T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and fADC/2
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity[3]		±0.7	±2.0	LSB	2.5 V internal reference 85°C to 125°C only
		±0.7	±1.5	LSB	2.5 V internal reference −40°C to +85°C
		±2.0		LSB	1.0 V external reference
Differential Nonlinearity[3]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		±0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[4]					
Offset Error			±5	LSB	
Offset Error Match		±1		LSB	
Gain Error			±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					F_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−80		dB	
Crosstalk Between Channel 12 and Channel 13		−60		dB	
ANALOG INPUT					
Input Voltage Ranges					
Differential Mode[5]			$V_{CM} \pm V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current			±15	µA	85°C to 125°C only
		±1	±3	µA	−40°C to +85°C
Input Capacitance		20		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±2.5	mV	Measured at T_A = 25°C
Reference Drop When DAC Enabled		9		mV	Reference drop when DAC enabled
Reference Temperature Coefficient		±40		ppm/°C	
Power Supply Rejection Ratio		80		dB	
Output Impedance		40		Ω	
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT[6]					
Input Voltage Range	0.625		AV_{DD}	V	
Input Impedance		38		kΩ	
DAC CHANNEL SPECIFICATIONS					
VDAC Output					R_L = 5 kΩ, C_L = 100 pF
Voltage Swing		$(0.33 \times V_{REF} \pm 0.2 \times V_{REF}) \times 1.33$			V_{REF} is the internal 2.5 V reference
I/V Output Resistance			7	Ω	V mode selected
Low-Pass Filter 3 dB Point		1		MHz	2-pole at 1.5 MHz and 2 MHz
Resolution		10		Bits	

Line Driver Load

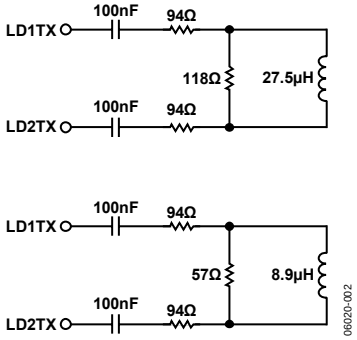


Figure 2. Line Driver Load Minimum (Top) and Maximum (Bottom)

TIMING SPECIFICATIONS

Table 2. External Memory Write Cycle

Parameter	Min	Typ	Max	Unit
CLK		UCLK		
$t_{MS\_AFTER\_CLKH}$	0		4	ns
$t_{ADDR\_AFTER\_CLKH}$	4		8	ns
$t_{AE\_H\_AFTER\_MS}$		½ CLK		
t_{AE}		(XMxPAR[14:12] + 1) × CLK		
$t_{HOLD\_ADDR\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10]) × CLK		
$t_{HOLD\_ADDR\_BEFORE\_WR\_L}$		(!XMxPAR[8]) × CLK		
$t_{WR\_L\_AFTER\_AE\_L}$		½ CLK + (!XMxPAR[10] + !XMxPAR[8]) × CLK		
$t_{DATA\_AFTER\_WR\_L}$	8		12	ns
t_{WR}		(XMxPAR[7:4] + 1) × CLK		
$t_{WR\_H\_AFTER\_CLKH}$	0		4	ns
$t_{HOLD\_DATA\_AFTER\_WR\_H}$		(!XMxPAR[8]) × CLK		
$t_{BEN\_AFTER\_AE\_L}$		½ CLK		
$t_{RELEASE\_MS\_AFTER\_WR\_H}$		(!XMxPAR[8] + 1) × CLK		

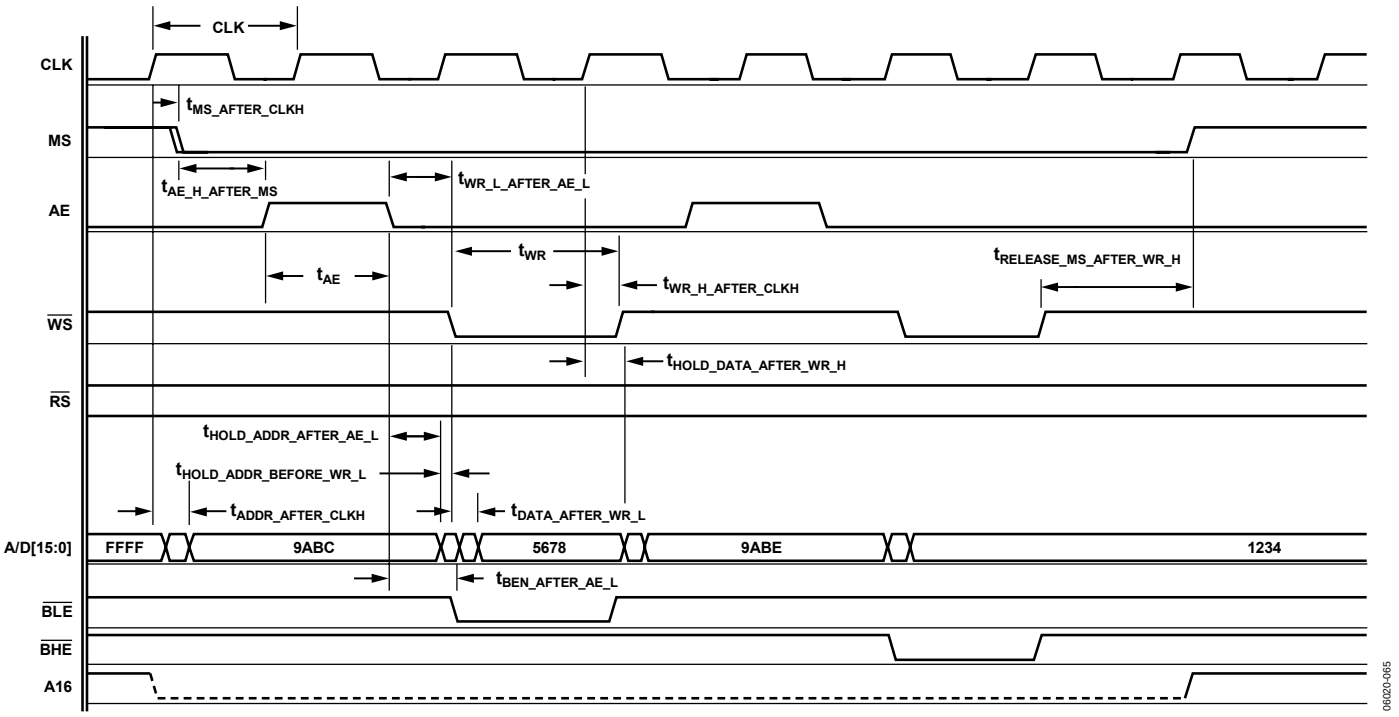


Figure 3. External Memory Write Cycle

Table 6. SPI Master Mode Timing (PHASE Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			2 × t_{HCLK} + 2 × t_{UCLK}	ns
t_{DOSU}	Data output setup before SCLOCK edge			75	ns
t_{DSU}	Data input setup time before SCLOCK edge[2]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[2]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLOCK rise time		5	12.5	ns
t_{SF}	SCLOCK fall time		5	12.5	ns

[1] t_{HCLK} depends on the clock divider or CD bits in the PLLCON MMR, $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

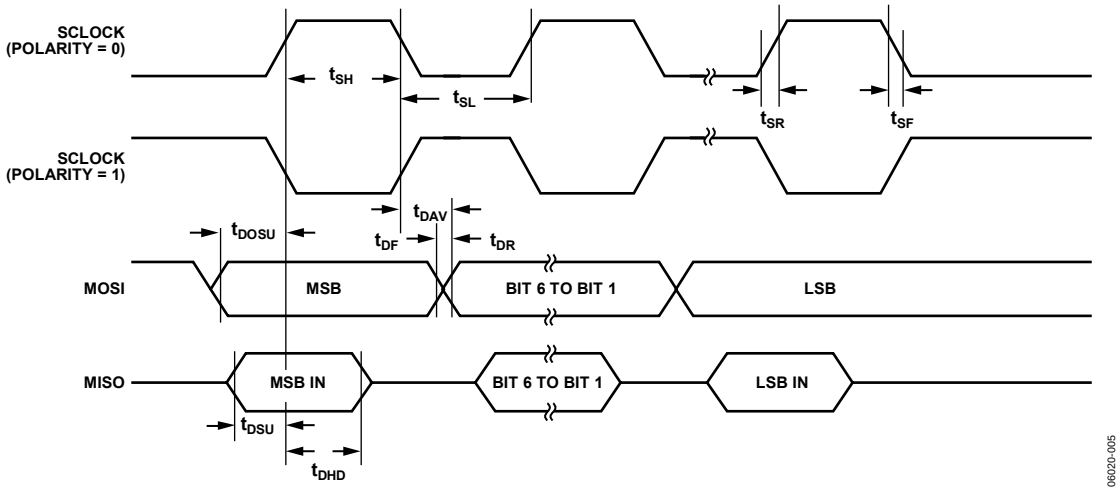


Figure 7. SPI Master Mode Timing (PHASE Mode = 0)

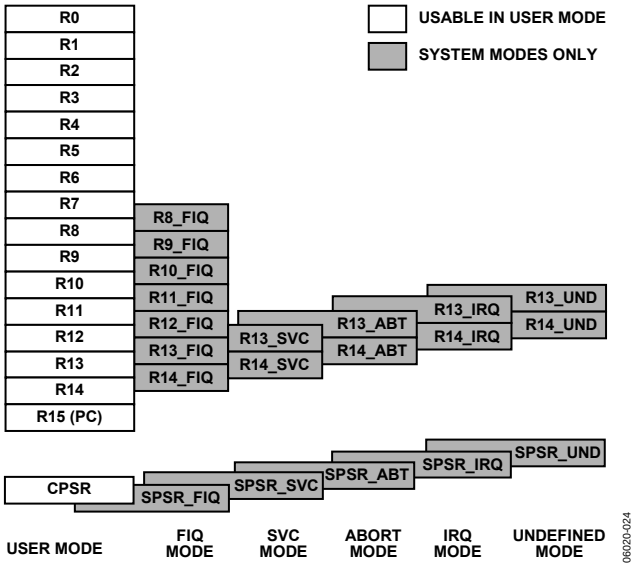


Figure 28. Register Organization

INTERRUPT LATENCY

The worst case latency for an FIQ consists of the following:

- The longest time the request can take to pass through the synchronizer
- The time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers, including the PC
- The time for the data abort entry
- The time for FIQ entry

At the end of this time, the ARM7TDMI executes the instruction at Address 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum IRQ latency calculation is similar, but it must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used; some compilers have an option to compile without using this command. Another option is to run the part in Thumb mode, where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is five cycles. It consists of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, that is, when executing interrupt service routines.

Table 41. FEExSTA MMR Bit Designations

Bit	Description
15:6	Reserved.
5	Reserved.
4	Reserved.
3	Flash/EE Interrupt Status Bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEExMOD register is set. Cleared when reading FEExSTA register.
2	Flash/EE Controller Busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command Fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading FEExSTA register.
0	Command Complete. Set by MicroConverter when a command is complete. Cleared automatically when reading FEExSTA register.

Table 42. FEExMOD MMR Bit Designations

Bit	Description
7:5	Reserved.
4	Flash/EE Interrupt Enable. Set by user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by user to disable the Flash/EE interrupt
3	Erase/Write Command Protection. Set by user to enable the erase and write commands. Cleared to protect the Flash/EE memory against erase/write command.
2	Reserved. Should always be set to 0 by the user.
1:0	Flash/EE Wait States. Both Flash/EE blocks must have the same wait state value for any change to take effect.

Table 43. Command Codes in FEExCON

Code	Command	Description
0x00[1]	Null	Idle State.
0x01[1]	Single read	Load FEExDAT with the 16-bit data indexed by FEExADR.
0x02[1]	Single write	Write FEExDAT at the address pointed by FEExADR. This operation takes 50 µs.
0x03[1]	Erase/Write	Erase the page indexed by FEExADR and write FEExDAT at the location pointed by FEExADR. This operation takes 20 ms.
0x04[1]	Single verify	Compare the contents of the location pointed by FEExADR to the data in FEExDAT. The result of the comparison is returned in FEExSTA Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEExADR.
0x06[1]	Mass erase	Erase user space. The 2 kB of kernel are protected in Block 0. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Gives a signature of the 64 kB of Flash/EE in the 24-bit FEExSIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can be run only once. The value of FEExPRO is saved and can be removed only with a mass erase (0x06) or with the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No Operation, Interrupt Generated.

[1] The FEExCON register always reads 0x07 immediately after execution of any of these commands.

Table 44. FEE0PRO and FEE0HID MMR Bit Designations

Bit	Description
31	Read Protection. Cleared by user to protect Block 0. Set by user to allow reading Block 0.
30:0	Write Protection for Page 123 to Page 120, for Page 119 to Page 116, and for Page 3 to Page 0. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.

Table 45. FEE1PRO and FEE1HID MMR Bit Designations

Bit	Description
31	Read Protection. Cleared by user to protect Block 1. Set by user to allow reading Block 1.
30	Write Protection for Page 127 to Page 120. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.
31:0	Write Protection for Page 119 to Page 116 and for Page 3 to Page 0. Cleared by user to protect the pages in writing. Set by user to allow writing the pages.

EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns and a clock cycle is 22 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE), one cycle to execute the instruction and two cycles to get the 32-bit data from Flash/EE. A control flow instruction, such as a branch instruction, takes one cycle to fetch, but it also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 23 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD bit = 0). In addition, some dead times are needed before accessing data for any value of CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter and then four cycles are needed to fill the pipeline. A data processing instruction involving only core registers doesn't require any extra clock cycles, but if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data and two cycles to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 46.

Table 46. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N	$2 \times N$	N
STR	2/1	1	2×20 µs	1
STRH	2/1	1	20 µs	1
STRM/POP	2/1	N	$2 \times N \times 20$ µs	N

With $1 < N \leq 16$, N is the number of bytes of data to load or store in the multiple load/store instruction. The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles plus 40 µs.

DDSFRQ Register

Name	Address	Default Value	Access
DDSFRQ	0xFFFF0694	0x00000000	R/W

Table 54. DDSFRQ MMR Bit Designations

Bit	Description
31:0	Frequency select word (FSW)

The DDS frequency is controlled via the DDSFRQ MMR. This MMR contains a 32-bit word (FSW) that controls the frequency according to the following formula:

$$Frequency = \frac{FSW \times 20.8896 \text{ MHz}}{2^{32}}$$

DDSPHS Register

Name	Address	Default Value	Access
DDSPHS	0xFFFF0698	0x00000000	R/W

Table 55. DDSPHS MMR Bit Designations

Bit	Description
31:12	Reserved
11:0	Phase

The DDS phase offset is controlled via the DDSPHS MMR. This MMR contains a 12-bit value that controls the phase of the DDS output according to the following formula:

$$Phase\ Offset = \frac{2 \times \pi \times Phase}{2^{12}}$$

POWER SUPPLY MONITOR

The power supply monitor on the ADuC7128/ADuC7129 indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register (see Table 56). If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is cleared immediately once CMP goes high. Note that if the interrupt generated is exited before CMP goes high (IOV_{DD} is above the trip point), no further interrupts are generated until CMP returns high. The user should ensure that code execution remains within the ISR until CMP returns high.

This monitor function allows the user to save working registers to avoid possible data loss due to the low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level has been established.

The PSM does not operate correctly when using JTAG debug. It should be disabled in JTAG debug mode.

COMPARATOR

The ADuC7128/ADuC7129 integrate an uncommitted voltage comparator. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or the internal reference. The output of the comparator can be configured to generate a system interrupt, can be routed directly to the programmable logic array, can start an ADC conversion, or can be on an external pin, CMP_{OUT}.

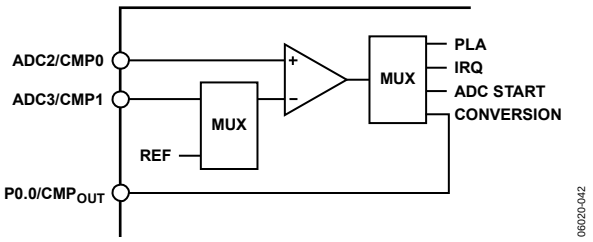


Figure 46. Comparator

Hysteresis

Figure 47 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

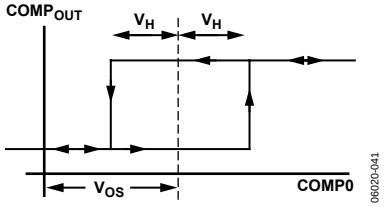


Figure 47. Comparator Hysteresis Transfer Function

Table 56. PSMCON MMR Bit Designations

Bit	Name	Description
3	CMP	Comparator Bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates the IOV_{DD} supply is above its selected trip point or the PSM is in power-down mode. Read 0 indicates the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip Point Selection Bit. 0 = 2.79 V 1 = 3.07 V
1	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.
0	PSMI	Power Supply Monitor Interrupt Bit. This bit is set high by the MicroConverter if CMP is low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. Once CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A write of 0 has no effect. There is no timeout delay. PSMI can be cleared immediately once CMP goes high.

Table 67. PWMCON2 MMR Bit Designations

Bit	Value	Name	Description
7		CSEN	Set to 1 by the user to enable the PWM to generate a convert start signal. Cleared by user to disable the PWM convert start signal.
6:4		RSVD	Reserved. This bit should be set to 0 by the user.
3:0		CSD3	Convert Start Delay. Delays the convert start signal by a number of clock pulses.
		CSD2	
		CSD1	
		CSD0	
	0000		4 clock pulses.
	0001		8 clock pulses.
	0010		12 clock pulses.
	0011		16 clock pulses.
	0100		20 clock pulses.
	0101		24 clock pulses.
	0110		28 clock pulses.
	0111		32 clock pulses.
	1000		36 clock pulses.
	1001		40 clock pulses.
	1010		44 clock pulses.
	1011		48 clock pulses.
	1100		52 clock pulses.
	1101		56 clock pulses.
	1110		60 clock pulses.
	1111		64 clock pulses.

When calculating the time from the convert start delay to the start of an ADC conversion, the user needs to take account of internal delays. The example below shows the case for a delay of four clocks. One additional clock is required to pass the convert start signal to the ADC logic. Once the ADC logic receives the convert start signal an ADC conversion begins on the next ADC clock edge (see Figure 50).

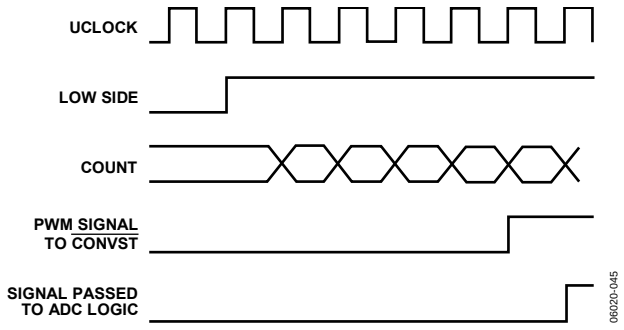


Figure 50. ADC Conversion

Quadrature Encoder

A quadrature encoder is used to determine both the speed and direction of a rotating shaft. In its most common form, there are two digital outputs, S1 and S2. As the shaft rotates, both S1 and S2 toggle; however, they are 90° out of phase. The leading output determines the direction of rotation. The time between each transition indicates the speed of rotation.

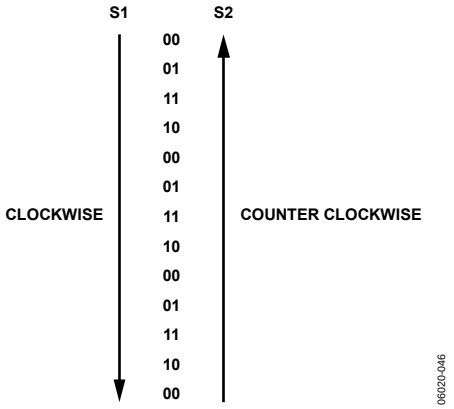


Figure 51. Quadrate Encoder Input Values

The quadrature encoder takes the incremental input shown in Figure 51 and increments or decrements a counter depending on the direction and speed of the rotating shaft.

On the ADuC7128/ADuC7129, the internal counter is clocked on the rising edge of the S1 input, and the S2 input indicates the direction of rotation/count. The counter increments when S2 is high and decrements when it is low.

In addition, if the software has prior knowledge of the direction of rotation, one input can be ignored (S2) and the other can act as a clock (S1).

For additional flexibility, all inputs can be internally inverted prior to use.

The quadrature encoder operates asynchronously from the system clock.

Input Filtering

Filtering can be applied to the S1 input by setting the FILTEN bit in QENCON. S1 normally acts as the clock to the counter; however, the filter can be used to ignore positive edges on S1 unless there has been a high or a low pulse on S2 between two positive edges on S1 (see Figure 52).

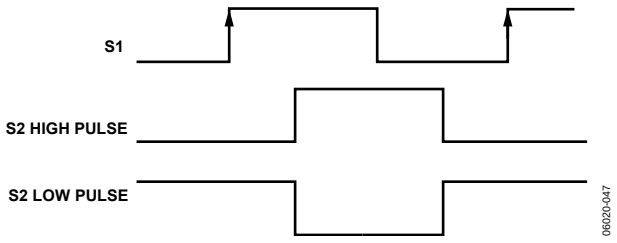


Figure 52. S1 Input Filtering

QENCLR Register

Name	Address	Default Value	Access
QENCLR	0xFFFF0F14	0x00000000	R/W

Writing any value to the QENCLR register clears the QENVAL register to 0x0000. The bits in this register are undefined.

QENSET Register

Name	Address	Default Value	Access
QENSET	0xFFFF0F18	0x00000000	R/W

Writing any value to the QENSET register loads the QENVAL register with the value in QENDAT. The bits in this register are undefined.

Note that the interrupt conditions are OR'ed together to form one interrupt to the interrupt controller. The interrupt service routine should check the QENSTA register to find out the cause of the interrupt.

- The S1 and S2 inputs appear as the QENS1 and QENS2 inputs in the GPIO list.
- The motor speed can be measured by using the capture facility in Timer0 or Timer1.
- An overflow of either timer can be checked by using an ISR or by checking IRQSIG.

The counter with the quadrature encoder is gray encoded to ensure reliable data transfer across clock boundaries. When an underflow or overflow occur, the count value does not jump to the other end of the scale; instead, the direction of count changes. When this happens, the value in QENDAT is subtracted from the value derived from the gray count.

When the value in QENDAT changes, the value read back from QENVAL changes. However, the gray encoded value does not change. This only occurs after an underflow or overflow. If the value in QENDAT changes, there must be a write to QENSET or QENCLR to ensure a valid number is read back from QENVAL.

GENERAL-PURPOSE I/O

The ADuC7128/ADuC7129 provide 40 general-purpose, bidirectional I/O (GPIO) pins. All I/O pins are 5 V tolerant, meaning that the GPIOs support an input voltage of 5 V. In general, many of the GPIO pins have multiple functions (see Table 70). By default, the GPIO pins are configured in GPIO mode.

All GPIO pins have an internal pull-up resistor (of about 100 kΩ) and their drive capability is 1.6 mA. Note that a maximum of 20 GPIO can drive 1.6 mA at the same time. The following GPIOs have programmable pull-up: P0.0, P0.4, P0.5, P0.6, P0.7, and the eight GPIOs of P1.

The 40 GPIOs are grouped in five ports: Port 0 to Port 4. Each port is controlled by four or five MMRs, with x representing the port number.

GPxCON Register

Name	Address	Default Value	Access
GP0CON	0xFFFF0D00	0x00000000	R/W
GP1CON	0xFFFF0D04	0x00000000	R/W
GP2CON	0xFFFF0D08	0x00000000	R/W
GP3CON	0xFFFF0D0C	0x11111111	R/W
GP4CON	0xFFFF0D10	0x00000000	R/W

Note that the kernel changes P0.6 from its default configuration at reset ($\overline{\text{MRST}}$) to GPIO mode. If $\overline{\text{MRST}}$ is used for external circuitry, an external pull-up resistor should be used to ensure that the level on P0.6 does not drop when the kernel switches mode. Otherwise, P0.6 goes low for the reset period. For example, if $\overline{\text{MRST}}$ is required for power-down, it can be reconfigured in GP0CON MMR.

The input level of any GPIO can be read at any time in the GPxDAT MMR, even when the pin is configured in a mode other than GPIO. The PLA input is always active.

When the ADuC7128/ADuC7129 enter a power-saving mode, the GPIO pins retain their state.

GPxCON is the Port x control register, and it selects the function of each pin of Port x, as described in Table 70.

Table 82. COMxIEN0 MMR Bit Designations

Bit	Name	Description
7:4	RSVD	Reserved.
3	EDSSI	Modem Status Interrupt Enable Bit. Set by user to enable generation of an interrupt if any of COMxSTA1[3:0] are set. Cleared by user.
2	ELSI	RX Status Interrupt Enable Bit. Set by user to enable generation of an interrupt if any of COMxSTA0[3:1] are set. Cleared by user.
1	ETBEI	Enable Transmit Buffer Empty Interrupt. Set by user to enable interrupt when buffer is empty during a transmission. Cleared by user.
0	ERBFI	Enable Receive Buffer Full Interrupt. Set by user to enable interrupt when buffer is full during a reception. Cleared by user.

Table 83. COMxIID0 MMR Bit Designations

Bit 2:1 Status Bits	Bit 0 NINT	Priority	Definition	Clearing Operation
00	1		No Interrupt.	
11	0	1	Receive Line Status Interrupt.	Read COMxSTA0.
10	0	2	Receive Buffer Full Interrupt.	Read COMxRX.
01	0	3	Transmit Buffer Empty Interrupt.	Write data to COMxTX or read COMxIID0.
00	0	4	Modem Status Interrupt.	Read COMxSTA1.

Table 84. COMxCON1 MMR Bit Designations

Bit	Name	Description
7:5	RSVD	Reserved.
4	LOOPBACK	Loop Back. Set by user to enable loop-back mode. In loop-back mode, the SOUT is forced high. In addition, the modem signals are directly connected to the status inputs (RTS to CTS, DTR to DSR, OUT1 to RI, and OUT2 to DCD).
3		Reserved.
2		Reserved.
1	RTS	Request to Send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data Terminal Ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

Table 85. COMxSTA1 MMR Bit Designations

Bit	Name	Description
7	DCD	Data Carrier Detect.
6	RI	Ring Indicator.
5	DSR	Data Set Ready.
4	CTS	Clear to Send.
3	DDCD	Delta Data Carrier Detect. Set automatically if DCD changed state since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.
2	TERI	Trailing Edge Ring Indicator. Set if NRI changed from 0 to 1 since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.
1	DDSR	Delta Data Set Ready. Set automatically if DSR changed state since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.
0	DCTS	Delta Clear to Send. Set automatically if CTS changed state since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.

Table 86. COMxDIV2 MMR Bit Designations

Bit	Name	Description
15	FBEN	Fractional Baud Rate Generator Enable Bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate baud rate using the standard 450 UART baud rate generator.
14:13	RSVD	Reserved.
12:11	FBM[1 to 0]	M, if FBM = 0, M = 4 (see the Using the Fractional Divider section).
10:0	FBN[10 to 0]	N (see the Using the Fractional Divider section).

Network Addressable UART Mode

This mode allows connecting the MicroConverter on a 256-node serial network, either as a hardware single master or via software in a multimaster network. Bit 7 of COMxIEN1 (ENAM bit) must be set to enable UART in network-addressable mode.

Note that there is no parity check in this mode. The parity bit is used for address.

Network Addressable UART Register Definitions

Four additional registers, COMxIEN0, COMxIEN1, COMxIID1, and COMxADR are used only in network addressable UART mode.

In network address mode, the least significant bit of the COMxIEN1 register is the transmitted network address control bit. If set to 1, the device is transmitting an address. If cleared to 0, the device is transmitting data. For example, the following master-based code transmits the slave address followed by the data:

```
COM0IEN1  = 0xE7;                    //Setting ENAM, E9BT, E9BR, ETD, NABP
COM0TX = 0xA0;                       // Slave address is 0xA0
while(!(0x020==(COM0STA0 & 0x020))){} // wait for adr tx to finish.
COM0IEN1  = 0xE6;                    //  Clear NAB bit to indicate Data is coming
COM0TX = 0x55;                       // Tx data to slave: 0x55
```

I2CxFIF Register

Name	Address	Default Value	Access
I2C0FIF	0xFFFF084C	0x0000	R
I2C1FIF	0xFFFF094C	0x0000	R

I2CxFIF is a FIFO status register.

Table 95. I2C0FIF MMR Bit Designations

Bit	Value	Description
15:10		Reserved.
9		Master Transmit FIFO Flush. Set by user to flush the master Tx FIFO. Cleared automatically once the master Tx FIFO is flushed. This bit also flushes the slave receive FIFO.
8		Slave Transmit FIFO Flush. Set by user to flush the slave Tx FIFO. Cleared automatically once the slave Tx FIFO is flushed.
7:6		Master Rx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
5:4		Master Tx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
3:2		Slave Rx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO Full.
1:0		Slave Tx FIFO Status Bits.
	00	FIFO Empty.
	01	Byte Written to FIFO.
	10	1 Byte in FIFO.
	11	FIFO full.

PROGRAMMABLE LOGIC ARRAY (PLA)

The ADuC7128/ADuC7129 integrate a fully programmable logic array (PLA) that consists of two independent but interconnected PLA blocks. Each block consists of eight PLA elements, giving a total of 16 PLA elements.

A PLA element contains a two input look-up table that can be configured to generate any logic output function based on two inputs and a flip-flop as represented in Figure 54.

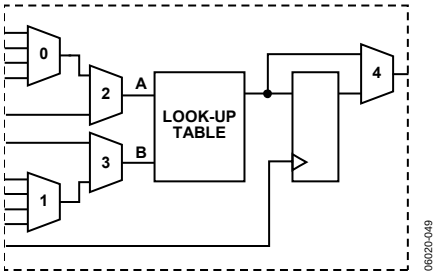


Figure 54. PLA Element

In total, 30 GPIO pins are available on the ADuC7128/ADuC7129 for the PLA. These include 16 input pins and 14 output pins. They need to be configured in the GPxCON register as PLA pins before using the PLA. Note that the comparator output is also included as one of the 16 input pins.

The PLA is configured via a set of user MMRs and the output(s) of the PLA can be routed to the internal interrupt system, to the $\overline{\text{CONVST}}$ signal of the ADC, to an MMR, or to any of the 16 PLA output pins.

The interconnection between the two blocks is supported by connecting the output of Element 7 of Block 1 fed back to the Input 0 of Mux 0 of Element 0 of Block 0, and the output of Element 7 of Block 0 is fed back to the Input 0 of Mux 0 of Element 0 of Block 1.

Table 96. Element Input/Output

PLA Block 0			PLA Block 1		
Element	**Input**	**Output**	**Element**	**Input**	**Output**
0	P1.0	P1.7	8	P3.0	P4.0
1	P1.1	P0.4	9	P3.1	P4.1
2	P1.2	P0.5	10	P3.2	P4.2
3	P1.3	P0.6	11	P3.3	P4.3
4	P1.4	P0.7	12	P3.4	P4.4
5	P1.5	P2.0	13	P3.5	P4.5
6	P1.6	P2.1	14	P3.6	P4.6
7	P0.0	P2.2	15	P3.7	P4.7

PLA MMRs Interface

The PLA peripheral interface consists on 21 MMRs, as shown in Table 97.

Table 97. PLA MMRs

Name	Description
PLAELMx	Element 0 to Element 15 Control Registers. Configure the input and output mux of each element, select the function in the look-up table, and bypass/use the flip-flop.
PLACLK	Clock Selection for the Flip-Flops of Block 0 and Clock Selection for the Flip-Flops of Block 1.
PLAIRQ	Enable IRQ0 and/or IRQ1. Select the source of the IRQ.
PLAADC	PLA Source from ADC Start Conversion Signal.
PLADIN	Data Input MMR for PLA.
PLAOUT	Data Output MMR for PLA. This register is always updated.

A PLA tool is provided in the development system to easily configure the PLA.

Table 98. PLAELMx MMR Bit Designations

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15	Description
31:11						Reserved.
10:9	00	Element 15	Element 0	Element 7	Element 8	Mux (0) Control. Select feedback source.
	01	Element 2	Element 2	Element 10	Element 10	
	10	Element 4	Element 4	Element 12	Element 12	
	11	Element 6	Element 6	Element 14	Element 14	
8:7	00	Element 1	Element 1	Element 9	Element 9	Mux (1) Control. Select feedback source.
	01	Element 3	Element 3	Element 11	Element 11	
	10	Element 5	Element 5	Element 13	Element 13	
	11	Element 7	Element 7	Element 15	Element 15	
6						Mux (2) Control. Set by user to select the output of Mux (0). Cleared by user to select the bit value from PLADIN.
5						Mux (3) Control. Set by user to select the input pin of the particular element. Cleared by user to select the output of Mux (1).
4:1						Look-Up Table Control.
	0000					0
	0001					NOR
	0010					B AND NOT A
	0011					NOT A
	0100					A AND NOT B
	0101					NOT B
	0110					EXOR
	0111					NAND
	1000					AND
	1001					EXNOR
	1010					B
	1011					NOT A OR B
	1100					A
	1101					A OR NOT B
	1110					OR
	1111					1
0						Mux (4) Control. Set by user to bypass the flip-flop. Cleared by user to select the flip-flop. Cleared by default.

TIMER4—GENERAL-PURPOSE TIMER

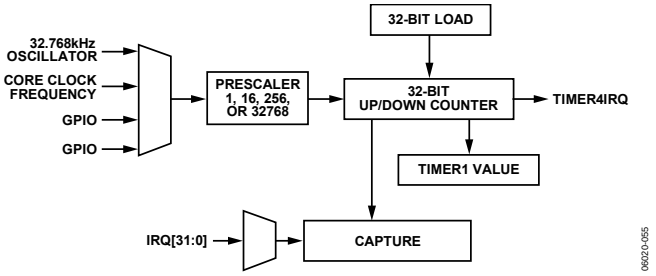


Figure 60. Timer4 Block Diagram

Timer4 is a 32-bit, general-purpose count down or count up timer with a programmable prescalar. The prescalar source can be the 32 kHz oscillator, the core clock, or one of two external GPIOs. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 42 ns when operating at CD zero, the core is operating at 41.78 MHz, and with a prescalar of 1 (ignoring external GPIO).

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer4 has a capture register (T4CAP), which can be triggered by a selected IRQ source initial assertion. Once triggered, the current timer value is copied to T4CAP, and the timer keeps running. This feature can be used to determine the assertion of an event with increased accuracy.

The Timer4 interface consists of five MMRs.

Table 116. Timer4 Interface MMRs

Name	Description
T4LD	A 32-bit register. Holds 32-bit unsigned integers.
T4VAL	A 32-bit register. Holds 32-bit unsigned integers. This register is read only.
T4CAP	A 32-bit register. Holds 32-bit unsigned integers. This register is read only.
T4ICLR	An 8-bit register. Writing any value to this register clears the Timer1 interrupt.
T4CON	The configuration MMR (see Table 117).

Note that if the part is in a low power mode and Timer4 is clocked from the GPIO or oscillator source, Timer4 continues to operate.

Timer4 reloads the value from T4LD either when Timer 4 overflows, or immediately when T4ICLR is written.

Timer4 Load Register

Name	Address	Default Value	Access
T4LD	0xFFFF0380	0x00000	R/W

T4LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer4 Clear Register

Name	Address	Default Value	Access
T4ICLR	0xFFFF038C	0x00	W

This 8-bit, write only MMR is written (with any value) by user code to refresh (reload) Timer4.

Timer4 Value Register

Name	Address	Default Value	Access
T4VAL	0xFFFF0384	0x0000	R

T4VAL is a 32-bit register that holds the current value of Timer4.

Timer4 Capture Register

Name	Address	Default Value	Access
T4CAP	0xFFFF0390	0x00	R

This is a 32-bit register that holds the 32-bit value captured by an enabled IRQ event.

Timer4 Control Register

Name	Address	Default Value	Access
T4CON	0xFFFF0388	0x0000	R/W

This 32-bit MMR configures the mode of operation of Timer4.

Table 117. T4CON MMR Bit Designations

Bit	Value	Description
31:18		Reserved. Set by user to 0.
17		Event Select Bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16:12		Event Select Range, 0 to 31. The events are as described in the Timers section.
11:9		Clock Select.
	000	Core Clock (Default).
	001	32.768 kHz Oscillator.
	010	P4.6.
	011	P4.7.
8		Count Up. Set by user for Timer4 to count up. Cleared by user for Timer4 to count down (default).
7		Timer4 Enable Bit. Set by user to enable Timer4. Cleared by user to disable Timer4 (default).
6		Timer4 Mode. Set by user to operate in periodic mode. Cleared by user to operate in free-running mode (default).
5:4		Format.
	00	Binary (Default).
	01	Reserved.
	10	Hours:Minutes:Seconds:Hundredths: 23 Hours to 0 Hours.
	11	Hours:Minutes:Seconds:Hundredths: 255 Hours to 0 Hours.
3:0		Prescaler.
	0000	Source Clock/1 (Default).
	0100	Source Clock/16.
	1000	Source Clock/256.
	1111	Source Clock/32,768.

The XMxPAR are registers that define the protocol used for accessing the external memory for each memory region.

Table 121. XMxPAR MMR Bit Designations

Bit	Description
15	Enable Byte Write Strobe. This bit is only used for two, 8-bit memory sharing the same memory region. Set by user to gate the AD0 output with the WS output. This allows byte write capability without using $\overline{BHE}$ and $\overline{BLE}$ signals. Cleared by user to use $\overline{BHE}$ and $\overline{BLE}$ signals.
14:12	Number of Wait States on the Address Latch Enable Strobe.
11	Reserved.
10	Extra Address Hold Time. Set by the user to disable extra hold time. Cleared by the user to enable one clock cycle of hold on the address in read and write.
9	Extra Bus Transition Time on Read. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the read select ($\overline{RS}$).
8	Extra Bus Transition Time on Write. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the write select ($\overline{WS}$).
7:4	Number of Write Wait States. Select the number of wait states added to the length of the $\overline{WS}$ pulse. 0x0 is 1 clock cycle; 0xF is 16 clock cycles (default value).
3:0	Number of Read Wait States. Select the number of wait states added to the length of the $\overline{RS}$ pulse. 0x0 is 1 clock cycle; 0xF is 16 clock cycles (default value).

TIMING DIAGRAMS

Figure 62 through Figure 65 show the timing for a read cycle (see Figure 62), a read cycle with address hold and bus turn cycles (see Figure 63), a write cycle with address hold and write hold cycles (see Figure 64), and a write cycle with wait states (see Figure 65).

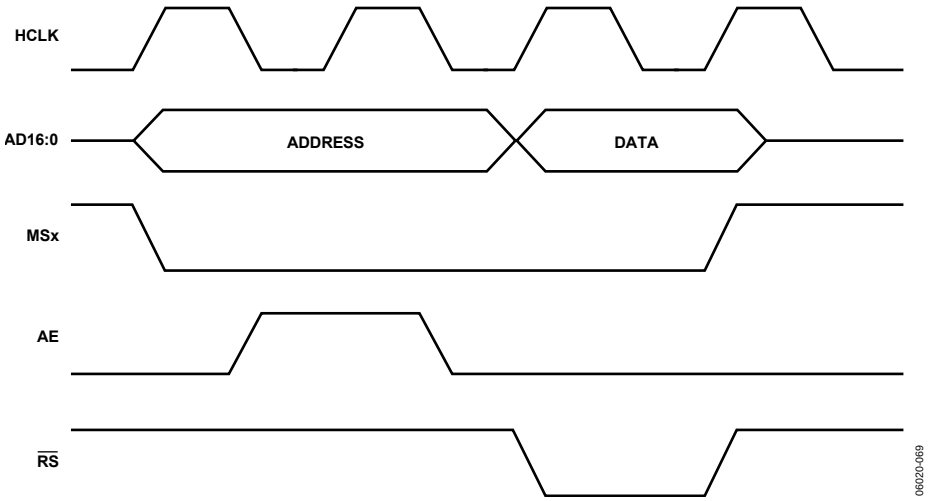


Figure 62. External Memory Read Cycle

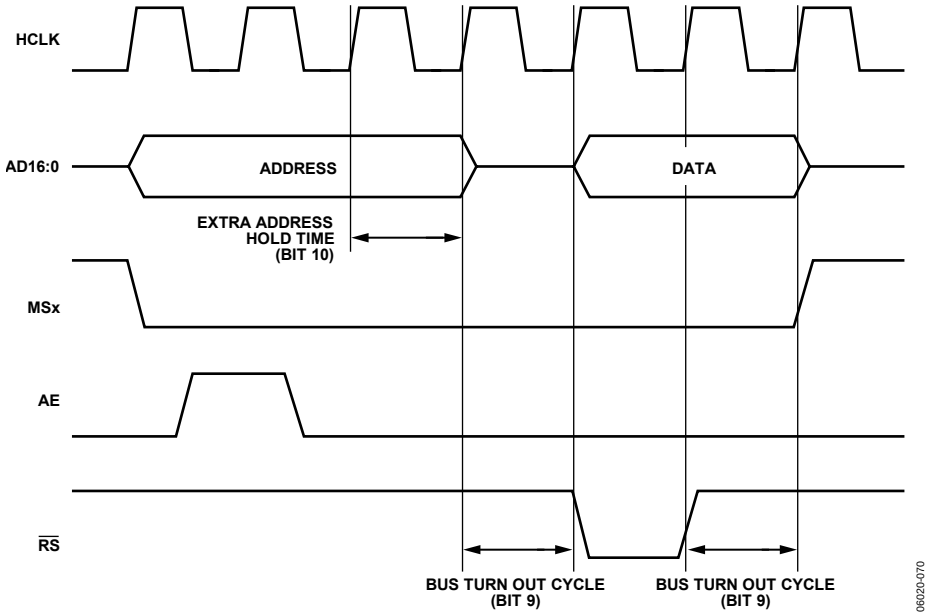


Figure 63. External Memory Read Cycle with Address Hold and Bus Turn Cycles

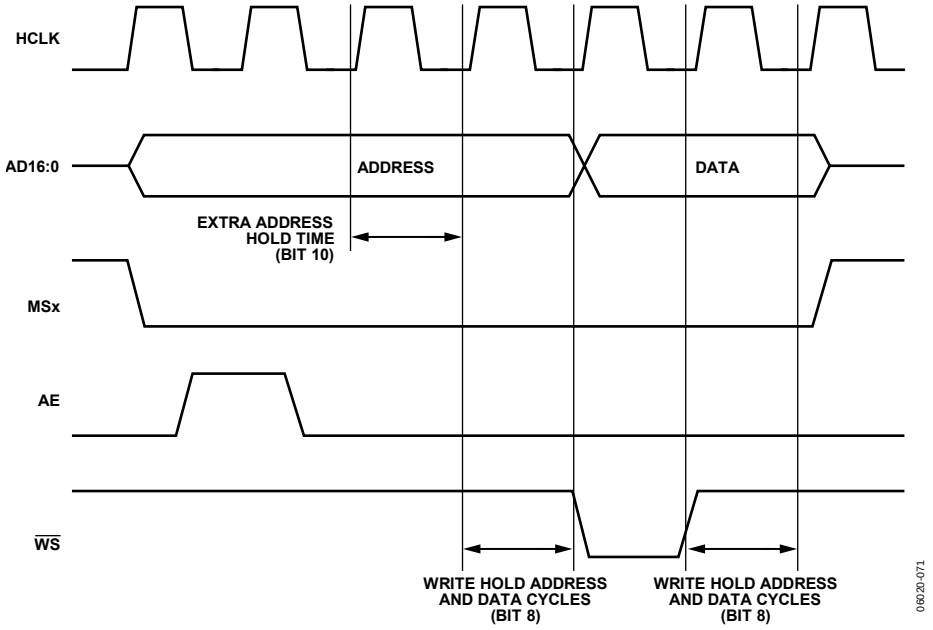


Figure 64. External Memory Write Cycle with Address Hold and Write Hold Cycles

OUTLINE DIMENSIONS

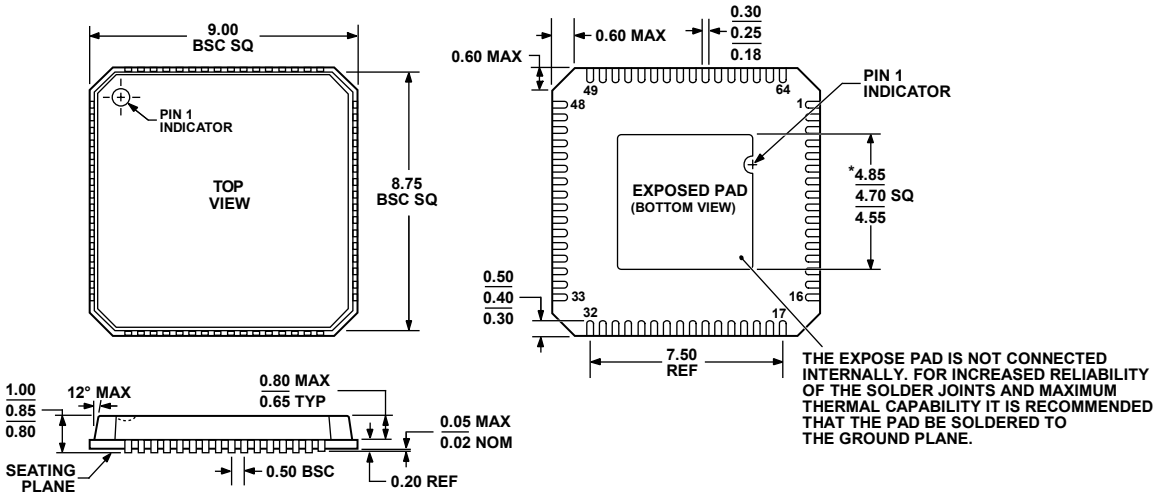


Figure 73. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

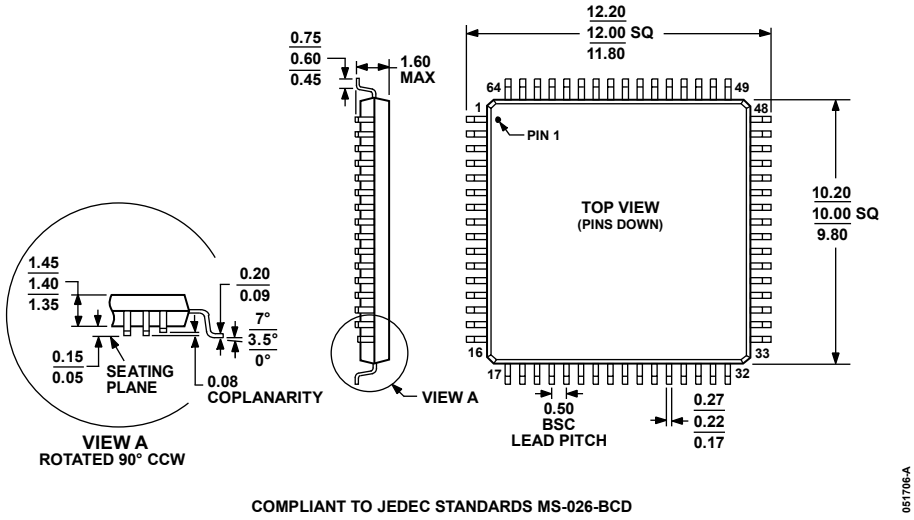
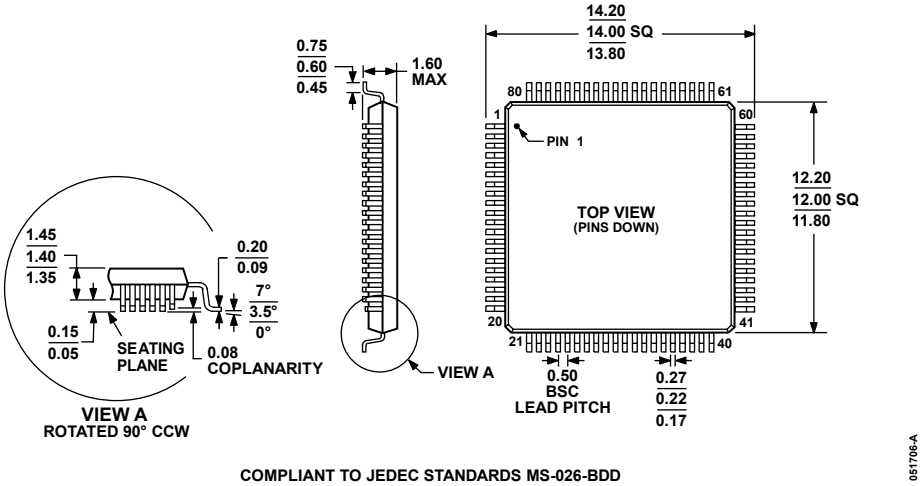


Figure 74. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BDD

Figure 75. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADUC7128BCPZ126[2]	−40°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
ADUC7128BCPZ126-RL[2]	−40°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
ADUC7128BSTZ126[2]	−40°C to +125°C	64-Lead LQFP	ST-64-2
ADUC7128BSTZ126-RL[2]	−40°C to +125°C	64-Lead LQFP	ST-64-2
ADUC7129BSTZ126[2]	−40°C to +125°C	80-Lead LQFP	ST-80-1
ADUC7129BSTZ126-RL[2]	−40°C to +125°C	80-Lead LQFP	ST-80-1
EVAL-ADUC7128QSPZ[2]		Evaluation Board	

[1] Reel quantities are 2,500 for the LFCSP and 1,000 for the LQFP.
[2] Z = RoHS Compliant Part.

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