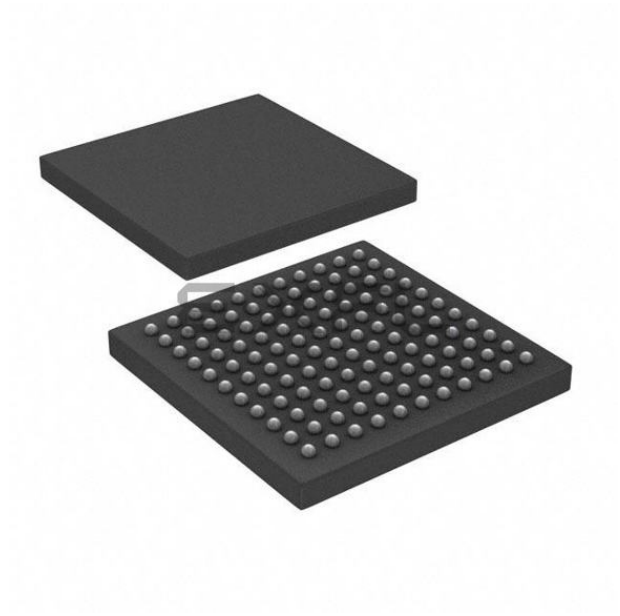

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	I²C, I²S, MMC/SD, SPI, UART, USB
Number of I/O	59
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb2014-bzxct

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See Pin Configurations for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
D6	C6	CVDDQ	I	CLKIN_32	CLKIN_32
C5	D8	CVDDQ	I	RESET#	RESET#
					I2C and JTAG
D9	D6	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL
D10	D2	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA
E7	F8	VIO5	I	TDI	TDI
C10	C2	VIO5	O	TDO	TDO
B11	C1	VIO5	I	TRST#	TRST#
E8	D5	VIO5	I	TMS	TMS
F6	D3	VIO5	I	TCK	TCK
D11	E8	VIO5	O	O[60]	Charger detect output
					Power
E10	E2	–	PWR	VBATT	–
B10	B1	–	PWR	VDD	–
–	A1	–	PWR	VDD	–
A1	C9	–	PWR	U3VSSQ	–
E11	E1	–	PWR	VBUS	–
D8	C4	–	PWR	VSS	–
H11	H1	–	PWR	VIO1	–
E2	K1	–	PWR	VSS	–
L9	L4	–	PWR	VIO1	–
G1	L5	–	PWR	VSS	–
–	L7	–	PWR	VIO1	–
–	L1	–	PWR	VSS	–
F1	J12	–	PWR	VIO2	–
G11	H12	–	PWR	VSS	–
	G12	–	PWR	VIO2	–
E3	C11	–	PWR	VIO3	–
L1	F12	–	PWR	VSS	–
B1	B11	–	PWR	VIO4	–
L6	A11	–	PWR	VSS	–
–	A12	–	PWR	VSS	–
B6	C7	–	PWR	CVDDQ	–
B5	C8	–	PWR	U3TXVDDQ	–
A2	C10	–	PWR	U3RXVDDQ	–
C11	D4	–	PWR	VIO5	–
L11	A3	–	PWR	VSS	–
A7	A5	–	PWR	AVDD	–
B7	A6	–	PWR	AVSS	–
C3	F4	–	PWR	VDD	–
B8	D1	–	PWR	VSS	–
E9	F5	–	PWR	VDD	–

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
B9	E4	–	PWR	VSS	–
F11	F6	–	PWR	VDD	–
–	E5	–	PWR	VSS	**GND**
–	F7	–	PWR	VDD	–
–	E6	–	PWR	VSS	GND
–	E7	–	PWR	VSS	GND
H1	G6	–	PWR	VDD	–
L7	D7	–	PWR	VDD	–
J11	L10	–	PWR	VDD	–
L5	L12	–	PWR	VDD	–
K4	H7	–	PWR	VSS	–
L3	G7	–	PWR	VSS	–
K3	L11	–	PWR	VSS	–
L2	G8	–	PWR	VSS	–
A8	G5	–	PWR	VSS	–
–	B4	–	–	NC	No Connect
A11	B2	–	–	NC	No Connect

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Ambient temperature with power supplied (Commercial) ..... 0 °C to +70 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} .....1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} .....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ .....1.25 V

DC input voltage to any input pin ..... V_{CC} + 0.3 V

DC voltage applied to outputs in high Z state ..... V_{CC} + 0.3 V

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current .....> 200 mA

Maximum output short-circuit current for all I/Os (cumulative).....–100 mA

Maximum output current per I/O (source or sink)..... .....20 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

Commercial ..... 0 °C to +70 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage .....1.15 V to 1.25 V

V_{BATT} supply voltage .....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage .....1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

DC Specifications

Table 8. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC – 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.

Host Processor Interface (P-Port) Timing

Asynchronous SRAM Timing

Figure 18. Non-multiplexed Asynchronous SRAM Read Timing

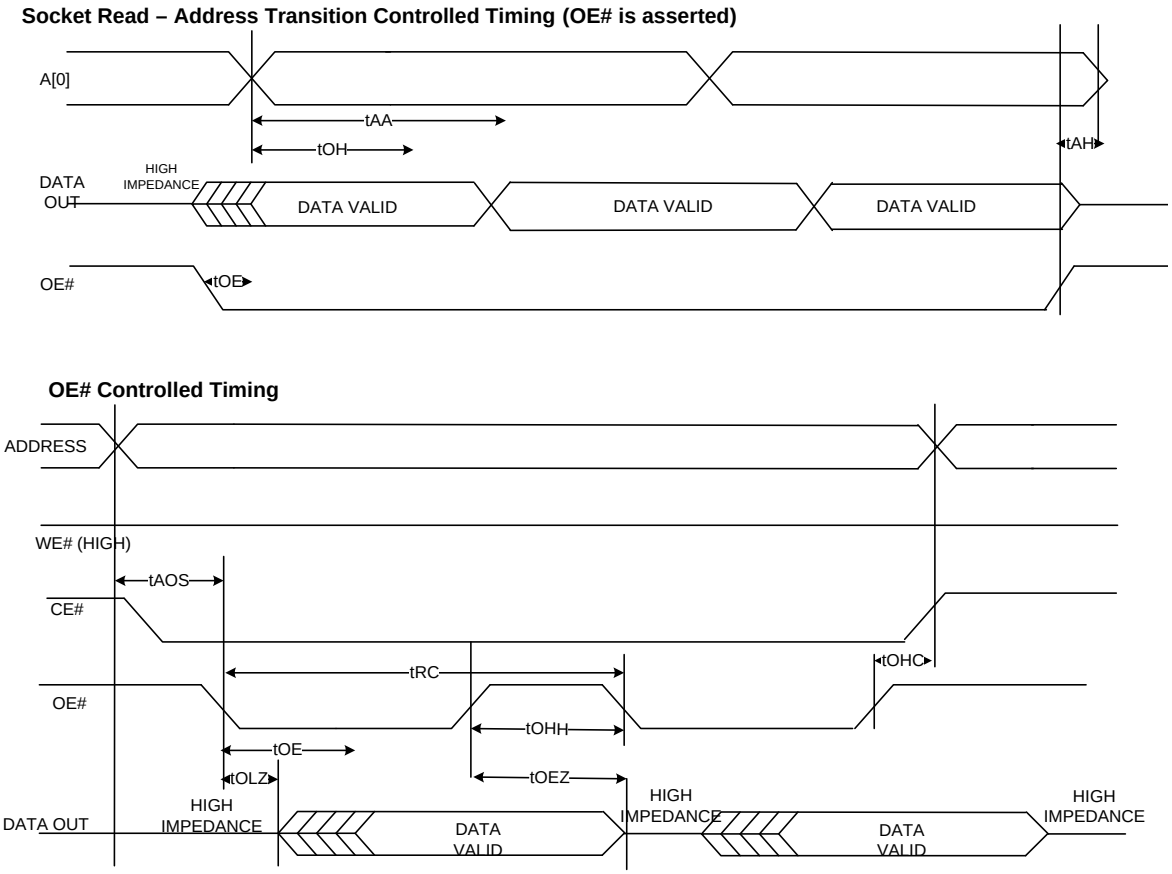
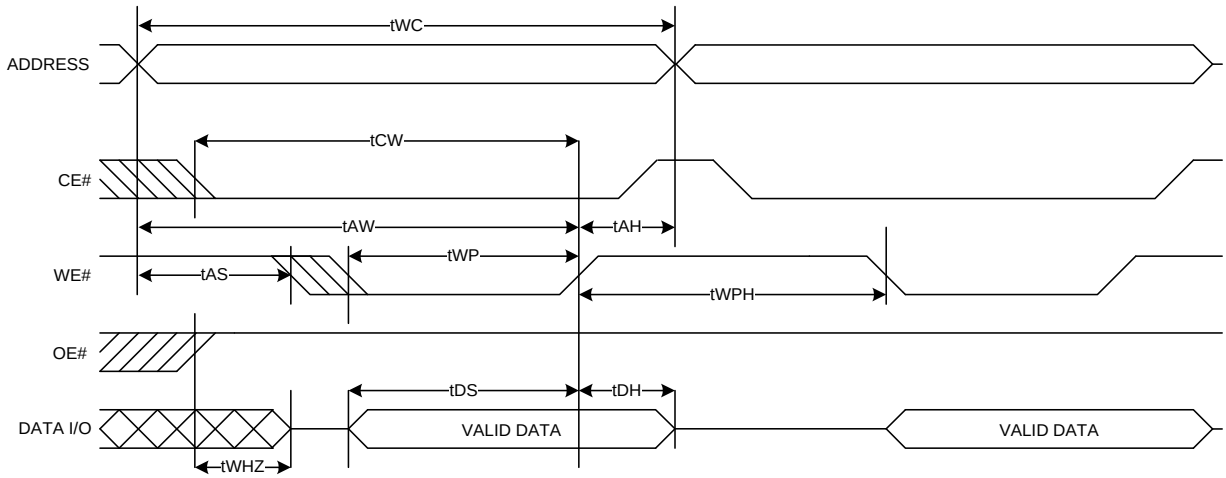


Figure 19. Non-multiplexed Asynchronous SRAM Write Timing (WE# and CE# Controlled)

Write Cycle 1 WE# Controlled, OE# High During Write



Write Cycle 2 CE# Controlled, OE# High During Write

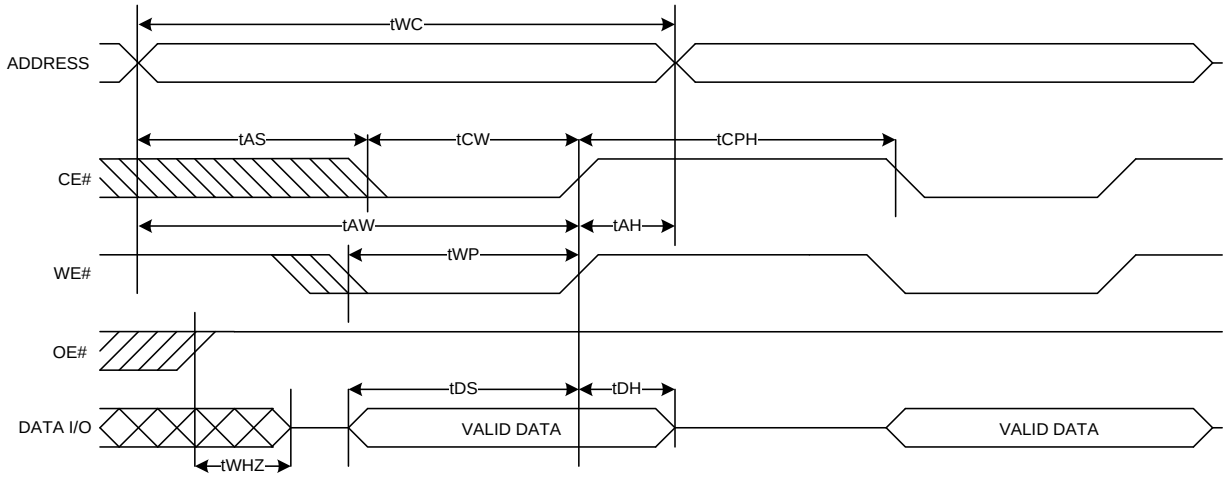
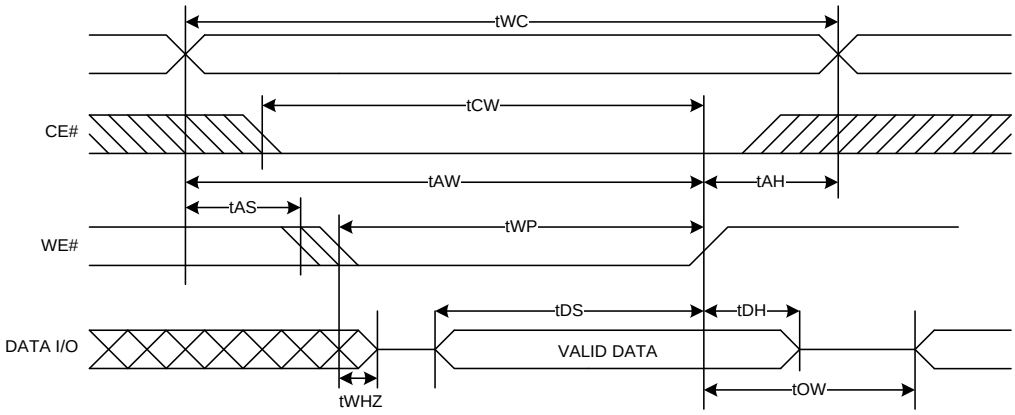


Figure 20. Non-multiplexed Asynchronous SRAM Write Timing (WE# controlled, OE# LOW)

Write Cycle 3 WE# Controlled. OE# Low



Note: tWP must be adjusted such that tWP > tWHZ + tDS

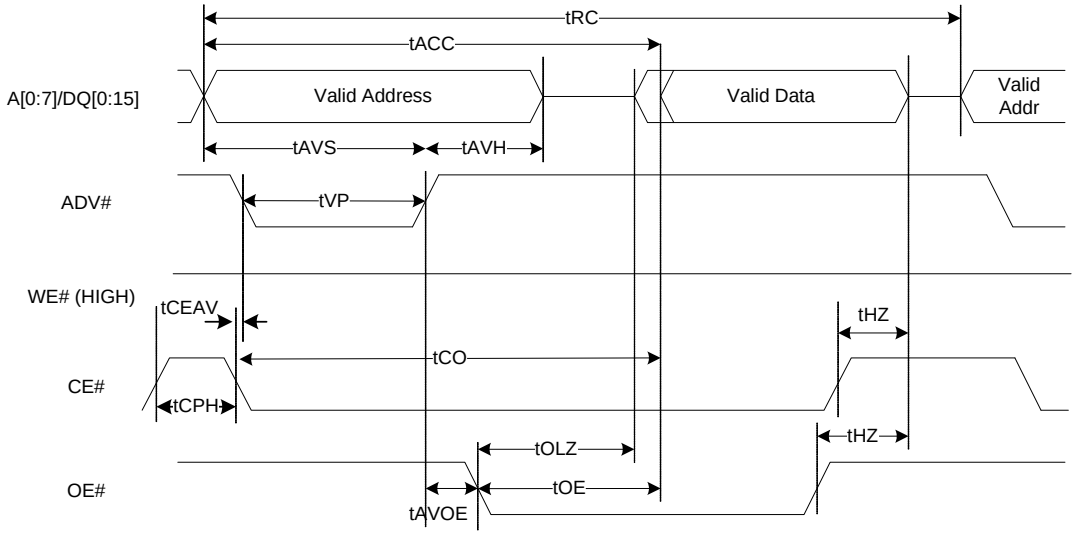
Table 13. Asynchronous SRAM Timing Parameters[7]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	Mbps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to LOW-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ HIGH-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ HIGH-Z output	–	22.5	ns
tOW	End of write to LOW-Z output	0	–	ns

Note
7. All parameters guaranteed by design and validated through characterization.

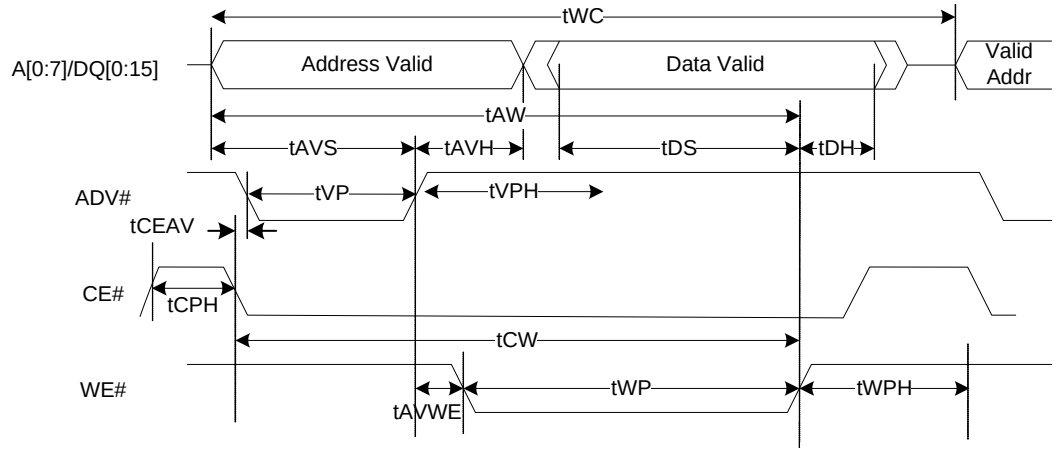
ADMux Timing for Asynchronous Access

Figure 21. ADMux Asynchronous Random Read



Note:
1. Multiple read cycles can be executed while keeping CE# low.
2. Read operation ends with either de-assertion of either OE# or CE#, whichever comes earlier.

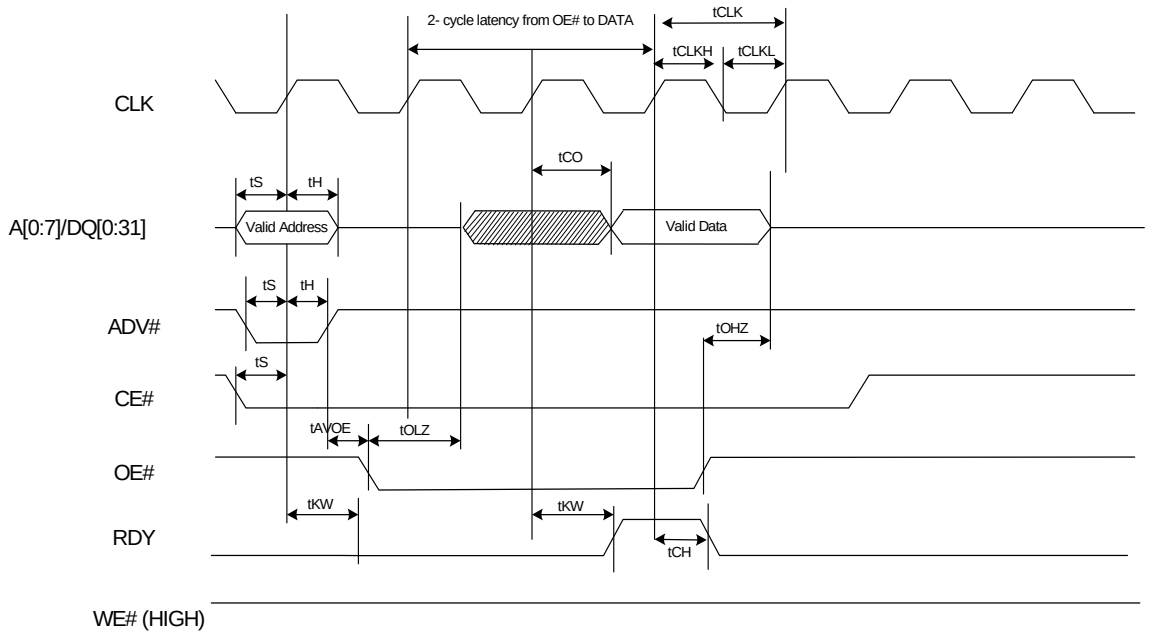
Figure 22. ADMux Asynchronous Random Write



Note:
1. Multiple write cycles can be executed while keeping CE# low.
2. Write operation ends with de-assertion of either WE# or CE#, whichever comes earlier.

Synchronous ADMux Timing

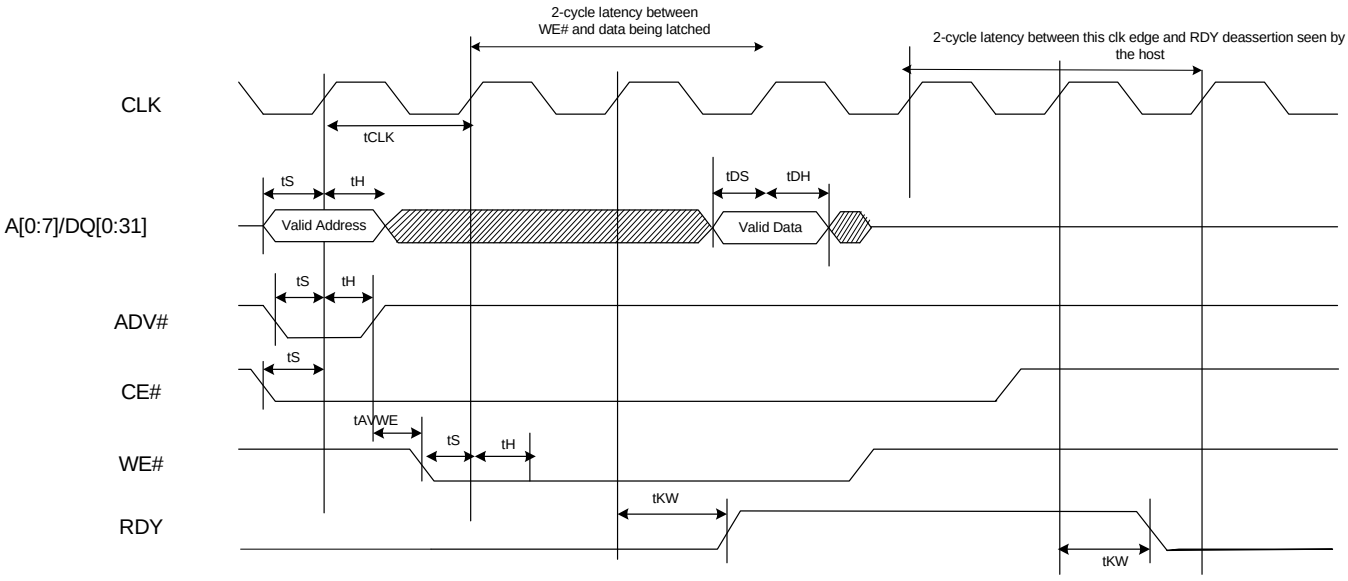
Figure 23. Synchronous ADMux Interface – Read Cycle Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The data is held until OE # deasserts
4) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

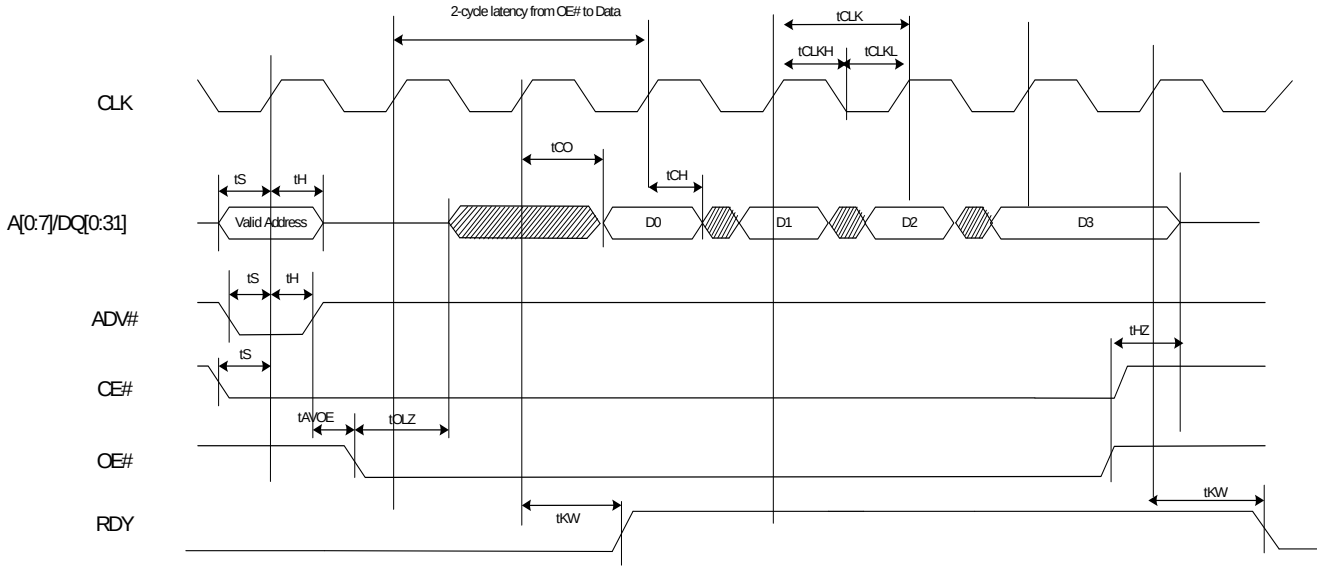
Figure 24. Synchronous ADMux Interface – Write Cycle Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deassert 3 cycles after the edge sampling the data.
3) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

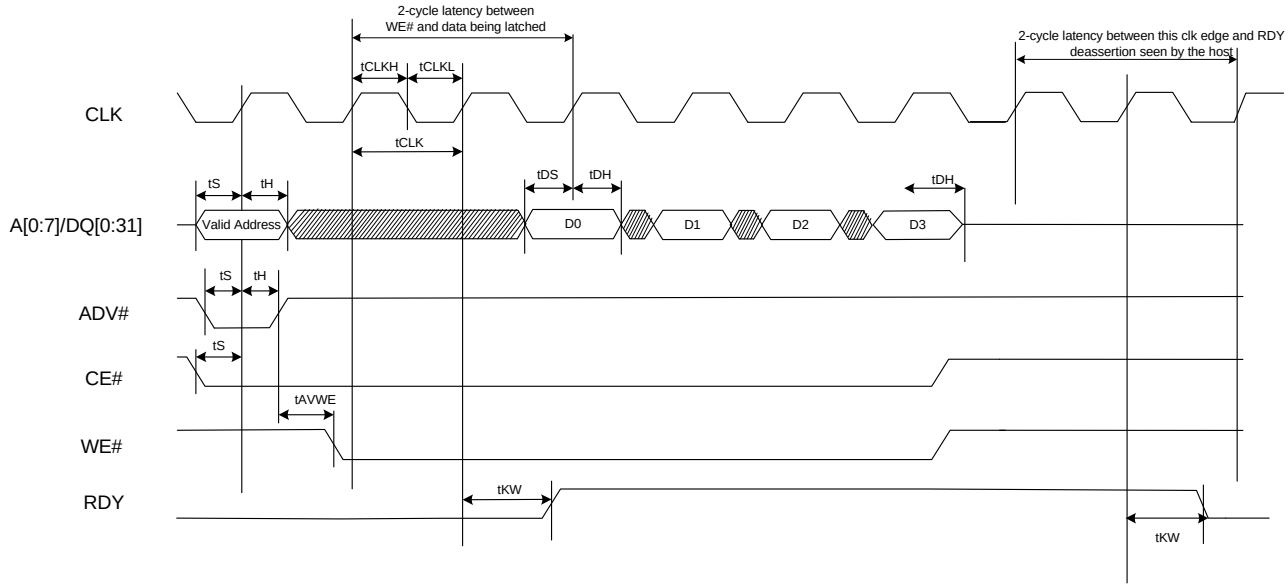
Figure 25. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 26. Sync ADMux Interface – Burst Write Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Table 16. I²C Timing Parameters[10]

Parameter	Description	Min	Max	Units
I²C Standard Mode Parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I²C Fast Mode Parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

Note
10. All parameters guaranteed by design and validated through characterization.

Table 16. I²C Timing Parameters[10] (continued)

Parameter	Description	Min	Max	Units
I²C Fast Mode Plus Parameters (Not supported at I2C_VDDQ=1.2 V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	ns
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus-free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I²S Timing Diagram

Figure 28. I²S Transmit Cycle

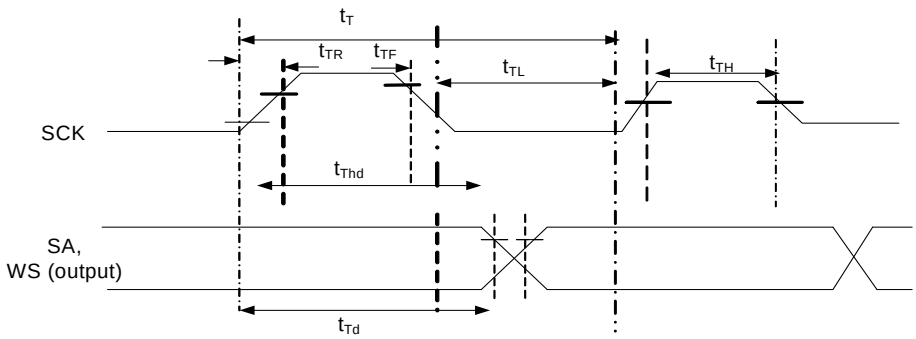


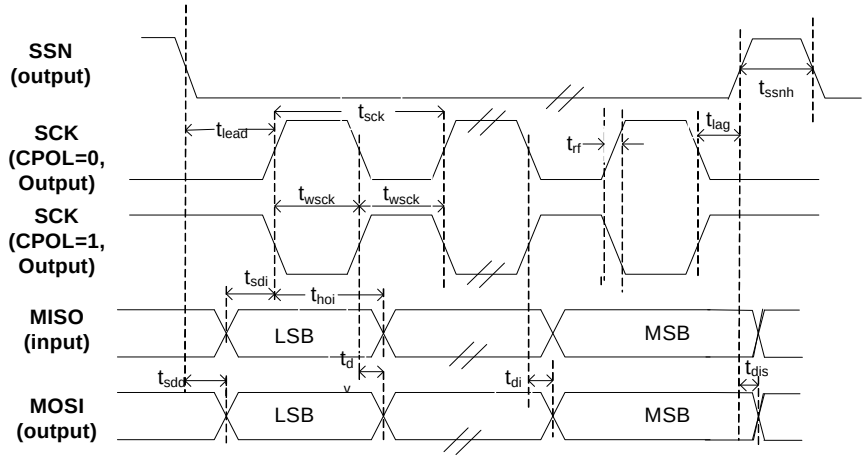
Table 17. I²S Timing Parameters[11]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 Ttr	ns
tTF	I²S transmitter fall time	–	0.15 Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

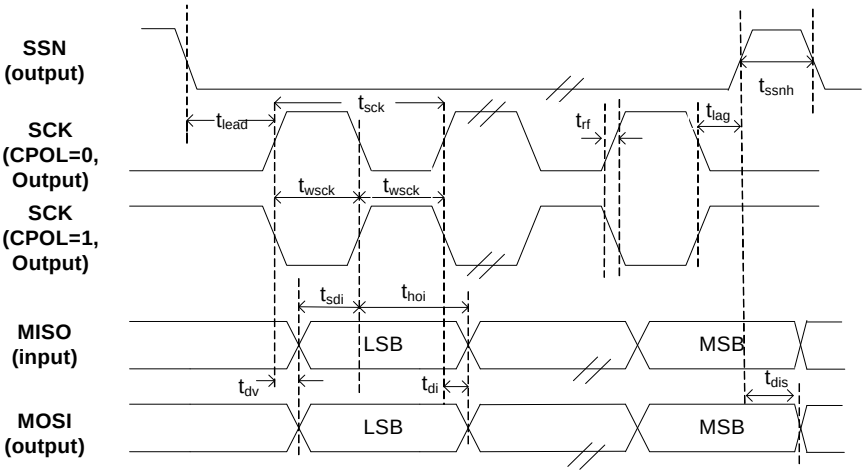
Note
11. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 29. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

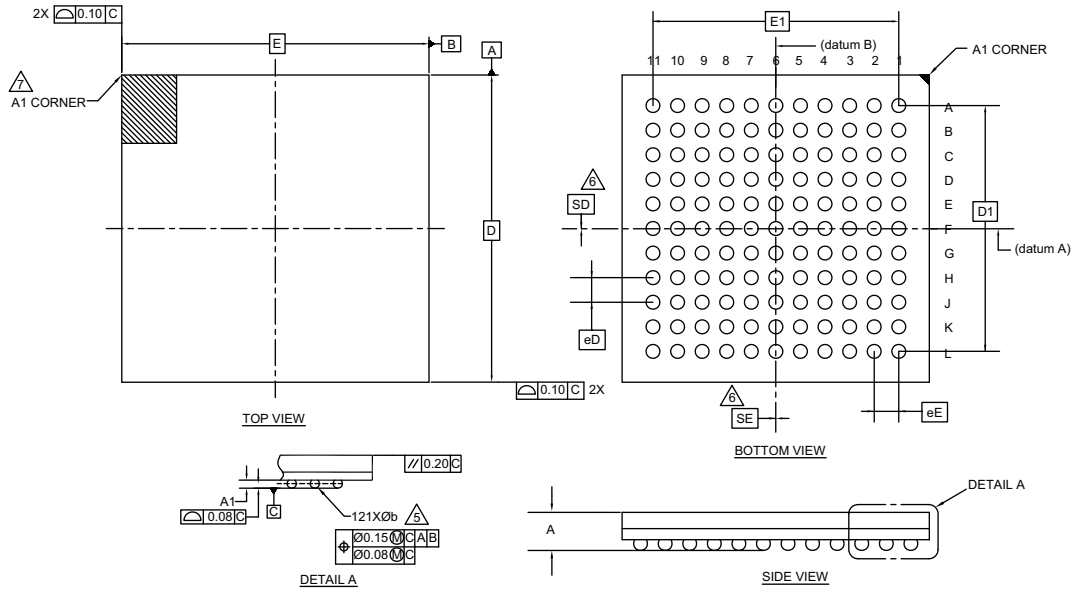
Table 18. SPI Timing Parameters[12]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[13]-5	1.5 tsck[13]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[13]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
12. All parameters guaranteed by design and validated through characterization.
13. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Package Diagram

Figure 31. 121-ball BGA Package Diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.15	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	121		
Ø b	0.25	0.30	0.35
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

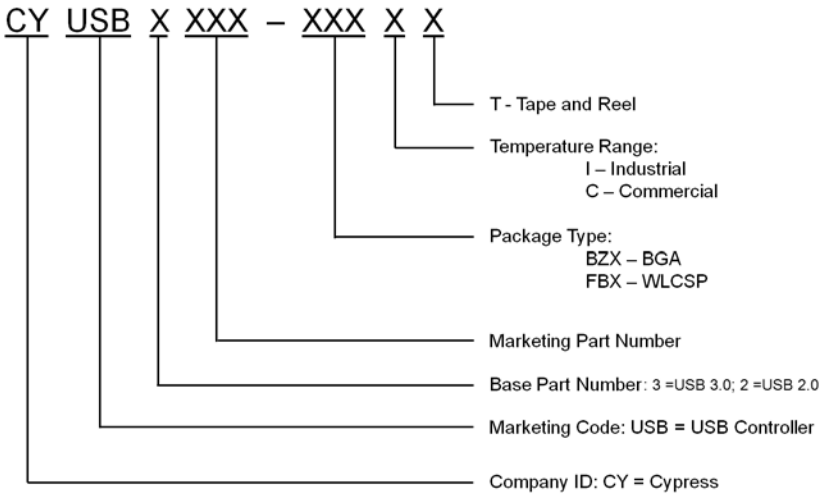
001-54471 *E

Ordering Information

Table 20. Ordering Information

Ordering Code	USB	SRAM (kB)	GPIF II Data Bus Width	Operating Temperature	Package Type
CYUSB3011-BZXC	USB 3.0	256	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3012-BZXC	USB 3.0	256	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3013-BZXC	USB 3.0	512	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXC	USB 3.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXI	USB 3.0	512	32-bit	–40°C to +85°C	121-ball BGA
CYUSB3014-FBXCT	USB 3.0	512	32-bit	0 °C to +70 °C	131-ball WLCSP
CYUSB3014-FBXIT	USB 3.0	512	32-bit	–40 °C to +85 °C	131-ball WLCSP
CYUSB2014-BZXC	USB 2.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB2014-BZXI	USB 2.0	512	32-bit	–40 °C to +85 °C	121-ball BGA

Ordering Code Definitions



■**Trigger Conditions**
This condition is triggered when FX3 is self-powered in USB boot mode.

■**Scope Of Impact**
Device does not enumerate

■**Workaround**
Reset the device after connecting to USB host.

■**Fix Status**
No fix. Workaround is required.

3. **Extra ZLP is generated by the COMMIT action in the GPIF II state.**

■**Problem Definition**
When COMMIT action is used in a GPIF-II state without IN_DATA action then an extra Zero Length Packet (ZLP) is committed along with the data packets.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when COMMIT action is used in a state without IN_DATA action.

■**Scope Of Impact**
Extra ZLP is generated.

■**Workaround**
Use IN_DATA action along with COMMIT action in the same state.

■**Fix Status**
No fix. Workaround is required.

4. **Invalid PID Sequence in USB 2.0 ISOC data transfer.**

■**Problem Definition**
When the FX3 device is functioning as a high speed USB device with high bandwidth isochronous endpoints, the PID sequence of the ISO data packets is governed solely by the isomult setting. The length of the data packet is not considered while generating the PID sequence during each microframe. For example, even if a short packet is being sent on an endpoint with MULT set to 2; the PID used will be DATA2

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when high bandwidth ISOC transfer endpoints are used.

■**Scope Of Impact**
ISOC data transfers failure.

■**Workaround**
This problem can be worked around by reconfiguring the endpoint with a lower isomult setting prior to sending short packets, and then switching back to the original value.

■**Fix Status**
No fix. Workaround is required.

5. **USB data transfer errors are seen when ZLP is followed by data packet within same microframe.**

■**Problem Definition**
Some data transfer errors may be seen if a Zero Length Packet is followed very quickly (within one microframe or 125 us) by another data packet on a burst enabled USB IN endpoint operating at super speed.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered in SuperSpeed transfer with ZLPs

■**Scope Of Impact**
Data failure and lower data speed.

■**Workaround**
The solution is to ensure that some time is allowed to elapse between a ZLP and the next data packet on burst enabled USB IN endpoints. If this cannot be ensured at the data source, the CyU3PDmaChannelSetSuspend() API can be used to suspend the

corresponding USB DMA socket on seeing the EOP condition. The channel operation can then be resumed as soon as the suspend callback is received.

■**Fix Status**
No fix. Workaround is required.

6. Bus collision is seen when the I²C block is used as a master in the I²C Multi-master configuration.

■Problem definition
When FX3 is used as a master in the I²C multi-master configuration, there can be occasional bus collisions.

■Parameters affected
NA

■Trigger Conditions
This condition is triggered only when the FX3 I²C block operates in Multi-master configuration.

■Scope Of Impact
The FX3 I²C block can transmit data when the I²C bus is not idle leading to bus collision.

■Workaround
Use FX3 as a single master.

■Fix Status
No fix.

Document History Page (continued)

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	3204393	OSG	03/24/2011	Updated Slave FIFO protocol and added ZLP signaling protocol Changed GPIFII asynchronous tDO parameter Changed Async Slave FIFO tOE parameter Changed Async Slave FIFO tRDO parameter Added tCOE parameter to GPIFII Sync mode timing parameters Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0 Modified description of GPIFII Sync tCO (previously tDO) parameter Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge. Correspondingly, changed the tAH number. Removed 24 bit data bus support for GPIFII.
*F	3219493	OSG	04/07/2011	Minor ECN - Release to web. No content changes.
*G	3235250	GSZ	04/20/2011	Minor updates in Features.
*H	3217917	OSG	04/06/2011	Updated GPIFII Synchronous Timing diagram. Added SPI Boot option. Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams. Corrected Synchronous Slave FIFO tDH parameter.
*I	3305568	DSG	07/07/2011	Minor ECN - Correct ECN number in revision *F. No content changes.
*J	3369042	OSG	12/06/2011	Changed datasheet status from Preliminary to Final. Changed tWRPE parameter to 2ns Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated Sync SLave FIFO Read timing diagram Updated SPI timing diagram Removed tGRANULARITY parameter Updated I2S Timing diagram and tTd parameter Updated 121-ball BGA package diagram. Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated tPEI parameter in Async Slave FIFO timing table Updated Sync Slave FIFO write and read timing diagrams Updated I2C interface tVD:ACK parameter for 1MHz operation Clarified that CTL[15] is not usable as a GPIO
*K	3534275	OSG	02/24/2012	Corrected typo in the block diagram.
*L	3649782	OSG	08/16/2012	Changed part number to CYUSB301X. Added 256 KB range for embedded SRAM. Updated Functional Overview, Other Interfaces, and Clocking sections. Added Pin List for CYUSB3011 and CYUSB3013 parts. Updated Ordering Information with new part numbers.
*M	3848148	OSG	12/20/2012	Updated 121-ball BGA package diagram to current revision.
*N	4016006	OSG	05/31/2013	Updated Features (Added 131-ball WLCSP under Package option). Updated Pin Configurations (Added FX3 131-ball WLCSP Ball Map (Figure 7)). Updated Pin Description (Updated Table 7). Updated Electrical Specifications (Included Commercial Temperature Range related information). Updated Operating Conditions (Included Commercial Temperature Range related information). Updated Package Diagram (Added 131-ball WLCSP Package Diagram (Figure 32)). Updated Ordering Information (Updated part numbers).

Document History Page (continued)

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*T	5306567	MDDD	06/29/2016	Updated AC Timing Parameters: Updated GPIF II Timing: Updated Table 9: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Write Sequence Description: Updated Table 11: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated to new template.
*U	5703914	GNKK	04/20/2017	Updated the Cypress logo and copyright information.