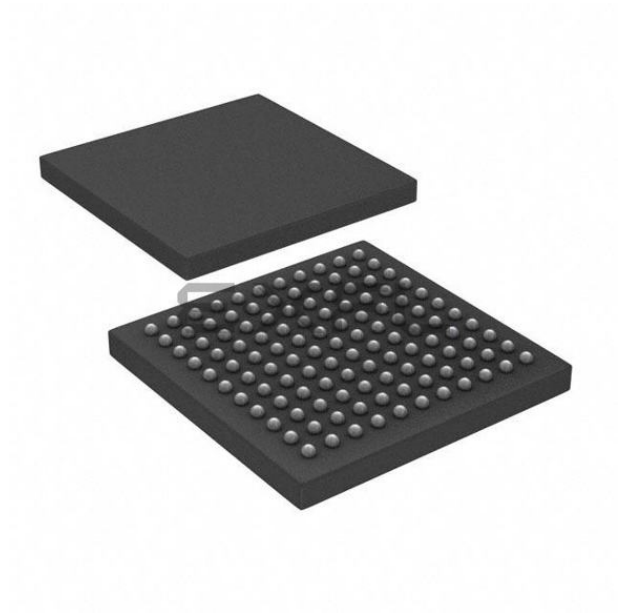

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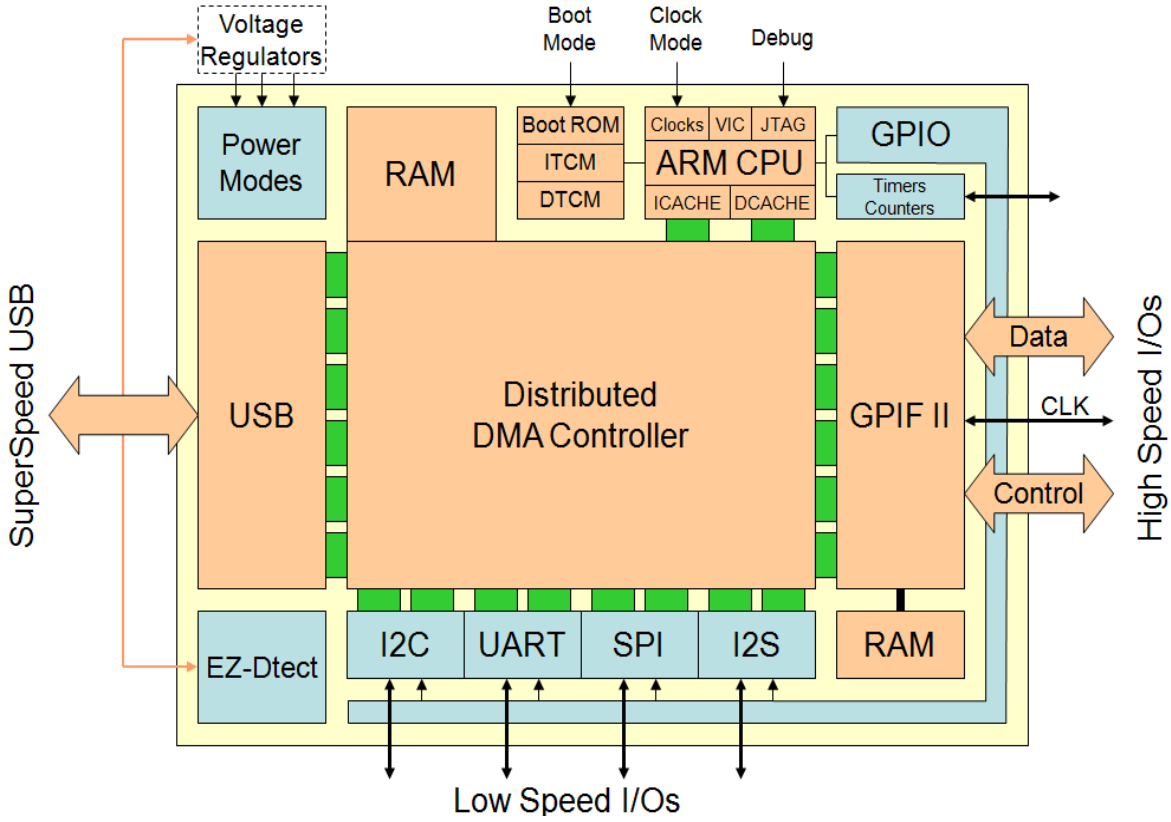
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	I²C, I²S, MMC/SD, SPI, UART, USB
Number of I/O	59
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb2014-bzxi

Logic Block Diagram



Contents

Functional Overview

Cypress's EZ-USB FX3 is a SuperSpeed peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.1 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see Ordering Information on page 45) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I^2S.

FX3 comes with application development tools. The software development kit comes with firmware and host application examples for accelerating time to market.

FX3 complies with the USB 3.1, Gen 1.0 specification and is also backward compatible with USB 2.0. It also complies with the Battery Charging Specification v1.1 and USB 2.0 OTG Specification v2.0.

Application Examples

In a typical application (see Figure 1), the FX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection. Additionally, FX3 can function as a coprocessor connecting via the GPIF II interface to an application processor (see Figure 2) and operates as a subsystem providing SuperSpeed USB connectivity to the application processor.

Figure 1. EZ-USB FX3 as Main Processor

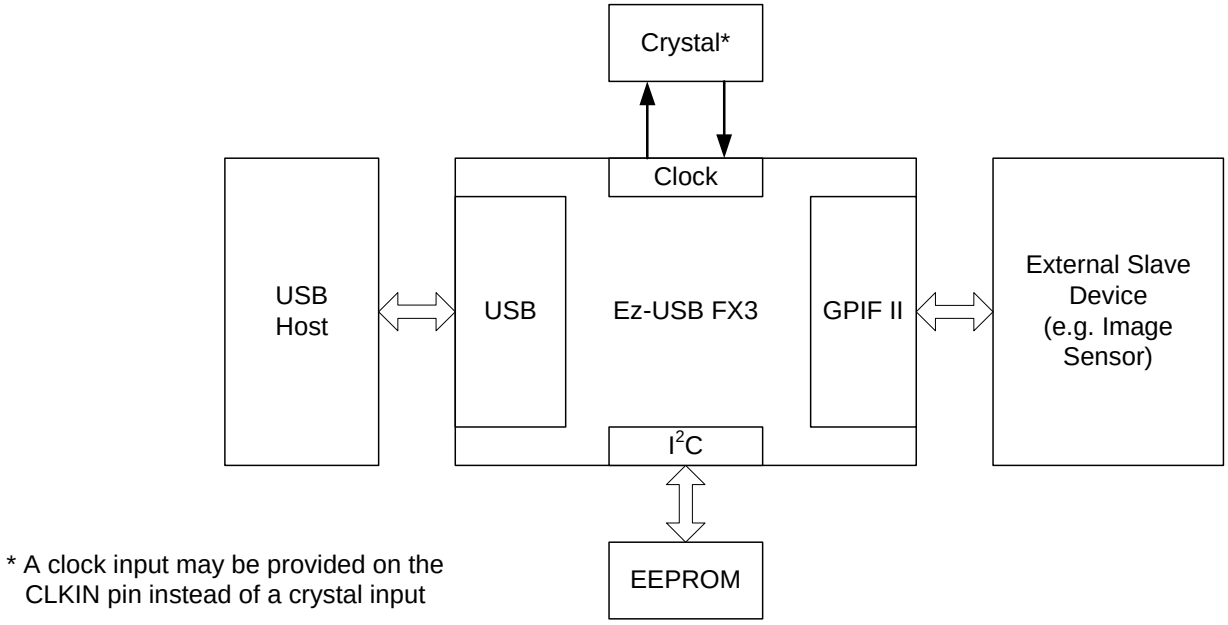
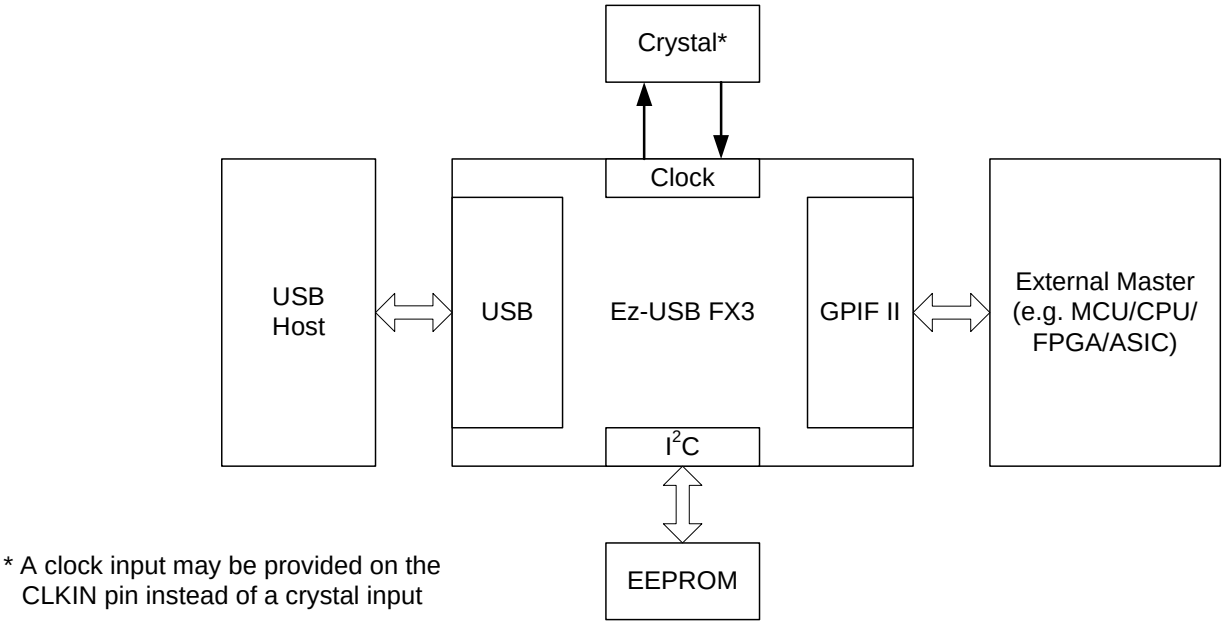


Figure 2. EZ-USB FX3 as a Coprocessor



USB Interface

FX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.1 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- FX3 Hi-Speed parts (CYUSB201X) only support USB 2.0.
- Complies with OTG Supplement Revision 2.0. It supports High-Speed, Full-Speed, and Low-Speed OTG dual-role device capability. As a peripheral, FX3 is capable of SuperSpeed, High-Speed, and Full-Speed. As a host, it is capable of High-Speed, Full-Speed, and Low-Speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, application examples show that the FX3 supports UAS, USB Video Class (UVC), and Mass Storage Class (MSC) USB peripheral classes. All other device classes can be supported by customer firmware; a template example is provided as a starting point.
- As an OTG host, application examples show that FX3 supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

OTG

FX3 is compliant with the OTG Specification Revision 2.0. In OTG mode, FX3 supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3 requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3 does not support Attach Detection Protocol (ADP).

OTG Connectivity

In OTG mode, FX3 can be configured to be an A, B, or dual-role device. It can connect to the following:

- ACA device
- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

EZ-Dtect

FX3 supports USB Charger and accessory detection (EZ-Dtect). The charger detection mechanism complies with the Battery Charging Specification Revision 1.1. In addition to supporting this version of the specification, FX3 also provides hardware support to detect the resistance values on the ID pin.

FX3 can detect the following resistance ranges:

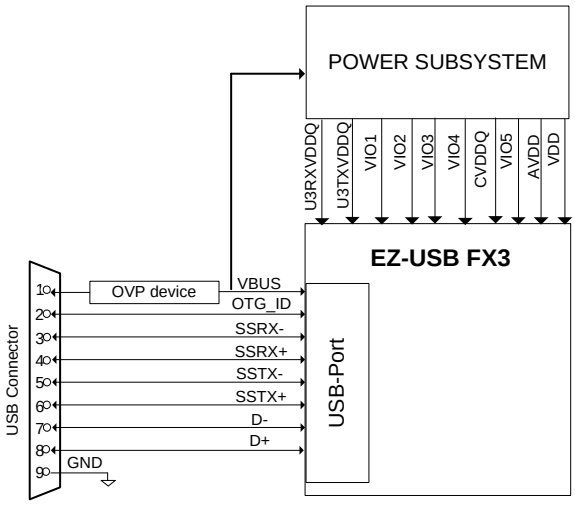
- Less than 10 Ω
- Less than 1 kΩ
- 65 kΩ to 72 kΩ
- 35 kΩ to 39 kΩ
- 99.96 kΩ to 104.4 kΩ (102 kΩ ± 2%)
- 119 kΩ to 132 kΩ
- Higher than 220 kΩ
- 431.2 kΩ to 448.8 kΩ (440 kΩ ± 2%)

FX3's charger detects a dedicated wall charger, Host/Hub charger, and Host/Hub.

VBUS Overvoltage Protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. Figure 3 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 8 for the operating range of VBUS and VBATT.

Figure 3. System Diagram with OVP Device For VBUS



Carkit UART Mode

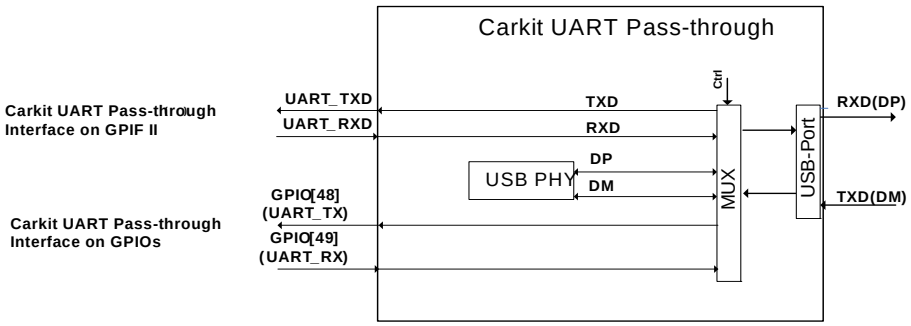
The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in Figure on page 8.

In this mode, FX3 supports a rate of up to 9600 bps.

Figure 4. Carkit UART Pass-through Block Diagram



UART Interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

I²C Interface

FX3's I²C interface is compatible with the I²C Bus Specification Revision 3. This I²C interface is capable of operating only as I²C master; therefore, it may be used to communicate with other I²C slave devices. For example, FX3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

FX3's I²C Master Controller also supports multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports clock-stretching to enable slower devices to exercise flow control.

The I²C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

I²S Interface

FX3 has an I²S port to support external audio codec devices. FX3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I²S interface are 32 kHz, 44.1 kHz, and 48 kHz.

Boot Options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I²C
- Boot from SPI (SPI devices supported are M25P32 (32 Mbit), M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode

Table 2. FX3 Booting Options

PMODE[2:0][1]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I²C, On Failure, USB Boot is Enabled
1FF	I²C only
0F1	SPI, On Failure, USB Boot is Enabled

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in Figure 30 on page 42 and Table 19 on page 42. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB® FX3™ Boot Options for more details.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Note
1. F indicates Floating.

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See Pin Configurations for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Pin Configurations

Figure 6. FX3 121-ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 7. FX3 131-Ball WLCSP Ball Map (Bottom View)

	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	SSRXM		SSTXM	FSLC[0]	AVSS	AVDD	DP	VSS	DM	VDD
B	GPIO[55]	VIO4	SSRXP	R_USB3	SSTXP	FSLC[2]	XTALIN	XTALOUT	NC	R_USB2	NC	VDD
C	GPIO[56]	VIO3	U3RXVDDQ	U3VSSQ	U3TXVDDQ	CVDDQ	CLKIN_32	CLKIN	VSS	OTG_ID	TDO	TRST#
D	GPIO[49]	GPIO[50]	GPIO[53]	GPIO[54]	RESET#	VDD	I2C_GPIO[58]	TMS	VIO5	TCK	I2C_GPIO[59]	VSS
E	GPIO[57]	GPIO[48]	GPIO[51]	GPIO[52]	O[60]	VSS	VSS	VSS	VSS	GPIO[3]	VBATT	VBUS
F	VSS	GPIO[46]	GPIO[47]	FSLC[1]	TDI	VDD	VDD	VDD	VDD	GPIO[4]	GPIO[1]	GPIO[0]
G	VIO2	GPIO[43]	GPIO[44]	GPIO[45]	VSS	VSS	VDD	VSS	GPIO[9]	GPIO[7]	GPIO[6]	GPIO[2]
H	VSS	GPIO[40]	GPIO[41]	GPIO[42]	GPIO[39]	VSS	GPIO[20]	GPIO[18]	GPIO[14]	GPIO[12]	GPIO[8]	VIO1
J	VIO2	GPIO[38]	GPIO[37]	GPIO[36]	GPIO[31]	GPIO[27]	GPIO[25]	GPIO[22]	GPIO[19]	GPIO[15]	GPIO[10]	GPIO[5]
K	GPIO[35]	GPIO[34]	GPIO[33]	GPIO[32]	GPIO[28]	GPIO[26]	GPIO[16]	GPIO[21]	INT#	GPIO[24]	GPIO[11]	VSS
L	VDD	VSS	VDD	GPIO[30]	GPIO[29]	VIO1	GPIO[23]	VSS	VIO1	GPIO[17]	GPIO[13]	VSS

Note No ball is populated at location A9.

Figure 8. FX3 Hi-Speed 121-Ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	VDD	NC	NC	NC	NC	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	NC	FSLC[1]	VDD	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Pin Description

Table 7. CYUSB3012 and CYUSB3014 Pin List

BGA	WLCSP	Power Domain	I/O	Name	Description					
					GPIF II Interface			Slave FIFO Interface		
F10	F1	VIO1	I/O	GPIO[0]	DQ[0]			DQ[0]		
F9	F2	VIO1	I/O	GPIO[1]	DQ[1]			DQ[1]		
F7	G1	VIO1	I/O	GPIO[2]	DQ[2]			DQ[2]		
G10	E3	VIO1	I/O	GPIO[3]	DQ[3]			DQ[3]		
G9	F3	VIO1	I/O	GPIO[4]	DQ[4]			DQ[4]		
F8	J1	VIO1	I/O	GPIO[5]	DQ[5]			DQ[5]		
H10	G2	VIO1	I/O	GPIO[6]	DQ[6]			DQ[6]		
H9	G3	VIO1	I/O	GPIO[7]	DQ[7]			DQ[7]		
J10	H2	VIO1	I/O	GPIO[8]	DQ[8]			DQ[8]		
J9	G4	VIO1	I/O	GPIO[9]	DQ[9]			DQ[9]		
K11	J2	VIO1	I/O	GPIO[10]	DQ[10]			DQ[10]		
L10	K2	VIO1	I/O	GPIO[11]	DQ[11]			DQ[11]		
K10	H3	VIO1	I/O	GPIO[12]	DQ[12]			DQ[12]		
K9	L2	VIO1	I/O	GPIO[13]	DQ[13]			DQ[13]		
J8	H4	VIO1	I/O	GPIO[14]	DQ[14]			DQ[14]		
G8	J3	VIO1	I/O	GPIO[15]	DQ[15]			DQ[15]		
J6	K6	VIO1	I/O	GPIO[16]	PCLK			CLK		
K8	L3	VIO1	I/O	GPIO[17]	CTL[0]			SLCS#		
K7	H5	VIO1	I/O	GPIO[18]	CTL[1]			SLWR#		
J7	J4	VIO1	I/O	GPIO[19]	CTL[2]			SLOE#		
H7	H6	VIO1	I/O	GPIO[20]	CTL[3]			SLRD#		
G7	K5	VIO1	I/O	GPIO[21]	CTL[4]			FLAGA		
G6	J5	VIO1	I/O	GPIO[22]	CTL[5]			FLAGB		
K6	L6	VIO1	I/O	GPIO[23]	CTL[6]			GPIO		
H8	K3	VIO1	I/O	GPIO[24]	CTL[7]			PKTEND#		
G5	J6	VIO1	I/O	GPIO[25]	CTL[8]			GPIO		
H6	K7	VIO1	I/O	GPIO[26]	CTL[9]			GPIO		
K5	J7	VIO1	I/O	GPIO[27]	CTL[10]			GPIO		
J5	K8	VIO1	I/O	GPIO[28]	CTL[11]			A1		
H5	L8	VIO1	I/O	GPIO[29]	CTL[12]			A0		
G4	L9	VIO1	I/O	GPIO[30]	PMODE[0]			PMODE[0]		
H4	J8	VIO1	I/O	GPIO[31]	PMODE[1]			PMODE[1]		
L4	K9	VIO1	I/O	GPIO[32]	PMODE[2]			PMODE[2]		
L8	K4	VIO1	I/O	INT#	INT#/CTL[15]			CTL[15]		
					32-bit Data Bus	16 - bit Data Bus + UART+SPI+I2S	16 - bit Data Bus + UART+GPIO	16 - bit Data Bus + SPI+GPIO	16 - bit Data Bus + I2S+GPIO	GPIO only
K2	K10	VIO2	I/O	GPIO[33]	DQ[16]	GPIO	GPIO	GPIO	GPIO	GPIO
J4	K11	VIO2	I/O	GPIO[34]	DQ[17]	GPIO	GPIO	GPIO	GPIO	GPIO
K1	K12	VIO2	I/O	GPIO[35]	DQ[18]	GPIO	GPIO	GPIO	GPIO	GPIO
J2	J9	VIO2	I/O	GPIO[36]	DQ[19]	GPIO	GPIO	GPIO	GPIO	GPIO
J3	J10	VIO2	I/O	GPIO[37]	DQ[20]	GPIO	GPIO	GPIO	GPIO	GPIO

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description					
J1	J11	VIO2	I/O	GPIO[38]	DQ[21]	GPIO	GPIO	GPIO	GPIO	GPIO
H2	H8	VIO2	I/O	GPIO[39]	DQ[22]	GPIO	GPIO	GPIO	GPIO	GPIO
H3	H11	VIO2	I/O	GPIO[40]	DQ[23]	GPIO	GPIO	GPIO	GPIO	GPIO
F4	H10	VIO2	I/O	GPIO[41]	DQ[24]	GPIO	GPIO	GPIO	GPIO	GPIO
G2	H9	VIO2	I/O	GPIO[42]	DQ[25]	GPIO	GPIO	GPIO	GPIO	GPIO
G3	G11	VIO2	I/O	GPIO[43]	DQ[26]	GPIO	GPIO	GPIO	GPIO	GPIO
F3	G10	VIO2	I/O	GPIO[44]	DQ[27]	GPIO	GPIO	GPIO	GPIO	GPIO
F2	G09	VIO2	I/O	GPIO[45]	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
F5	F11	VIO3	I/O	GPIO[46]	DQ[28]	UART_RT S	GPIO	GPIO	GPIO	GPIO
E1	F10	VIO3	I/O	GPIO[47]	DQ[29]	UART_CT S	GPIO	GPIO	GPIO	GPIO
E5	E11	VIO3	I/O	GPIO[48]	DQ[30]	UART_TX	GPIO	GPIO	GPIO	GPIO
E4	D12	VIO3	I/O	GPIO[49]	DQ[31]	UART_R X	GPIO	GPIO	GPIO	GPIO
D1	D11	VIO3	I/O	GPIO[50]	I2S_CLK	I2S_CLK	GPIO	GPIO	GPIO	GPIO
D2	E10	VIO3	I/O	GPIO[51]	I2S_SD	I2S_SD	GPIO	GPIO	GPIO	GPIO
D3	E9	VIO3	I/O	GPIO[52]	I2S_WS	I2S_WS	GPIO	GPIO	GPIO	GPIO
D4	D10	VIO4	I/O	GPIO[53]	UART_RTS	SPI_SCK	UART_RTS	SPI_SCK	GPIO	GPIO
C1	D9	VIO4	I/O	GPIO[54]	UART_CTS	SPI_SSN	UART_CTS	SPI_SSN	I2S_CLK	GPIO
C2	B12	VIO4	I/O	GPIO[55]	UART_TX	SPI_MIS O	UART_TX	SPI_MISO	I2S_SD	GPIO
D5	C12	VIO4	I/O	GPIO[56]	UART_RX	SPI_MOS I	UART_RX	SPI_MOSI	I2S_WS	GPIO
C4	E12	VIO4	I/O	GPIO[57]	I2S_MCLK	I2S_MCL K	GPIO	GPIO	I2S_MCL K	GPIO
					USB Port					
					CYUSB301X			**CYUSB201X**		
A3	A10	U3RXVD DQ	I	SSRXM	SSRX-			NC		
A4	B10	U3RXVD DQ	I	SSRXP	SSRX+			NC		
A6	A8	U3TXVD DQ	O	SSTXM	SSTX-			NC		
A5	B8	U3TXVD DQ	O	SSTXP	SSTX+			NC		
B3	B9	U3TXVD DQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND)			NC		
C9	C3	VBUS/ VBATT	I	OTG_ID	OTG_ID					
A9	A4	VBUS/V BATT	I/O	DP	D+					
A10	A2	VBUS/V BATT	I/O	DM	D–					
C8	B3	VBUS/VBAT T	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)					
					Clock and Reset					
B2	A7	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	B6	AVDD	I/O	XTALIN	XTALIN					
C7	B5	AVDD	I/O	XTALOUT	XTALOUT					
B4	F9	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	B7	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	C5	CVDDQ	I	CLKIN	CLKIN					

Figure 10. GPIF II Timing in Asynchronous Mode

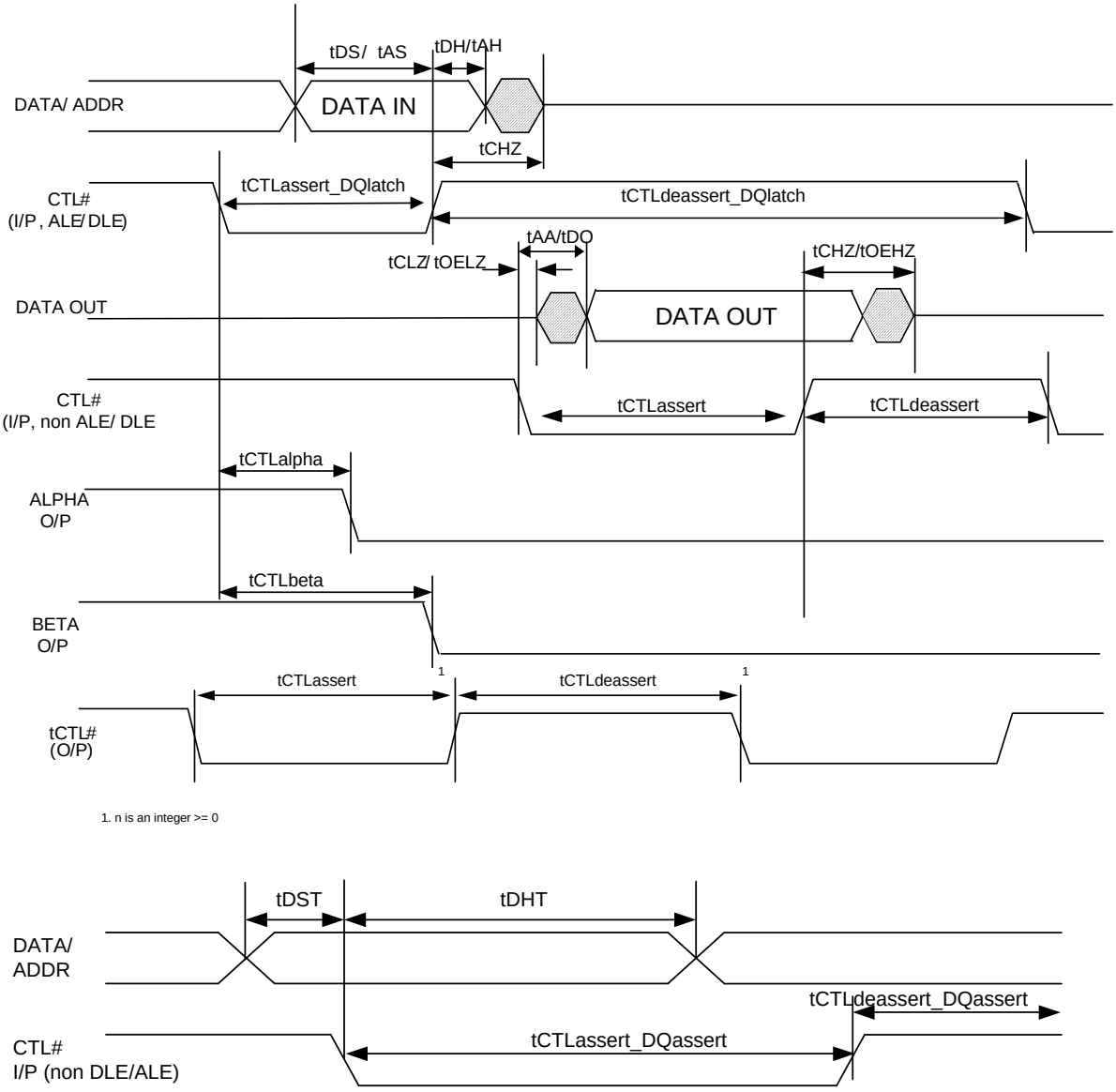


Figure 11. GPIF II Timing in Asynchronous DDR Mode

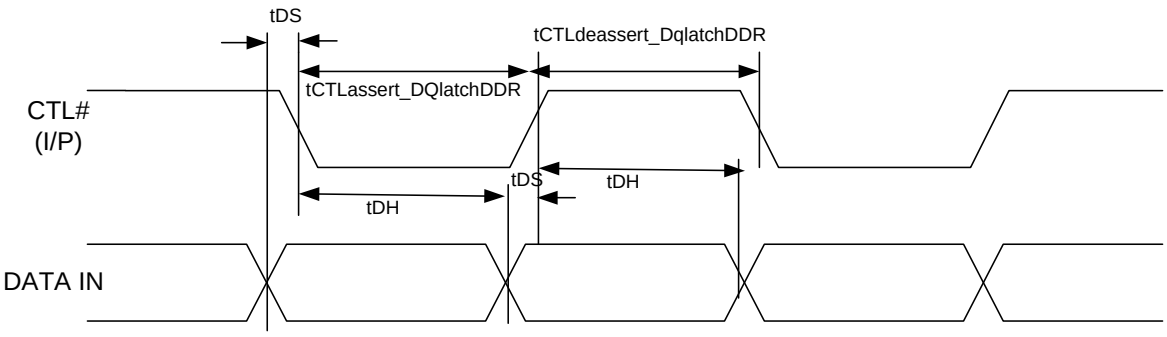
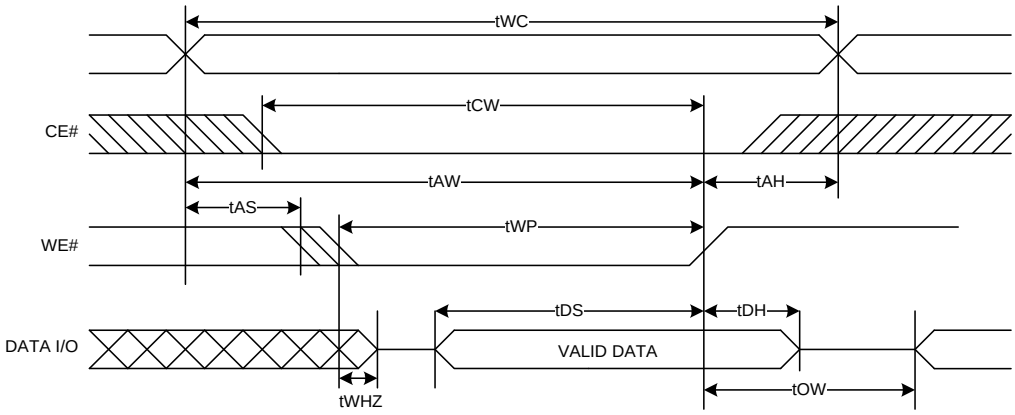


Figure 20. Non-multiplexed Asynchronous SRAM Write Timing (WE# controlled, OE# LOW)

Write Cycle 3 WE# Controlled. OE# Low



Note: tWP must be adjusted such that tWP > tWHZ + tDS

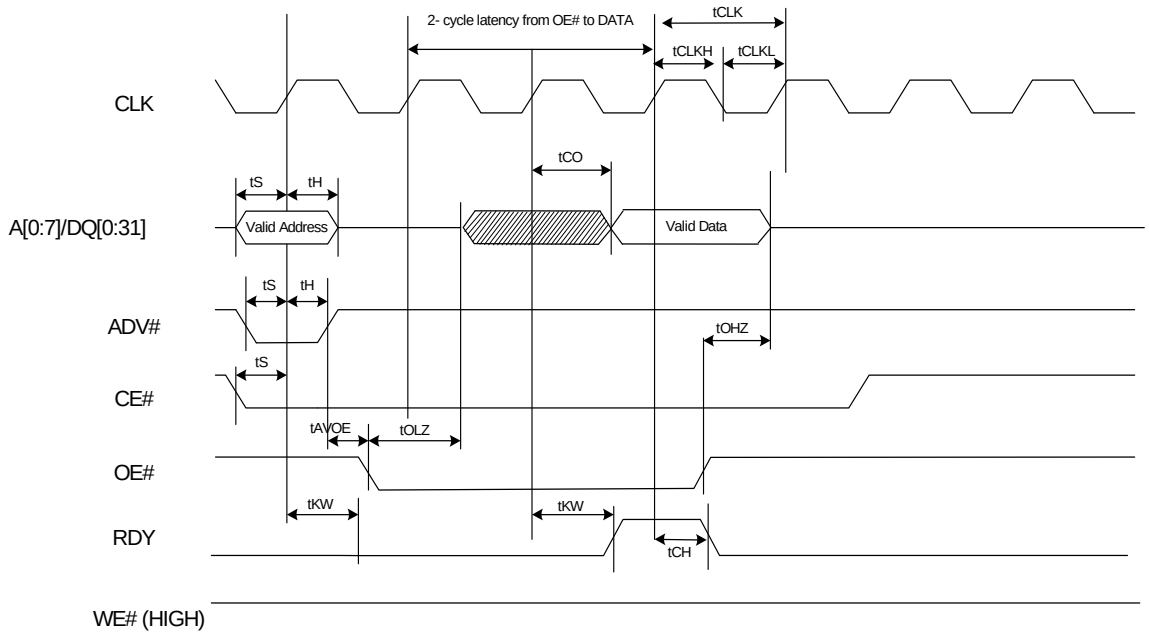
Table 13. Asynchronous SRAM Timing Parameters[7]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	Mbps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to LOW-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ HIGH-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ HIGH-Z output	–	22.5	ns
tOW	End of write to LOW-Z output	0	–	ns

Note
7. All parameters guaranteed by design and validated through characterization.

Synchronous ADMux Timing

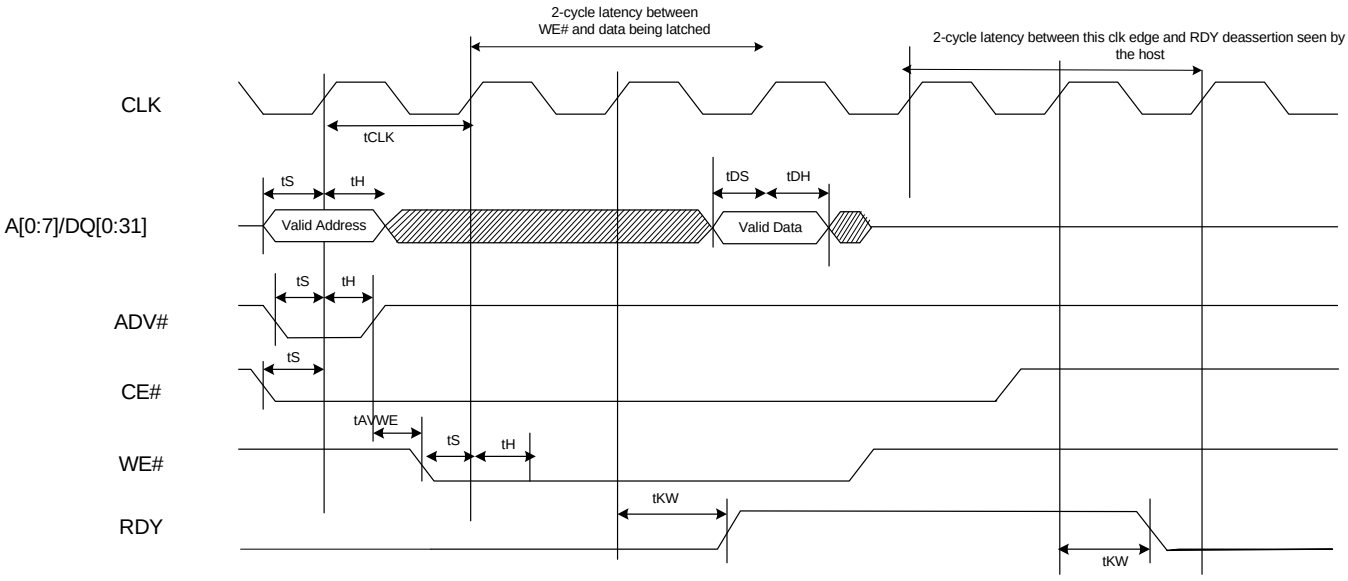
Figure 23. Synchronous ADMux Interface – Read Cycle Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The data is held until OE # deasserts
4) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

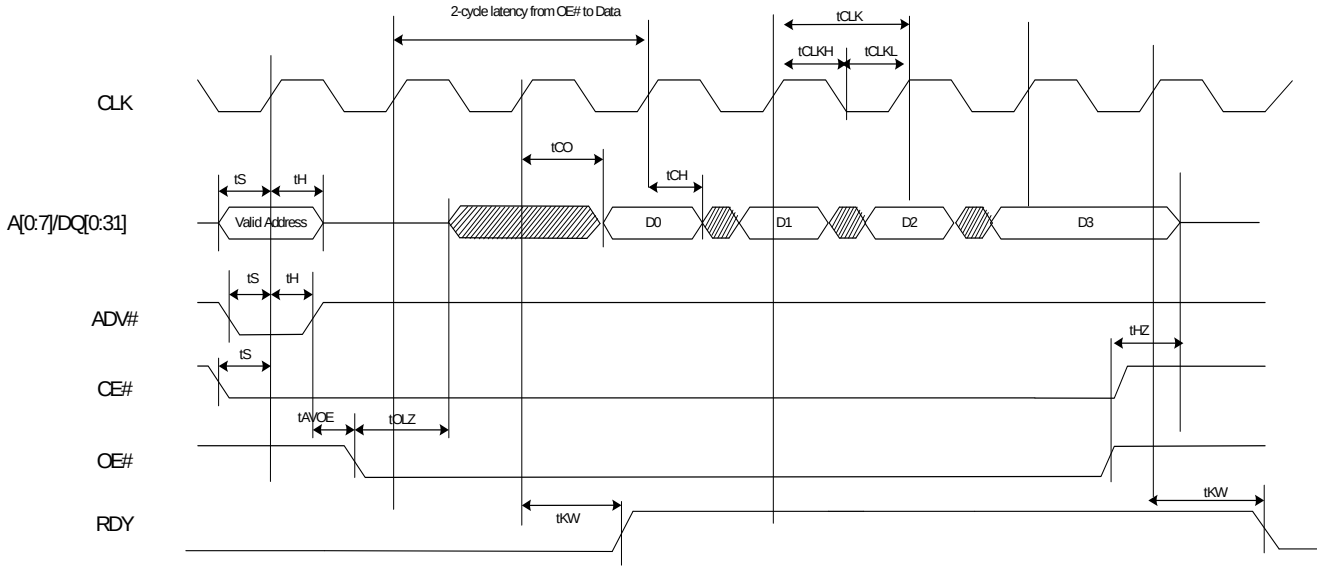
Figure 24. Synchronous ADMux Interface – Write Cycle Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deassert 3 cycles after the edge sampling the data.
3) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

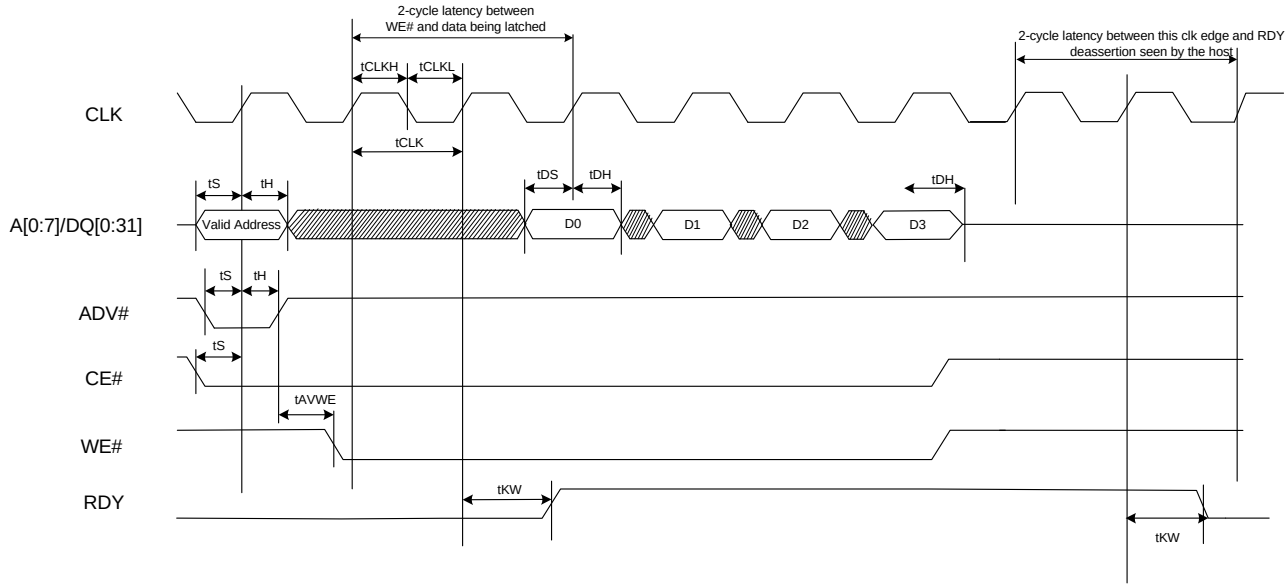
Figure 25. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 26. Sync ADMux Interface – Burst Write Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

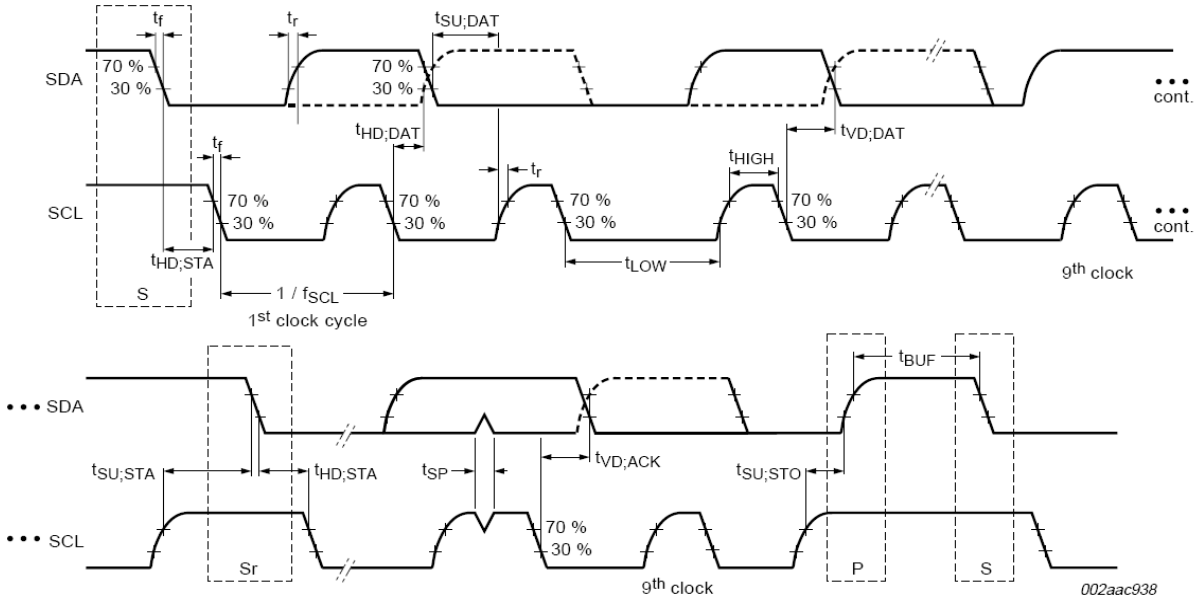
Table 15. Synchronous ADMux Timing Parameters[9]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Serial Peripherals Timing

I^2C Timing

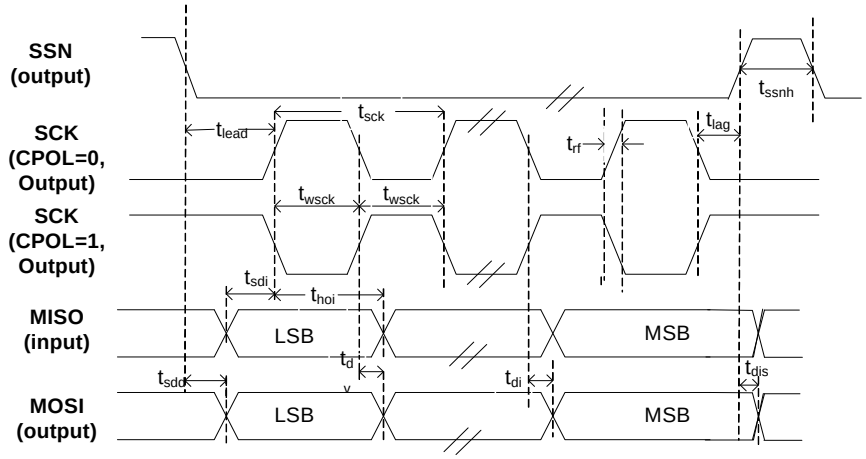
Figure 27. I^2C Timing Definition



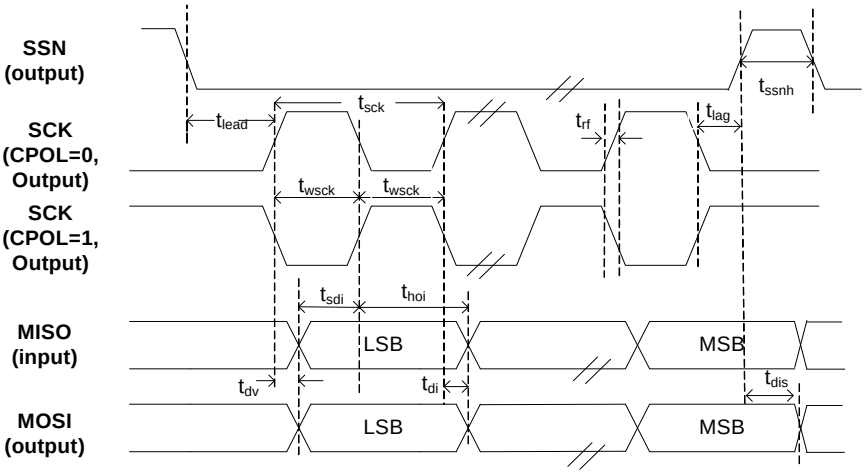
Note
9. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 29. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

■**Trigger Conditions**
This condition is triggered when FX3 is self-powered in USB boot mode.

■**Scope Of Impact**
Device does not enumerate

■**Workaround**
Reset the device after connecting to USB host.

■**Fix Status**
No fix. Workaround is required.

3. **Extra ZLP is generated by the COMMIT action in the GPIF II state.**

■**Problem Definition**
When COMMIT action is used in a GPIF-II state without IN_DATA action then an extra Zero Length Packet (ZLP) is committed along with the data packets.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when COMMIT action is used in a state without IN_DATA action.

■**Scope Of Impact**
Extra ZLP is generated.

■**Workaround**
Use IN_DATA action along with COMMIT action in the same state.

■**Fix Status**
No fix. Workaround is required.

4. **Invalid PID Sequence in USB 2.0 ISOC data transfer.**

■**Problem Definition**
When the FX3 device is functioning as a high speed USB device with high bandwidth isochronous endpoints, the PID sequence of the ISO data packets is governed solely by the isomult setting. The length of the data packet is not considered while generating the PID sequence during each microframe. For example, even if a short packet is being sent on an endpoint with MULT set to 2; the PID used will be DATA2

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when high bandwidth ISOC transfer endpoints are used.

■**Scope Of Impact**
ISOC data transfers failure.

■**Workaround**
This problem can be worked around by reconfiguring the endpoint with a lower isomult setting prior to sending short packets, and then switching back to the original value.

■**Fix Status**
No fix. Workaround is required.

5. **USB data transfer errors are seen when ZLP is followed by data packet within same microframe.**

■**Problem Definition**
Some data transfer errors may be seen if a Zero Length Packet is followed very quickly (within one microframe or 125 us) by another data packet on a burst enabled USB IN endpoint operating at super speed.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered in SuperSpeed transfer with ZLPs

■**Scope Of Impact**
Data failure and lower data speed.

■**Workaround**
The solution is to ensure that some time is allowed to elapse between a ZLP and the next data packet on burst enabled USB IN endpoints. If this cannot be ensured at the data source, the CyU3PDmaChannelSetSuspend() API can be used to suspend the

Document History Page (continued)

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	3204393	OSG	03/24/2011	Updated Slave FIFO protocol and added ZLP signaling protocol Changed GPIFII asynchronous tDO parameter Changed Async Slave FIFO tOE parameter Changed Async Slave FIFO tRDO parameter Added tCOE parameter to GPIFII Sync mode timing parameters Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0 Modified description of GPIFII Sync tCO (previously tDO) parameter Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge. Correspondingly, changed the tAH number. Removed 24 bit data bus support for GPIFII.
*F	3219493	OSG	04/07/2011	Minor ECN - Release to web. No content changes.
*G	3235250	GSZ	04/20/2011	Minor updates in Features.
*H	3217917	OSG	04/06/2011	Updated GPIFII Synchronous Timing diagram. Added SPI Boot option. Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams. Corrected Synchronous Slave FIFO tDH parameter.
*I	3305568	DSG	07/07/2011	Minor ECN - Correct ECN number in revision *F. No content changes.
*J	3369042	OSG	12/06/2011	Changed datasheet status from Preliminary to Final. Changed tWRPE parameter to 2ns Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated Sync SLave FIFO Read timing diagram Updated SPI timing diagram Removed tGRANULARITY parameter Updated I2S Timing diagram and tTd parameter Updated 121-ball BGA package diagram. Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated tPEI parameter in Async Slave FIFO timing table Updated Sync Slave FIFO write and read timing diagrams Updated I2C interface tVD:ACK parameter for 1MHz operation Clarified that CTL[15] is not usable as a GPIO
*K	3534275	OSG	02/24/2012	Corrected typo in the block diagram.
*L	3649782	OSG	08/16/2012	Changed part number to CYUSB301X. Added 256 KB range for embedded SRAM. Updated Functional Overview, Other Interfaces, and Clocking sections. Added Pin List for CYUSB3011 and CYUSB3013 parts. Updated Ordering Information with new part numbers.
*M	3848148	OSG	12/20/2012	Updated 121-ball BGA package diagram to current revision.
*N	4016006	OSG	05/31/2013	Updated Features (Added 131-ball WLCSP under Package option). Updated Pin Configurations (Added FX3 131-ball WLCSP Ball Map (Figure 7)). Updated Pin Description (Updated Table 7). Updated Electrical Specifications (Included Commercial Temperature Range related information). Updated Operating Conditions (Included Commercial Temperature Range related information). Updated Package Diagram (Added 131-ball WLCSP Package Diagram (Figure 32)). Updated Ordering Information (Updated part numbers).

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Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	4368374	RSKV	05/02/2014	Updated Package Diagram: spec 001-62221 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*P	4474200	ANOP	08/14/2014	Added CYUSB201x MPNs, ball map, and pin list to the datasheet.
*Q	4668496	DBIR	02/24/2015	Updated Features. Updated Logic Block Diagram. Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Added More Information. Updated Functional Overview: Updated Application Examples: Updated Figure 1. Updated Figure 2. Updated USB Interface: Updated description. Removed Figure “USB Interface Signals”. Updated Pin Configurations: Updated Figure 6. Updated Reset: Updated Hard Reset: Updated description. Updated Pin Description: Updated Table 7: Updated entire table. Modified CVDDQ power domain description. Removed Table “CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width)”. Removed Table “CYUSB2014 Pin List (GPIF II with 32-bit Data Bus Width)”. Updated Electrical Specifications: Updated DC Specifications: Added ISS parameter and its details. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11. Updated AC Timing Parameters: Added Host Processor Interface (P-Port) Timing. Updated Acronyms. Added Errata. Replaced West Bridge Benicia with FX3.
*R	4703347	AMDK	03/27/2015	Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11: Updated minimum value of tSSD parameter. Added tACCD, tFAD parameters and their details.
*S	5160624	AJAI	04/07/2016	Removed ISS parameter. Added item 6 in Errata.

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Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*T	5306567	MDDD	06/29/2016	Updated AC Timing Parameters: Updated GPIF II Timing: Updated Table 9: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Write Sequence Description: Updated Table 11: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated to new template.
*U	5703914	GNKK	04/20/2017	Updated the Cypress logo and copyright information.