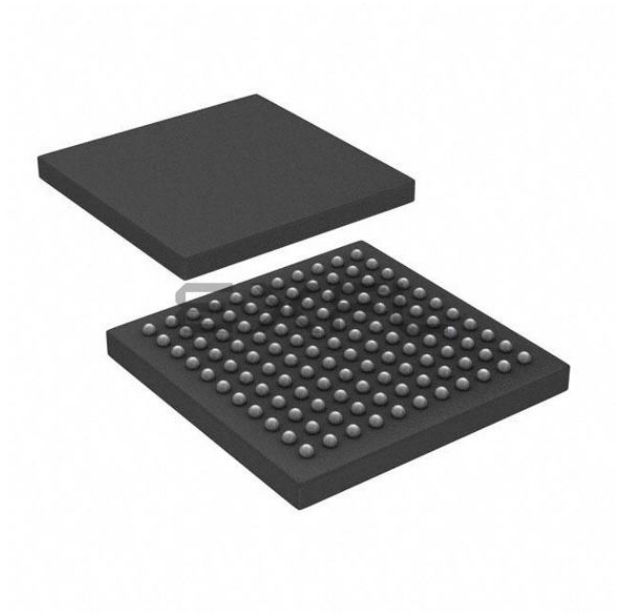

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

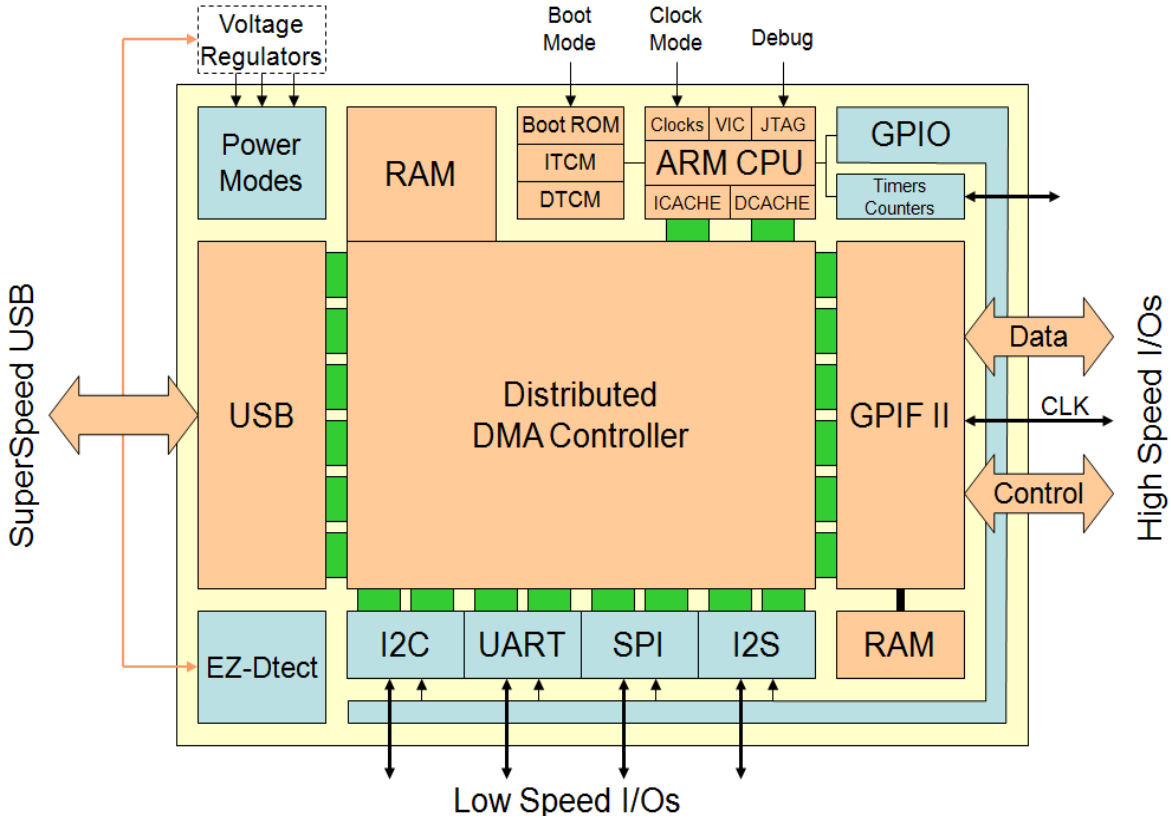
**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | SuperSpeed USB Peripheral Controller |
| Core Processor | ARM9® |
| Program Memory Type | External Program Memory |
| Controller Series | CYUSB |
| RAM Size | 512K x 8 |
| Interface | I²C, I²S, MMC/SD, SPI, UART, USB |
| Number of I/O | 59 |
| Voltage - Supply | 1.15V ~ 1.25V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-FBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cyusb2014-bzxit |

## Logic Block Diagram



## More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right <product> device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA87889, How to design with FX3/FX3S.

- Overview: USB Portfolio, USB Roadmap
- USB 3.0 Product Selectors: FX3, FX3S, CX3, HX3, West Bridge Benicia
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX3 are:
  - AN75705 - Getting Started with EZ-USB FX3
  - AN76405 - EZ-USB FX3 Boot Options
  - AN70707 - EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist
  - AN65974 - Designing with the EZ-USB FX3 Slave FIFO Interface
  - AN75779 - How to Implement an Image Sensor Interface with EZ-USB FX3 in a USB Video Class (UVC) Framework
  - AN86947 - Optimizing USB 3.0 Throughput with EZ-USB FX3
  - AN84868 - Configuring an FPGA over USB Using Cypress EZ-USB FX3
  - AN68829 - Slave FIFO Interface for EZ-USB FX3: 5-Bit Address Mode
  - AN73609 - EZ-USB FX2LP/ FX3 Developing Bulk-Loop Example on Linux
  - AN77960 - Introduction to EZ-USB FX3 High-Speed USB Host Controller
  - AN76348 - Differences in Implementation of EZ-USB FX2LP and EZ-USB FX3 Applications
  - AN89661 - USB RAID 1 Disk Design Using EZ-USB FX3S
- Code Examples: < Modify as required >
  - USB Hi-Speed
  - USB Full-Speed
  - USB SuperSpeed
- Technical Reference Manual (TRM):
  - EZ-USB FX3 Technical Reference Manual
- Development Kits:
  - CYUSB3KIT-003, EZ-USB FX3 SuperSpeed Explorer Kit
  - CYUSB3KIT-001, EZ-USB FX3 Development Kit
- Models: IBIS

### EZ-USB FX3 Software Development Kit

Cypress delivers the complete software and firmware stack for FX3, in order to easily integrate SuperSpeed USB into any embedded application. The Software Development Kit (SDK) comes with tools, drivers and application examples, which help accelerate application development.

### GPIF™ II Designer

The GPIF II Designer is a graphical software that allows designers to configure the GPIF II interface of the EZ-USB FX3 USB 3.0 Device Controller.

The tool allows users the ability to select from one of five Cypress supplied interfaces, or choose to create their own GPIF II interface from scratch. Cypress has supplied industry standard interfaces such as Asynchronous and Synchronous Slave FIFO, Asynchronous and Synchronous SRAM, and Asynchronous SRAM. Designers who already have one of these pre-defined interfaces in their system can simply select the interface of choice, choose from a set of standard parameters such as bus width (x8, 16, x32) endianess, clock settings, and compile the interface. The tool has a streamlined three step GPIF interface development process for users who need a customized interface. Users are able to first select their pin configuration and standard parameters. Secondly, they can design a virtual state machine using configurable actions. Finally, users can view output timing to verify that it matches the expected timing. Once the three step process is complete, the interface can be compiled and integrated with FX3.

## GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here is a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, 24-bit, and 32-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 14 configurable control pins when a 32- bit data bus is used. All control pins can be either input/output or bidirectional.
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 KB of memory (separate from the 256/512 KB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

Cypress's GPIFII Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

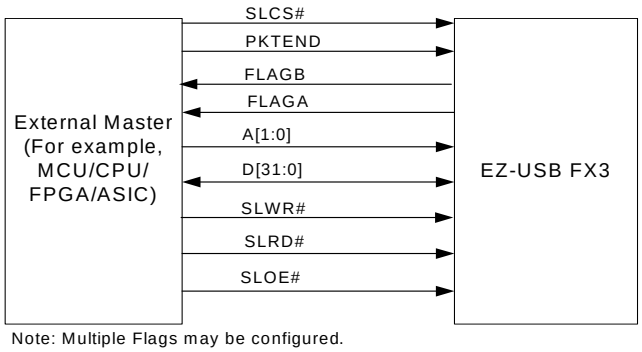
Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

*Slave FIFO interface*

The Slave FIFO interface signals are shown in Figure 5. This interface allows an external processor to directly access up to four buffers internal to FX3. Further details of the Slave FIFO interface are described on page 24.

**Note** Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Cypress Applications Support.

**Figure 5. Slave FIFO Interface**




Note: Multiple Flags may be configured.

## CPU

FX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 KB of Instruction Tightly Coupled Memory (TCM) and 8 KB of Data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

FX3 offers the following advantages:

- Integrates 256/512 KB of embedded SRAM for code and data and 8 KB of Instruction cache and Data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, GPIF II, $I^2S$, SPI, UART, $I^2C$), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development using industry-standard development tools for ARM926EJ-S.

Examples of the FX3 firmware are available with the Cypress EZ-USB FX3 Development Kit.

## JTAG Interface

FX3's JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core's on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the FX3 application development.

## Other Interfaces

FX3 supports the following serial peripherals:

- SPI
- UART
- $I^2C$
- $I^2S$

The SPI, UART, and $I^2S$ interfaces are multiplexed on the serial peripheral port.

The CYUSB3012 and CYUSB3014 Pin List on page 15 shows details of how these interfaces are multiplexed. Note that when GPIF II is configured for a 32-bit data bus width (CYUSB3012 and CYUSB3014), then the SPI interface is not available.

### SPI Interface

FX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 40 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from four bits to 32 bits.

## Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 3.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in Table 4 on page 10.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

**Table 3. Crystal/Clock Frequency Selection**

| FSLC[2] | FSLC[1] | FSLC[0] | Crystal/Clock Frequency |
|---|---|---|---|
| 0 | 0 | 0 | 19.2-MHz crystal |
| 1 | 0 | 0 | 19.2-MHz input CLK |
| 1 | 0 | 1 | 26-MHz input CLK |
| 1 | 1 | 0 | 38.4-MHz input CLK |
| 1 | 1 | 1 | 52-MHz input CLK |

**Table 4. FX3 Input Clock Specifications**

| Parameter | Description | Specification | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| Phase noise | 100-Hz offset | – | –75 | dB |
| | 1-kHz offset | – | –104 | |
| | 10-kHz offset | – | –120 | |
| | 100-kHz offset | – | –128 | |
| | 1-MHz offset | – | –130 | |
| Maximum frequency deviation | – | – | 150 | ppm |
| Duty cycle | – | 30 | 70 | % |
| Overshoot | – | – | 3 | |
| Undershoot | – | – | –3 | |
| Rise time/fall time | – | – | 3 | ns |

### 32-kHz Watchdog Timer Clock Input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer. Requirements for the optional 32-kHz clock input are listed in Table 5.

**Table 5. 32-kHz Clock Input Requirements**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Duty cycle | 40 | 60 | % |
| Frequency deviation | – | ±200 | ppm |
| Rise time/fall time | – | 200 | ns |

## Pin Configurations

**Figure 6. FX3 121-ball BGA Ball Map (Top View)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | U3VSSQ | U3RXVDDQ | SSRXM | SSRXP | SSTXP | SSTXM | AVDD | VSS | DP | DM | NC |
| B | VIO4 | FSLC[0] | R_USB3 | FSLC[1] | U3TXVDDQ | CVDDQ | AVSS | VSS | VSS | VDD | TRST# |
| C | GPIO[54] | GPIO[55] | VDD | GPIO[57] | RESET# | XTALIN | XTALOUT | R_USB2 | OTG_ID | TDO | VIO5 |
| D | GPIO[50] | GPIO[51] | GPIO[52] | GPIO[53] | GPIO[56] | CLKIN_32 | CLKIN | VSS | I2C_GPIO[58] | I2C_GPIO[59] | O[60] |
| E | GPIO[47] | VSS | VIO3 | GPIO[49] | GPIO[48] | FSLC[2] | TDI | TMS | VDD | VBATT | VBUS |
| F | VIO2 | GPIO[45] | GPIO[44] | GPIO[41] | GPIO[46] | TCK | GPIO[2] | GPIO[5] | GPIO[1] | GPIO[0] | VDD |
| G | VSS | GPIO[42] | GPIO[43] | GPIO[30] | GPIO[25] | GPIO[22] | GPIO[21] | GPIO[15] | GPIO[4] | GPIO[3] | VSS |
| H | VDD | GPIO[39] | GPIO[40] | GPIO[31] | GPIO[29] | GPIO[26] | GPIO[20] | GPIO[24] | GPIO[7] | GPIO[6] | VIO1 |
| J | GPIO[38] | GPIO[36] | GPIO[37] | GPIO[34] | GPIO[28] | GPIO[16] | GPIO[19] | GPIO[14] | GPIO[9] | GPIO[8] | VDD |
| K | GPIO[35] | GPIO[33] | VSS | VSS | GPIO[27] | GPIO[23] | GPIO[18] | GPIO[17] | GPIO[13] | GPIO[12] | GPIO[10] |
| L | VSS | VSS | VSS | GPIO[32] | VDD | VSS | VDD | INT# | VIO1 | GPIO[11] | VSS |

**Figure 7. FX3 131-Ball WLCSP Ball Map (Bottom View)**

| | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VSS | SSRXM | | SSTXM | FSLC[0] | AVSS | AVDD | DP | VSS | DM | VDD |
| B | GPIO[55] | VIO4 | SSRXP | R_USB3 | SSTXP | FSLC[2] | XTALIN | XTALOUT | NC | R_USB2 | NC | VDD |
| C | GPIO[56] | VIO3 | U3RXVDDQ | U3VSSQ | U3TXVDDQ | CVDDQ | CLKIN_32 | CLKIN | VSS | OTG_ID | TDO | TRST# |
| D | GPIO[49] | GPIO[50] | GPIO[53] | GPIO[54] | RESET# | VDD | I2C_GPIO[58] | TMS | VIO5 | TCK | I2C_GPIO[59] | VSS |
| E | GPIO[57] | GPIO[48] | GPIO[51] | GPIO[52] | O[60] | VSS | VSS | VSS | VSS | GPIO[3] | VBATT | VBUS |
| F | VSS | GPIO[46] | GPIO[47] | FSLC[1] | TDI | VDD | VDD | VDD | VDD | GPIO[4] | GPIO[1] | GPIO[0] |
| G | VIO2 | GPIO[43] | GPIO[44] | GPIO[45] | VSS | VSS | VDD | VSS | GPIO[9] | GPIO[7] | GPIO[6] | GPIO[2] |
| H | VSS | GPIO[40] | GPIO[41] | GPIO[42] | GPIO[39] | VSS | GPIO[20] | GPIO[18] | GPIO[14] | GPIO[12] | GPIO[8] | VIO1 |
| J | VIO2 | GPIO[38] | GPIO[37] | GPIO[36] | GPIO[31] | GPIO[27] | GPIO[25] | GPIO[22] | GPIO[19] | GPIO[15] | GPIO[10] | GPIO[5] |
| K | GPIO[35] | GPIO[34] | GPIO[33] | GPIO[32] | GPIO[28] | GPIO[26] | GPIO[16] | GPIO[21] | INT# | GPIO[24] | GPIO[11] | VSS |
| L | VDD | VSS | VDD | GPIO[30] | GPIO[29] | VIO1 | GPIO[23] | VSS | VIO1 | GPIO[17] | GPIO[13] | VSS |

**Note** No ball is populated at location A9.

**Figure 8. FX3 Hi-Speed 121-Ball BGA Ball Map (Top View)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | U3VSSQ | VDD | NC | NC | NC | NC | AVDD | VSS | DP | DM | NC |
| B | VIO4 | FSLC[0] | NC | FSLC[1] | VDD | CVDDQ | AVSS | VSS | VSS | VDD | TRST# |
| C | GPIO[54] | GPIO[55] | VDD | GPIO[57] | RESET# | XTALIN | XTALOUT | R_USB2 | OTG_ID | TDO | VIO5 |
| D | GPIO[50] | GPIO[51] | GPIO[52] | GPIO[53] | GPIO[56] | CLKIN_32 | CLKIN | VSS | I2C_GPIO[58] | I2C_GPIO[59] | O[60] |
| E | GPIO[47] | VSS | VIO3 | GPIO[49] | GPIO[48] | FSLC[2] | TDI | TMS | VDD | VBATT | VBUS |
| F | VIO2 | GPIO[45] | GPIO[44] | GPIO[41] | GPIO[46] | TCK | GPIO[2] | GPIO[5] | GPIO[1] | GPIO[0] | VDD |
| G | VSS | GPIO[42] | GPIO[43] | GPIO[30] | GPIO[25] | GPIO[22] | GPIO[21] | GPIO[15] | GPIO[4] | GPIO[3] | VSS |
| H | VDD | GPIO[39] | GPIO[40] | GPIO[31] | GPIO[29] | GPIO[26] | GPIO[20] | GPIO[24] | GPIO[7] | GPIO[6] | VIO1 |
| J | GPIO[38] | GPIO[36] | GPIO[37] | GPIO[34] | GPIO[28] | GPIO[16] | GPIO[19] | GPIO[14] | GPIO[9] | GPIO[8] | VDD |
| K | GPIO[35] | GPIO[33] | VSS | VSS | GPIO[27] | GPIO[23] | GPIO[18] | GPIO[17] | GPIO[13] | GPIO[12] | GPIO[10] |
| L | VSS | VSS | VSS | GPIO[32] | VDD | VSS | VDD | INT# | VIO1 | GPIO[11] | VSS |

**Table 7. CYUSB3012 and CYUSB3014 Pin List** (continued)

| BGA | WLCSP | Power Domain | I/O | Name | Description | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| J1 | J11 | VIO2 | I/O | GPIO[38] | DQ[21] | GPIO | GPIO | GPIO | GPIO | GPIO |
| H2 | H8 | VIO2 | I/O | GPIO[39] | DQ[22] | GPIO | GPIO | GPIO | GPIO | GPIO |
| H3 | H11 | VIO2 | I/O | GPIO[40] | DQ[23] | GPIO | GPIO | GPIO | GPIO | GPIO |
| F4 | H10 | VIO2 | I/O | GPIO[41] | DQ[24] | GPIO | GPIO | GPIO | GPIO | GPIO |
| G2 | H9 | VIO2 | I/O | GPIO[42] | DQ[25] | GPIO | GPIO | GPIO | GPIO | GPIO |
| G3 | G11 | VIO2 | I/O | GPIO[43] | DQ[26] | GPIO | GPIO | GPIO | GPIO | GPIO |
| F3 | G10 | VIO2 | I/O | GPIO[44] | DQ[27] | GPIO | GPIO | GPIO | GPIO | GPIO |
| F2 | G09 | VIO2 | I/O | GPIO[45] | GPIO | GPIO | GPIO | GPIO | GPIO | GPIO |
| F5 | F11 | VIO3 | I/O | GPIO[46] | DQ[28] | UART_RT S | GPIO | GPIO | GPIO | GPIO |
| E1 | F10 | VIO3 | I/O | GPIO[47] | DQ[29] | UART_CT S | GPIO | GPIO | GPIO | GPIO |
| E5 | E11 | VIO3 | I/O | GPIO[48] | DQ[30] | UART_TX | GPIO | GPIO | GPIO | GPIO |
| E4 | D12 | VIO3 | I/O | GPIO[49] | DQ[31] | UART_R X | GPIO | GPIO | GPIO | GPIO |
| D1 | D11 | VIO3 | I/O | GPIO[50] | I2S_CLK | I2S_CLK | GPIO | GPIO | GPIO | GPIO |
| D2 | E10 | VIO3 | I/O | GPIO[51] | I2S_SD | I2S_SD | GPIO | GPIO | GPIO | GPIO |
| D3 | E9 | VIO3 | I/O | GPIO[52] | I2S_WS | I2S_WS | GPIO | GPIO | GPIO | GPIO |
| D4 | D10 | VIO4 | I/O | GPIO[53] | UART_RTS | SPI_SCK | UART_RTS | SPI_SCK | GPIO | GPIO |
| C1 | D9 | VIO4 | I/O | GPIO[54] | UART_CTS | SPI_SSN | UART_CTS | SPI_SSN | I2S_CLK | GPIO |
| C2 | B12 | VIO4 | I/O | GPIO[55] | UART_TX | SPI_MIS O | UART_TX | SPI_MISO | I2S_SD | GPIO |
| D5 | C12 | VIO4 | I/O | GPIO[56] | UART_RX | SPI_MOS I | UART_RX | SPI_MOSI | I2S_WS | GPIO |
| C4 | E12 | VIO4 | I/O | GPIO[57] | I2S_MCLK | I2S_MCL K | GPIO | GPIO | I2S_MCL K | GPIO |
| | | | | | **USB Port** | | | | | |
| | | | | | **CYUSB301X** | | | **CYUSB201X** | | |
| A3 | A10 | U3RXVD DQ | I | SSRXM | SSRX- | | | NC | | |
| A4 | B10 | U3RXVD DQ | I | SSRXP | SSRX+ | | | NC | | |
| A6 | A8 | U3TXVD DQ | O | SSTXM | SSTX- | | | NC | | |
| A5 | B8 | U3TXVD DQ | O | SSTXP | SSTX+ | | | NC | | |
| B3 | B9 | U3TXVD DQ | I/O | R_usb3 | Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND) | | | NC | | |
| C9 | C3 | VBUS/ VBATT | I | OTG_ID | OTG_ID | | | | | |
| A9 | A4 | VBUS/V BATT | I/O | DP | D+ | | | | | |
| A10 | A2 | VBUS/V BATT | I/O | DM | D– | | | | | |
| C8 | B3 | VBUS/VBAT T | I/O | R_usb2 | Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND) | | | | | |
| | | | | | **Clock and Reset** | | | | | |
| B2 | A7 | CVDDQ | I | FSLC[0] | FSLC[0] | | | | | |
| C6 | B6 | AVDD | I/O | XTALIN | XTALIN | | | | | |
| C7 | B5 | AVDD | I/O | XTALOUT | XTALOUT | | | | | |
| B4 | F9 | CVDDQ | I | FSLC[1] | FSLC[1] | | | | | |
| E6 | B7 | CVDDQ | I | FSLC[2] | FSLC[2] | | | | | |
| D7 | C5 | CVDDQ | I | CLKIN | CLKIN | | | | | |

**Table 7. CYUSB3012 and CYUSB3014 Pin List** (continued)

| BGA | WLCSP | Power Domain | I/O | Name | Description |
|---|---|---|---|---|---|
| D6 | C6 | CVDDQ | I | CLKIN_32 | CLKIN_32 |
| C5 | D8 | CVDDQ | I | RESET# | RESET# |
| | | | | | **I2C and JTAG** |
| D9 | D6 | VIO5 | I/O | I2C_GPIO[58] | $I^2C$_SCL |
| D10 | D2 | VIO5 | I/O | I2C_GPIO[59] | $I^2C$_SDA |
| E7 | F8 | VIO5 | I | TDI | TDI |
| C10 | C2 | VIO5 | O | TDO | TDO |
| B11 | C1 | VIO5 | I | TRST# | TRST# |
| E8 | D5 | VIO5 | I | TMS | TMS |
| F6 | D3 | VIO5 | I | TCK | TCK |
| D11 | E8 | VIO5 | O | O[60] | Charger detect output |
| | | | | | **Power** |
| E10 | E2 | – | PWR | VBATT | – |
| B10 | B1 | – | PWR | VDD | – |
| – | A1 | – | PWR | VDD | – |
| A1 | C9 | – | PWR | U3VSSQ | – |
| E11 | E1 | – | PWR | VBUS | – |
| D8 | C4 | – | PWR | VSS | – |
| H11 | H1 | – | PWR | VIO1 | – |
| E2 | K1 | – | PWR | VSS | – |
| L9 | L4 | – | PWR | VIO1 | – |
| G1 | L5 | – | PWR | VSS | – |
| – | L7 | – | PWR | VIO1 | – |
| – | L1 | – | PWR | VSS | – |
| F1 | J12 | – | PWR | VIO2 | – |
| G11 | H12 | – | PWR | VSS | – |
| | G12 | – | PWR | VIO2 | – |
| E3 | C11 | – | PWR | VIO3 | – |
| L1 | F12 | – | PWR | VSS | – |
| B1 | B11 | – | PWR | VIO4 | – |
| L6 | A11 | – | PWR | VSS | – |
| – | A12 | – | PWR | VSS | – |
| B6 | C7 | – | PWR | CVDDQ | – |
| B5 | C8 | – | PWR | U3TXVDDQ | – |
| A2 | C10 | – | PWR | U3RXVDDQ | – |
| C11 | D4 | – | PWR | VIO5 | – |
| L11 | A3 | – | PWR | VSS | – |
| A7 | A5 | – | PWR | AVDD | – |
| B7 | A6 | – | PWR | AVSS | – |
| C3 | F4 | – | PWR | VDD | – |
| B8 | D1 | – | PWR | VSS | – |
| E9 | F5 | – | PWR | VDD | – |

**Figure 10. GPIF II Timing in Asynchronous Mode**

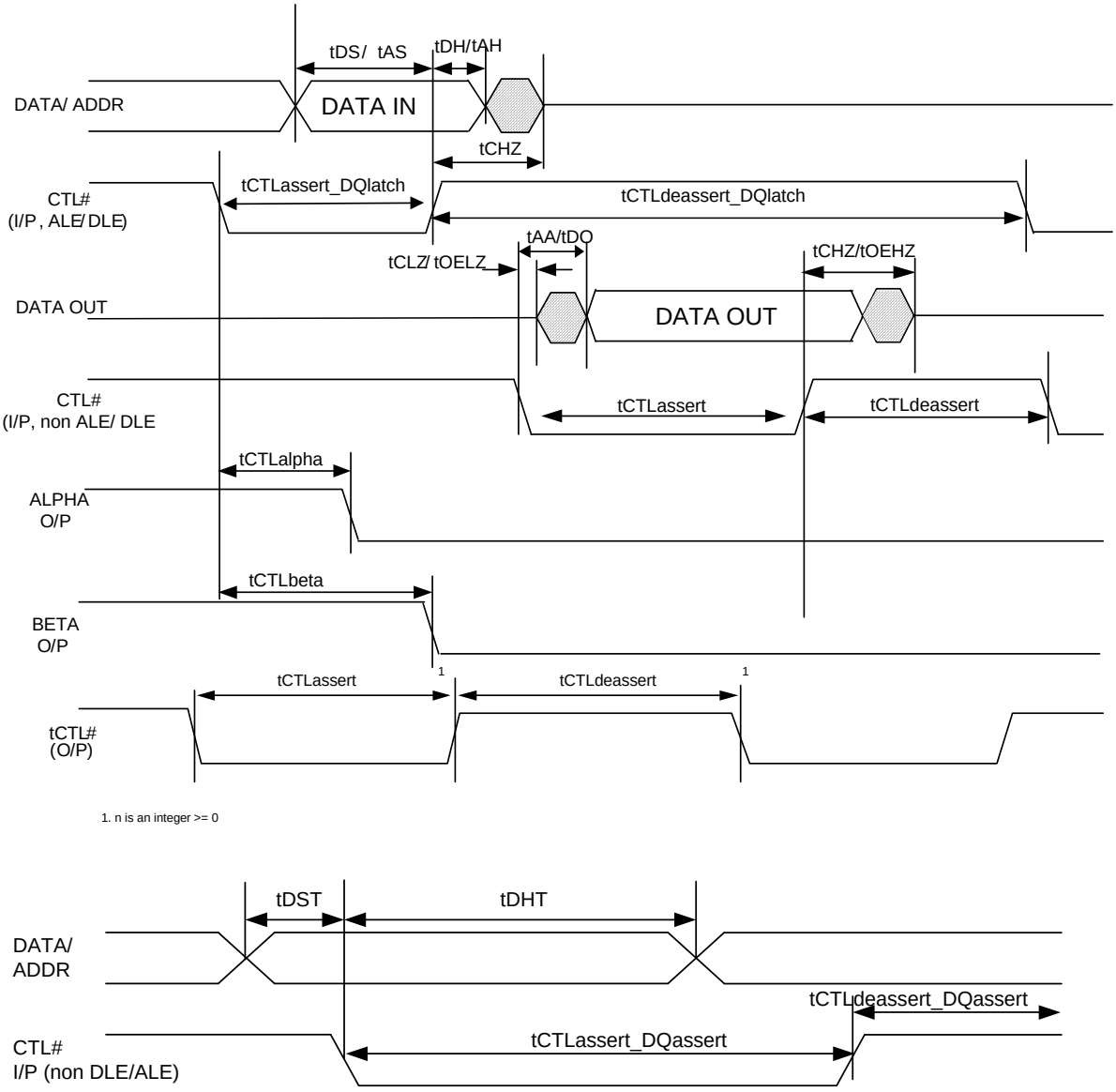
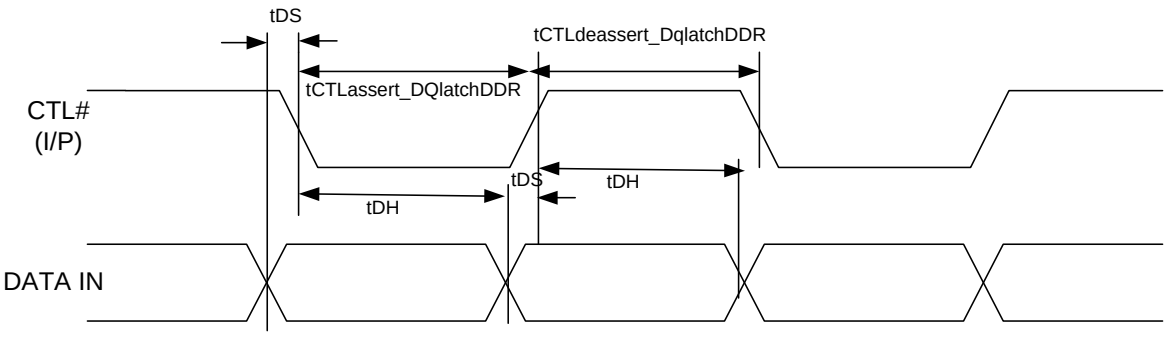






**Figure 11. GPIF II Timing in Asynchronous DDR Mode**



*Synchronous Slave FIFO Write Sequence Description*

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of $t_{WFLG}$ from the rising edge of the clock

The same sequence of events is also applicable for burst write

**Note** For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

**Short Packet:** A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

**Zero-Length Packet:** The external device or processor can signal a Zero-Length Packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in Figure 13.

**Figure 13. Synchronous Slave FIFO Write Mode**

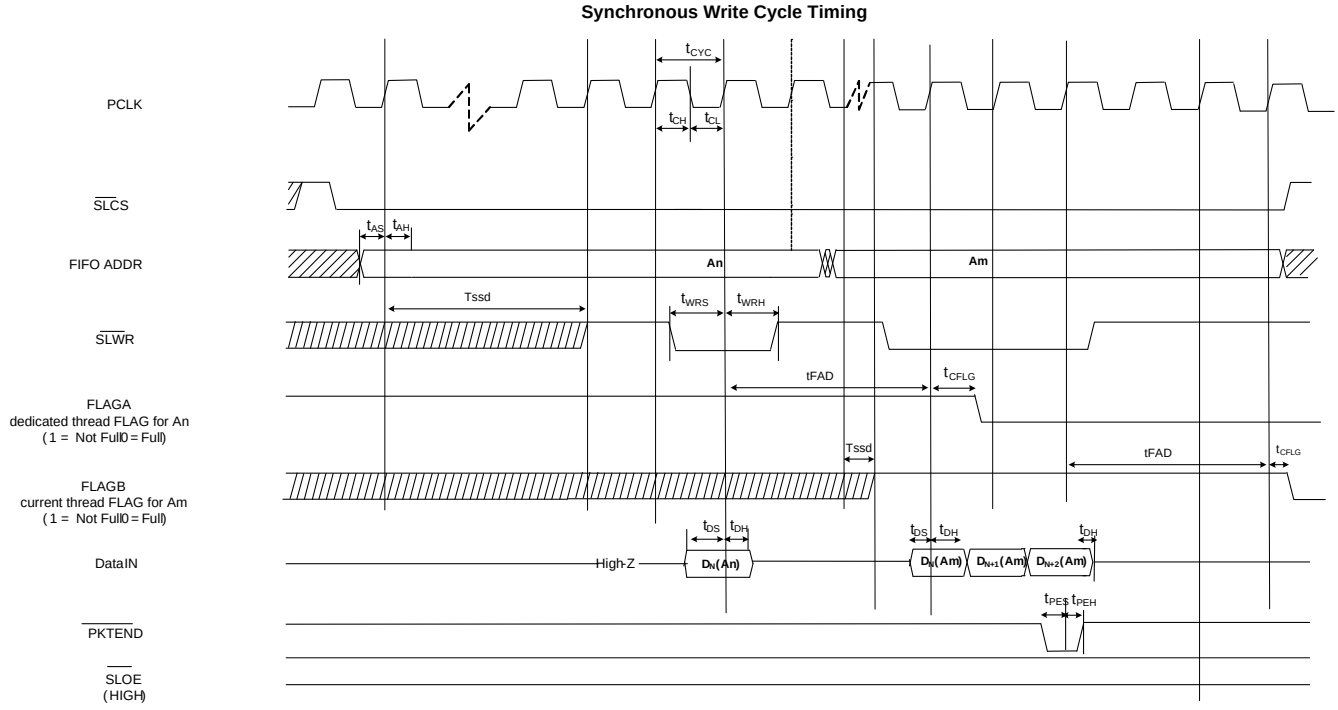


**Figure 14. Synchronous Slave FIFO ZLP Write Cycle Timing**

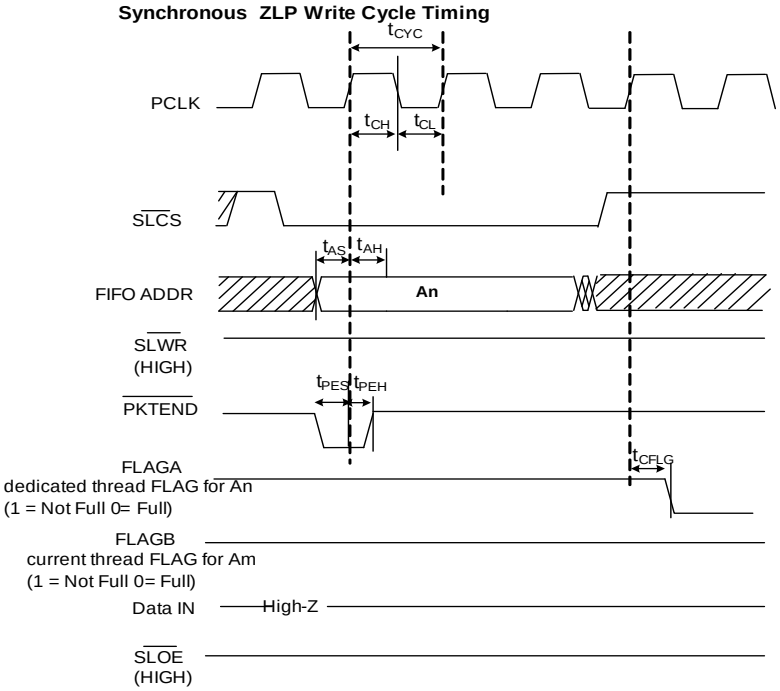



**Table 11. Synchronous Slave FIFO Parameters**[5]

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| FREQ | Interface clock frequency | – | 100 | MHz |
| tCYC | Clock period | 10 | – | ns |
| tCH | Clock high time | 4 | – | ns |
| tCL | Clock low time | 4 | – | ns |
| tRDS | SLRD# to CLK setup time | 2 | – | ns |
| tRDH | SLRD# to CLK hold time | 0.5 | – | ns |
| tWRS | SLWR# to CLK setup time | 2 | – | ns |
| tWRH | SLWR# to CLK hold time | 0.5 | – | ns |
| tCO | Clock to valid data | – | 7 | ns |
| tDS | Data input setup time | 2 | – | ns |
| tDH | CLK to data input hold | 0.5 | – | ns |
| tAS | Address to CLK setup time | 2 | – | ns |
| tAH | CLK to address hold time | 0.5 | – | ns |
| tOELZ | SLOE# to data low-Z | 0 | – | ns |
| tCFLG | CLK to flag output propagation delay | – | 8 | ns |
| tOEZ | SLOE# deassert to Data Hi Z | – | 8 | ns |
| tPES | PKTEND# to CLK setup | 2 | – | ns |
| tPEH | CLK to PKTEND# hold | 0.5 | – | ns |
| tCDH | CLK to data output hold | 2 | – | ns |
| tSSD | Socket switching delay | 2 | 68 | Clock cycles |
| tACCD | Latency from SLRD# to Data | 2 | 2 | Clock cycles |
| tFAD | Latency from SLWR# to FLAG | 3 | 3 | Clock cycles |
| **Note** Three-cycle latency from ADDR to DATA/FLAGS. | | | | |

**Note**
5. All parameters guaranteed by design and validated through characterization.

## Host Processor Interface (P-Port) Timing

*Asynchronous SRAM Timing*

**Figure 18. Non-multiplexed Asynchronous SRAM Read Timing**

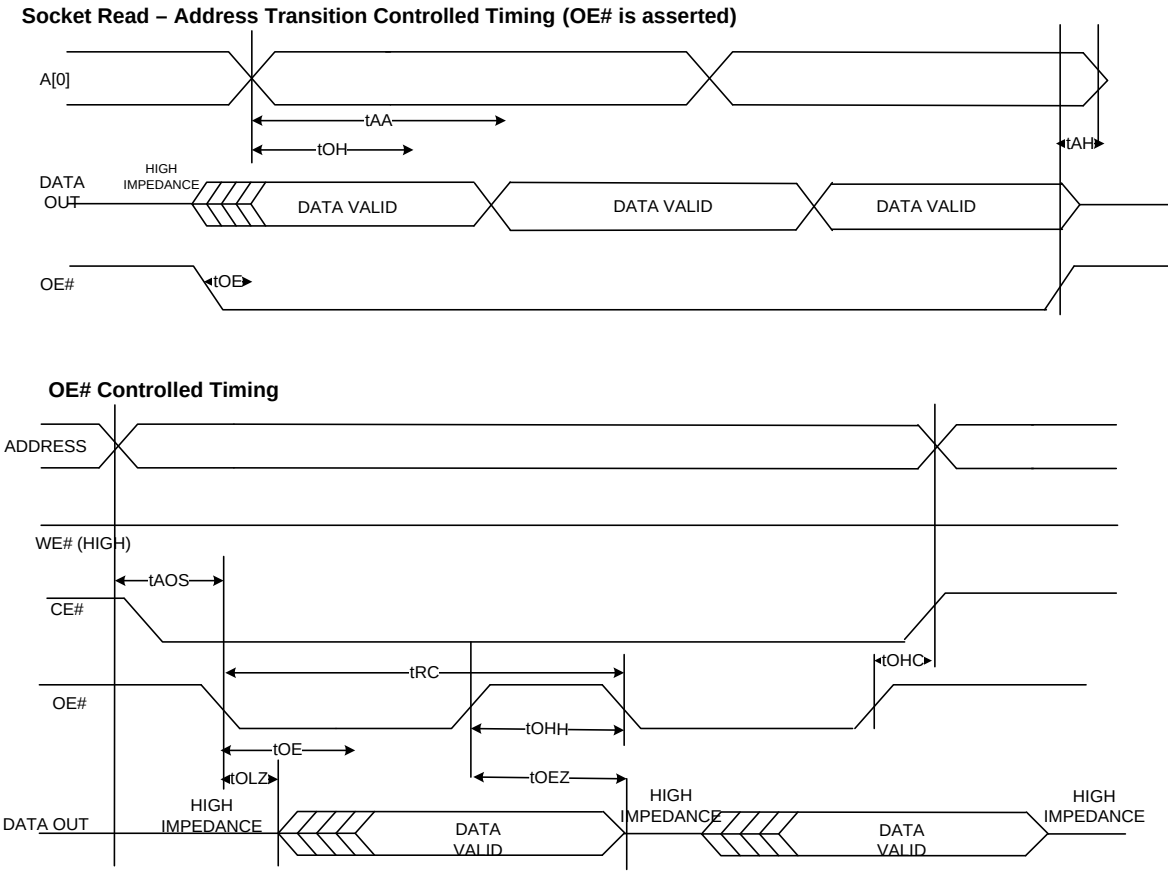
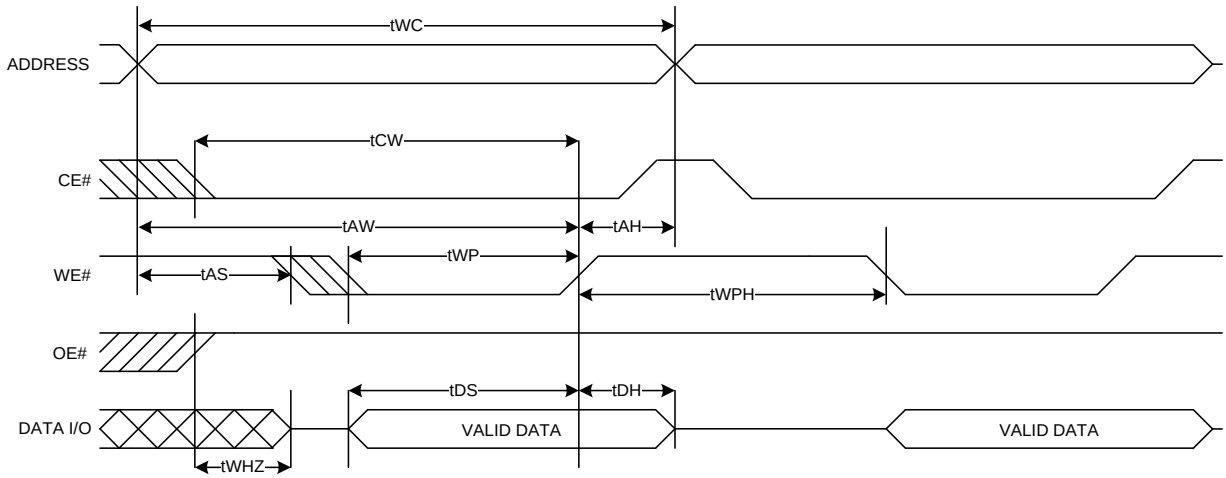


**Figure 19. Non-multiplexed Asynchronous SRAM Write Timing (WE# and CE# Controlled)**

**Write Cycle 1 WE# Controlled, OE# High During Write**




**Write Cycle 2 CE# Controlled, OE# High During Write**

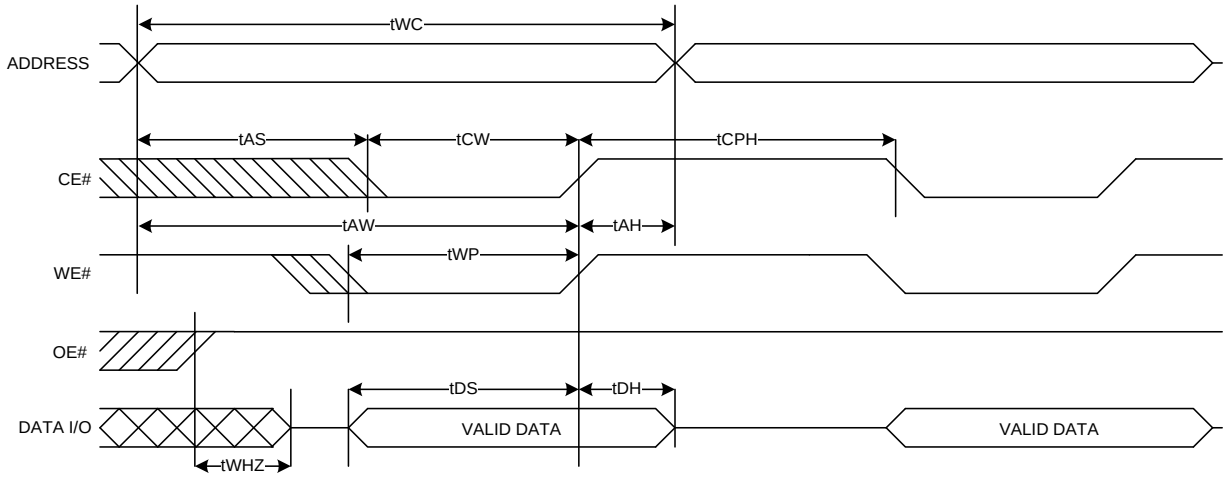


**Table 14. Asynchronous ADMux Timing Parameters**[8]

| Parameter | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **ADMux Asynchronous READ Access Timing Parameters** | | | | | |
| tRC | Read cycle time (address valid to address valid) | 54.5 | – | ns | This parameter is dependent on when the P-port processors deasserts OE# |
| tACC | Address valid to data valid | – | 32 | ns | – |
| tCO | CE# assert to data valid | – | 34.5 | ns | – |
| tAVOE | ADV# deassert to OE# assert | 2 | – | ns | – |
| tOLZ | OE# assert to data LOW-Z | 0 | – | ns | – |
| tOE | OE# assert to data valid | – | 25 | ns | – |
| tHZ | Read cycle end to data HIGH-Z | – | 22.5 | ns | – |
| **ADMux Asynchronous WRITE Access Timing Parameters** | | | | | |
| tWC | Write cycle time (Address Valid to Address Valid) | – | 52.5 | ns | – |
| tAW | Address valid to write end | 30 | – | ns | – |
| tCW | CE# assert to write end | 30 | – | ns | – |
| tAVWE | ADV# deassert to WE# assert | 2 | – | ns | – |
| tWP | WE# LOW pulse width | 20 | – | ns | – |
| tWPH | WE# HIGH pulse width | 10 | – | ns | – |
| tDS | Data valid setup to WE# deassert | 18 | – | ns | – |
| tDH | Data valid hold from WE# deassert | 2 | – | ns | – |
| **ADMux Asynchronous Common READ/WRITE Access Timing Parameters** | | | | | |
| tAVS | Address valid setup to ADV# deassert | 5 | – | ns | – |
| tAVH | Address valid hold from ADV# deassert | 2 | – | ns | – |
| tVP | ADV# LOW pulse width | 7.5 | – | ns | – |
| tCPH | CE# HIGH pulse width | 10 | – | ns | – |
| tVPH | ADV# HIGH pulse width | 15 | – | ns | – |
| tCEAV | CE# assert to ADV# assert | 0 | – | ns | – |

**Note**
8. All parameters guaranteed by design and validated through characterization.

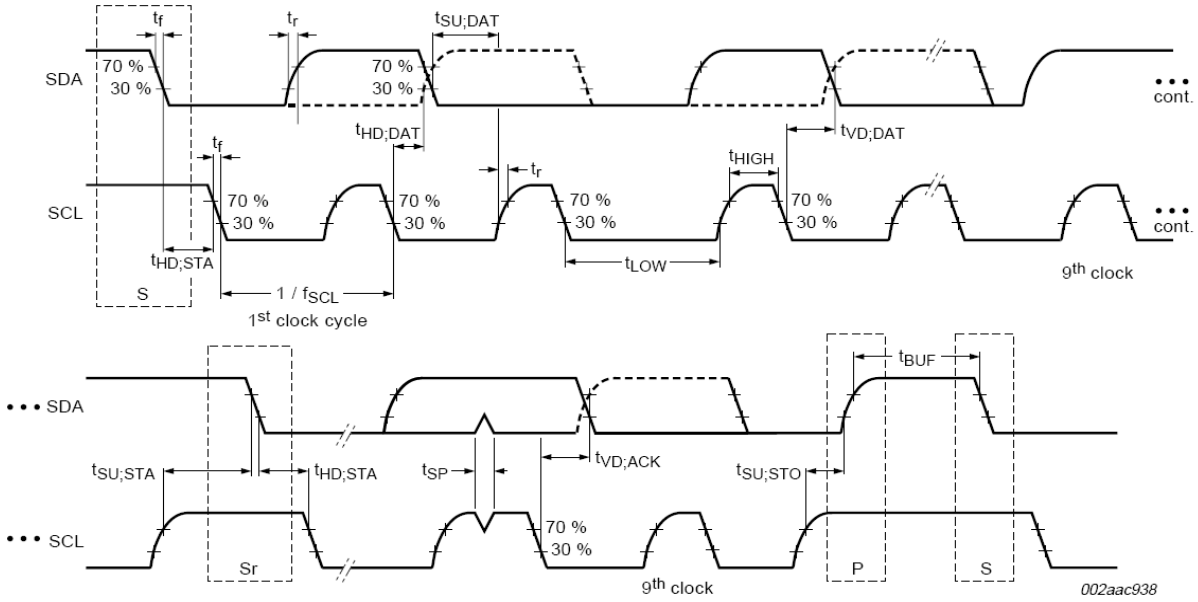
**Table 15. Synchronous ADMux Timing Parameters**[9]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| FREQ | Interface clock frequency | – | 100 | MHz |
| tCLK | Clock period | 10 | – | ns |
| tCLKH | Clock HIGH time | 4 | – | ns |
| tCLKL | Clock LOW time | 4 | – | ns |
| tS | CE#/WE#/DQ setup time | 2 | – | ns |
| tH | CE#/WE#/DQ hold time | 0.5 | – | ns |
| tCH | Clock to data output hold time | 0 | – | ns |
| tDS | Data input setup time | 2 | – | ns |
| tDH | Clock to data input hold | 0.5 | – | ns |
| tAVDOE | ADV# HIGH to OE# LOW | 0 | – | ns |
| tAVDWE | ADV# HIGH to WE# LOW | 0 | – | ns |
| tHZ | CE# HIGH to Data HIGH-Z | – | 8 | ns |
| tOHZ | OE# HIGH to Data HIGH-Z | – | 8 | ns |
| tOLZ | OE# LOW to Data LOW-Z | 0 | – | ns |
| tKW | Clock to RDY valid | – | 8 | ns |

## Serial Peripherals Timing

*$I^2C$ Timing*

**Figure 27. $I^2C$ Timing Definition**




**Note**
9. All parameters guaranteed by design and validated through characterization.

**Table 16. I²C Timing Parameters**[10] (continued)

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| **I²C Fast Mode Plus Parameters** (Not supported at I2C_VDDQ=1.2 V) | | | | |
| fSCL | SCL clock frequency | 0 | 1000 | kHz |
| tHD:STA | Hold time START condition | 0.26 | – | µs |
| tLOW | LOW period of the SCL | 0.5 | – | µs |
| tHIGH | HIGH period of the SCL | 0.26 | – | µs |
| tSU:STA | Setup time for a repeated START condition | 0.26 | – | µs |
| tHD:DAT | Data hold time | 0 | – | µs |
| tSU:DAT | Data setup time | 50 | – | ns |
| tr | Rise time of both SDA and SCL signals | – | 120 | ns |
| tf | Fall time of both SDA and SCL signals | – | 120 | ns |
| tSU:STO | Setup time for STOP condition | 0.26 | – | µs |
| tBUF | Bus-free time between a STOP and START condition | 0.5 | – | µs |
| tVD:DAT | Data valid time | – | 0.45 | µs |
| tVD:ACK | Data valid ACK | – | 0.55 | µs |
| tSP | Pulse width of spikes that must be suppressed by input filter | 0 | 50 | ns |

*I²S Timing Diagram*

**Figure 28. I²S Transmit Cycle**

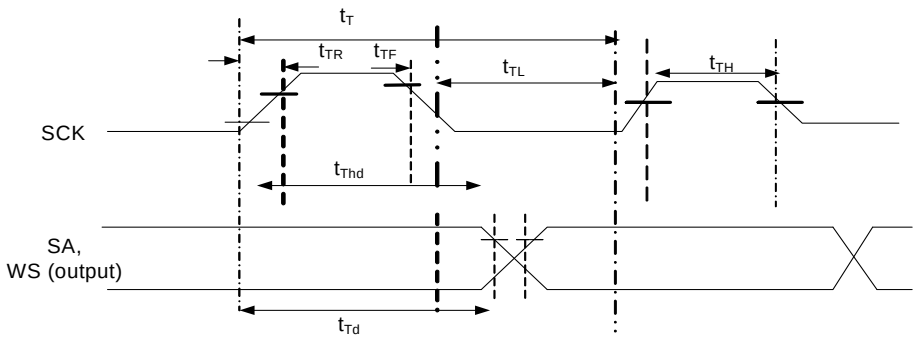



**Table 17. I²S Timing Parameters**[11]

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| tT | I²S transmitter clock cycle | Ttr | – | ns |
| tTL | I²S transmitter cycle LOW period | 0.35 Ttr | – | ns |
| tTH | I²S transmitter cycle HIGH period | 0.35 Ttr | – | ns |
| tTR | I²S transmitter rise time | – | 0.15 Ttr | ns |
| tTF | I²S transmitter fall time | – | 0.15 Ttr | ns |
| tThd | I²S transmitter data hold time | 0 | – | ns |
| tTd | I²S transmitter delay time | – | 0.8tT | ns |
| **Note** tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz). | | | | |

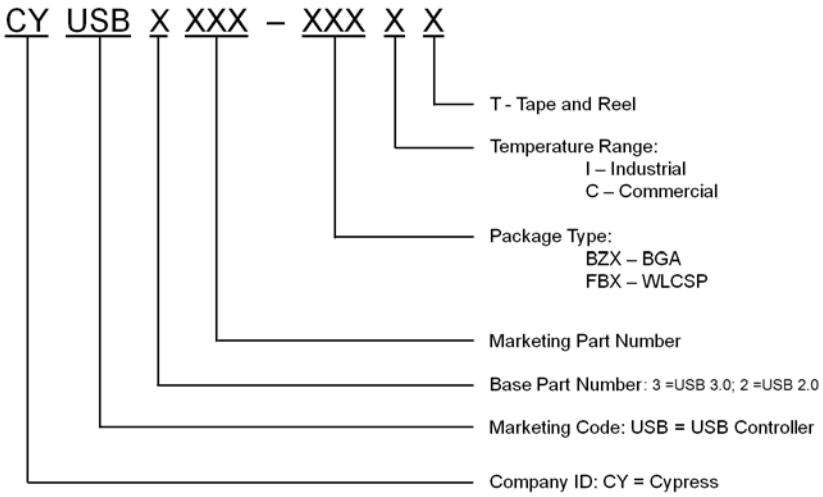
**Note**
11. All parameters guaranteed by design and validated through characterization.

## Ordering Information

**Table 20. Ordering Information**

| Ordering Code | USB | SRAM (kB) | GPIF II Data Bus Width | Operating Temperature | Package Type |
|---|---|---|---|---|---|
| CYUSB3011-BZXC | USB 3.0 | 256 | 16-bit | 0 °C to +70 °C | 121-ball BGA |
| CYUSB3012-BZXC | USB 3.0 | 256 | 32-bit | 0 °C to +70 °C | 121-ball BGA |
| CYUSB3013-BZXC | USB 3.0 | 512 | 16-bit | 0 °C to +70 °C | 121-ball BGA |
| CYUSB3014-BZXC | USB 3.0 | 512 | 32-bit | 0 °C to +70 °C | 121-ball BGA |
| CYUSB3014-BZXI | USB 3.0 | 512 | 32-bit | –40°C to +85°C | 121-ball BGA |
| CYUSB3014-FBXCT | USB 3.0 | 512 | 32-bit | 0 °C to +70 °C | 131-ball WLCSP |
| CYUSB3014-FBXIT | USB 3.0 | 512 | 32-bit | –40 °C to +85 °C | 131-ball WLCSP |
| CYUSB2014-BZXC | USB 2.0 | 512 | 32-bit | 0 °C to +70 °C | 121-ball BGA |
| CYUSB2014-BZXI | USB 2.0 | 512 | 32-bit | –40 °C to +85 °C | 121-ball BGA |

### Ordering Code Definitions



## Document History Page

| Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller<br>Document Number: 001-52136 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2669761 | VSO / PYRS | 03/06/2009 | New data sheet |
| *A | 2758370 | VSO | 09/01/2009 | Updated the part# from CYX01XXBB to CYUSB3011-BZXI<br>Changed the title from “ADVANCE” to “ADVANCE INFORMATION”<br>In page 1, the second bullet (Flexible Host Interface), add “32-bit, 100 MHz” to first sub bullet.<br>In page 1, changed the second bullet “Flexible Host Interface” to General Programmable Interface”.<br>In page 1, the second bullet (Flexible Host Interface), removed "DMA Slave Support” and "MMC Slave support with Pass through Boot" sub bullets.<br>In page 1, third bullet, changed "50 µA with Core Power" to "60 µA with Core Power"<br>In page 1, fifth bullet, added "at 1 MHz"<br>In page 1, seventh bullet, added "up to 4MHz" to UART<br>In page 1, Applications Section, move “Digital Still Cameras” to second line.<br>In page 1, Applications Section, added “Machine Vision” and Industrial Cameras”<br>Added ™ to GPIF and FX3.<br>In page 1, updated Logic Block Diagram.<br>In page 2, section of “Functional Overview”, updated the whole section.<br>In page 2, removed the section of “Product Interface”<br>In page 2, removed the section of “Processor Interface (P-Port)”<br>In page 2, removed the section of “USB Interface (U-Port)”<br>In page 2, removed the section of “Other Interfaces”<br>In page 2, added a section of "GPIF II"<br>In page 2, added a section of "CPU"<br>In page 2, added a section of "JTAG Interface"<br>In page 2, added a section of "Boot Options"<br>In page 2, added a section of "ReNumeration"<br>In page 2, added a section of "Power"<br>In the section of “Package”, replaced “West Bridge USB 3.0 Platform” by FX3.<br>In the section of “Package”, added 0.8 mm pitch in front of BGA.<br>Added Pin List (Table 1) |
| *B | 2779196 | VSO/PYRS | 09/29/2009 | Features:<br>Added the thrid bullet “Fully accessible 32-bit ARM9 core with 512kB of embedded SRAM”<br>Added the thrid line “EZ USB™ Software and DVK for easy code development”<br>Table 1: Pin 74, corrected to NC - No Connect.<br>Changed title to EZ-USB™ FX3: SuperSpeed USB Controller |
| *C | 2823531 | OSG | 12/08/2009 | Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates. |
| *D | 3080927 | OSG | 11/08/2010 | Changed status from Advance to Preliminary<br>Changed part number from CYUSB3011 to CYUSB3014<br>Added the following sections: Power, Digital I/Os, Digital I/Os, System-level ESD, Electrical Specifications, AC Timing Parameters, Reset Sequence, Package Diagram<br>Added DC Specifications table<br>Updated feature list<br>Updated Pin List<br>Added support for selectable clock input frequencies.<br>Updated block diagram<br>Updated part number<br>Updated package diagram |

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| Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller<br>Document Number: 001-52136 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *E | 3204393 | OSG | 03/24/2011 | Updated Slave FIFO protocol and added ZLP signaling protocol<br>Changed GPIFII asynchronous tDO parameter<br>Changed Async Slave FIFO tOE parameter<br>Changed Async Slave FIFO tRDO parameter<br>Added tCOE parameter to GPIFII Sync mode timing parameters<br>Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0<br>Modified description of GPIFII Sync tCO (previously tDO) parameter<br>Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge.<br>Correspondingly, changed the tAH number.<br>Removed 24 bit data bus support for GPIFII. |
| *F | 3219493 | OSG | 04/07/2011 | Minor ECN - Release to web. No content changes. |
| *G | 3235250 | GSZ | 04/20/2011 | Minor updates in Features. |
| *H | 3217917 | OSG | 04/06/2011 | Updated GPIFII Synchronous Timing diagram. Added SPI Boot option.<br>Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams.<br>Corrected Synchronous Slave FIFO tDH parameter. |
| *I | 3305568 | DSG | 07/07/2011 | Minor ECN - Correct ECN number in revision *F. No content changes. |
| *J | 3369042 | OSG | 12/06/2011 | Changed datasheet status from Preliminary to Final.<br>Changed tWRPE parameter to 2ns<br>Updated tRR and tRPW for crystal input<br>Added clarification regarding $I_{OZ}$ and $I_{IX}$<br>Updated Sync SLave FIFO Read timing diagram<br>Updated SPI timing diagram<br>Removed tGRANULARITY parameter<br>Updated I2S Timing diagram and tTd parameter<br>Updated 121-ball BGA package diagram.<br>Added clarification regarding VCC in DC Specifications table<br>In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application<br>Updated Absolute Maximum Ratings<br>Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$<br>Updated tPEI parameter in Async Slave FIFO timing table<br>Updated Sync Slave FIFO write and read timing diagrams<br>Updated I2C interface tVD:ACK parameter for 1MHz operation<br>Clarified that CTL[15] is not usable as a GPIO |
| *K | 3534275 | OSG | 02/24/2012 | Corrected typo in the block diagram. |
| *L | 3649782 | OSG | 08/16/2012 | Changed part number to CYUSB301X.<br>Added 256 KB range for embedded SRAM.<br>Updated Functional Overview, Other Interfaces, and Clocking sections.<br>Added Pin List for CYUSB3011 and CYUSB3013 parts.<br>Updated Ordering Information with new part numbers. |
| *M | 3848148 | OSG | 12/20/2012 | Updated 121-ball BGA package diagram to current revision. |
| *N | 4016006 | OSG | 05/31/2013 | Updated Features (Added 131-ball WLCSP under Package option).<br>Updated Pin Configurations (Added FX3 131-ball WLCSP Ball Map (Figure 7)).<br>Updated Pin Description (Updated Table 7).<br>Updated Electrical Specifications (Included Commercial Temperature Range related information).<br>Updated Operating Conditions (Included Commercial Temperature Range related information).<br>Updated Package Diagram (Added 131-ball WLCSP Package Diagram (Figure 32)).<br>Updated Ordering Information (Updated part numbers). |

## Document History Page (continued)

| Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller<br>Document Number: 001-52136 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *T | 5306567 | MDDD | 06/29/2016 | Updated AC Timing Parameters:<br>Updated GPIF II Timing:<br>Updated Table 9:<br>Changed maximum value of $t_{CO}$ parameter from 8 ns to 7 ns.<br>Updated Slave FIFO Interface:<br>Updated Synchronous Slave FIFO Write Sequence Description:<br>Updated Table 11:<br>Changed maximum value of $t_{CO}$ parameter from 8 ns to 7 ns.<br>Updated to new template. |
| *U | 5703914 | GNKK | 04/20/2017 | Updated the Cypress logo and copyright information. |

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