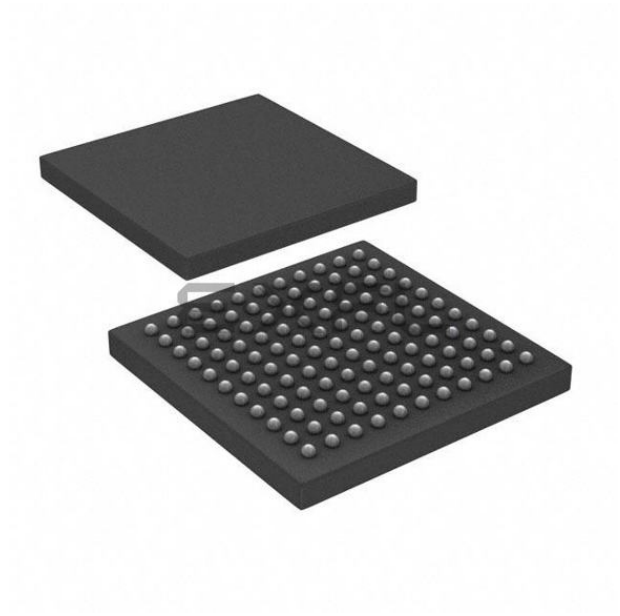

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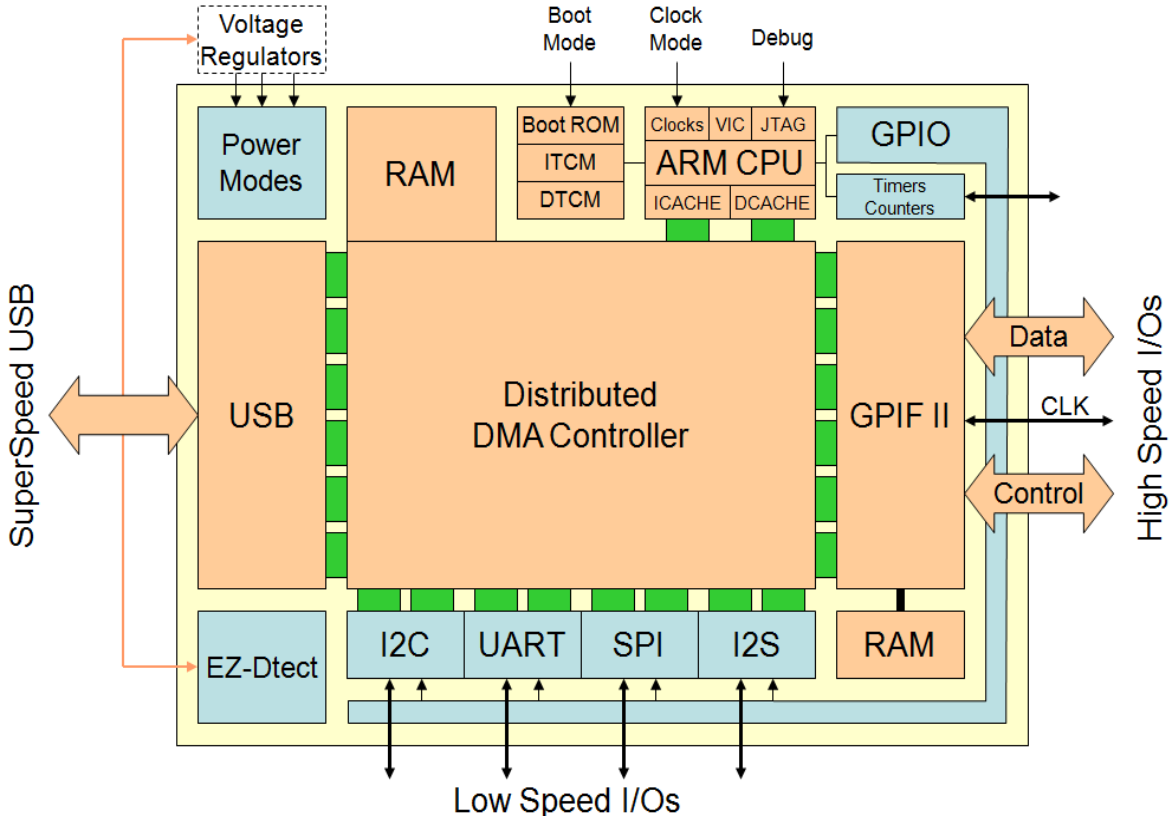
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	256K x 8
Interface	GPIF, I²C, I²S, SPI, UART, USB
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3011-bzxc

Logic Block Diagram



GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here is a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, 24-bit, and 32-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 14 configurable control pins when a 32- bit data bus is used. All control pins can be either input/output or bidirectional.
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 KB of memory (separate from the 256/512 KB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

Cypress's GPIFII Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

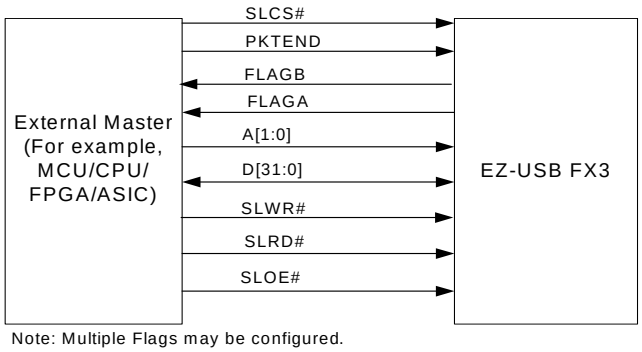
Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

Slave FIFO interface

The Slave FIFO interface signals are shown in Figure 5. This interface allows an external processor to directly access up to four buffers internal to FX3. Further details of the Slave FIFO interface are described on page 24.

Note Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Cypress Applications Support.

Figure 5. Slave FIFO Interface



Note: Multiple Flags may be configured.

CPU

FX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 KB of Instruction Tightly Coupled Memory (TCM) and 8 KB of Data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

FX3 offers the following advantages:

- Integrates 256/512 KB of embedded SRAM for code and data and 8 KB of Instruction cache and Data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, GPIF II, I^2S, SPI, UART, I^2C), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development using industry-standard development tools for ARM926EJ-S.

Examples of the FX3 firmware are available with the Cypress EZ-USB FX3 Development Kit.

JTAG Interface

FX3's JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core's on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the FX3 application development.

Other Interfaces

FX3 supports the following serial peripherals:

- SPI
- UART
- I^2C
- I^2S

The SPI, UART, and I^2S interfaces are multiplexed on the serial peripheral port.

The CYUSB3012 and CYUSB3014 Pin List on page 15 shows details of how these interfaces are multiplexed. Note that when GPIF II is configured for a 32-bit data bus width (CYUSB3012 and CYUSB3014), then the SPI interface is not available.

SPI Interface

FX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 40 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from four bits to 32 bits.

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See Pin Configurations for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Pin Configurations

Figure 6. FX3 121-ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 7. FX3 131-Ball WLCSP Ball Map (Bottom View)

	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	SSRXM		SSTXM	FSLC[0]	AVSS	AVDD	DP	VSS	DM	VDD
B	GPIO[55]	VIO4	SSRXP	R_USB3	SSTXP	FSLC[2]	XTALIN	XTALOUT	NC	R_USB2	NC	VDD
C	GPIO[56]	VIO3	U3RXVDDQ	U3VSSQ	U3TXVDDQ	CVDDQ	CLKIN_32	CLKIN	VSS	OTG_ID	TDO	TRST#
D	GPIO[49]	GPIO[50]	GPIO[53]	GPIO[54]	RESET#	VDD	I2C_GPIO[58]	TMS	VIO5	TCK	I2C_GPIO[59]	VSS
E	GPIO[57]	GPIO[48]	GPIO[51]	GPIO[52]	O[60]	VSS	VSS	VSS	VSS	GPIO[3]	VBATT	VBUS
F	VSS	GPIO[46]	GPIO[47]	FSLC[1]	TDI	VDD	VDD	VDD	VDD	GPIO[4]	GPIO[1]	GPIO[0]
G	VIO2	GPIO[43]	GPIO[44]	GPIO[45]	VSS	VSS	VDD	VSS	GPIO[9]	GPIO[7]	GPIO[6]	GPIO[2]
H	VSS	GPIO[40]	GPIO[41]	GPIO[42]	GPIO[39]	VSS	GPIO[20]	GPIO[18]	GPIO[14]	GPIO[12]	GPIO[8]	VIO1
J	VIO2	GPIO[38]	GPIO[37]	GPIO[36]	GPIO[31]	GPIO[27]	GPIO[25]	GPIO[22]	GPIO[19]	GPIO[15]	GPIO[10]	GPIO[5]
K	GPIO[35]	GPIO[34]	GPIO[33]	GPIO[32]	GPIO[28]	GPIO[26]	GPIO[16]	GPIO[21]	INT#	GPIO[24]	GPIO[11]	VSS
L	VDD	VSS	VDD	GPIO[30]	GPIO[29]	VIO1	GPIO[23]	VSS	VIO1	GPIO[17]	GPIO[13]	VSS

Note No ball is populated at location A9.

Figure 8. FX3 Hi-Speed 121-Ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	VDD	NC	NC	NC	NC	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	NC	FSLC[1]	VDD	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description					
J1	J11	VIO2	I/O	GPIO[38]	DQ[21]	GPIO	GPIO	GPIO	GPIO	GPIO
H2	H8	VIO2	I/O	GPIO[39]	DQ[22]	GPIO	GPIO	GPIO	GPIO	GPIO
H3	H11	VIO2	I/O	GPIO[40]	DQ[23]	GPIO	GPIO	GPIO	GPIO	GPIO
F4	H10	VIO2	I/O	GPIO[41]	DQ[24]	GPIO	GPIO	GPIO	GPIO	GPIO
G2	H9	VIO2	I/O	GPIO[42]	DQ[25]	GPIO	GPIO	GPIO	GPIO	GPIO
G3	G11	VIO2	I/O	GPIO[43]	DQ[26]	GPIO	GPIO	GPIO	GPIO	GPIO
F3	G10	VIO2	I/O	GPIO[44]	DQ[27]	GPIO	GPIO	GPIO	GPIO	GPIO
F2	G09	VIO2	I/O	GPIO[45]	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
F5	F11	VIO3	I/O	GPIO[46]	DQ[28]	UART_RT S	GPIO	GPIO	GPIO	GPIO
E1	F10	VIO3	I/O	GPIO[47]	DQ[29]	UART_CT S	GPIO	GPIO	GPIO	GPIO
E5	E11	VIO3	I/O	GPIO[48]	DQ[30]	UART_TX	GPIO	GPIO	GPIO	GPIO
E4	D12	VIO3	I/O	GPIO[49]	DQ[31]	UART_R X	GPIO	GPIO	GPIO	GPIO
D1	D11	VIO3	I/O	GPIO[50]	I2S_CLK	I2S_CLK	GPIO	GPIO	GPIO	GPIO
D2	E10	VIO3	I/O	GPIO[51]	I2S_SD	I2S_SD	GPIO	GPIO	GPIO	GPIO
D3	E9	VIO3	I/O	GPIO[52]	I2S_WS	I2S_WS	GPIO	GPIO	GPIO	GPIO
D4	D10	VIO4	I/O	GPIO[53]	UART_RTS	SPI_SCK	UART_RTS	SPI_SCK	GPIO	GPIO
C1	D9	VIO4	I/O	GPIO[54]	UART_CTS	SPI_SSN	UART_CTS	SPI_SSN	I2S_CLK	GPIO
C2	B12	VIO4	I/O	GPIO[55]	UART_TX	SPI_MIS O	UART_TX	SPI_MISO	I2S_SD	GPIO
D5	C12	VIO4	I/O	GPIO[56]	UART_RX	SPI_MOS I	UART_RX	SPI_MOSI	I2S_WS	GPIO
C4	E12	VIO4	I/O	GPIO[57]	I2S_MCLK	I2S_MCL K	GPIO	GPIO	I2S_MCL K	GPIO
					USB Port					
					CYUSB301X			**CYUSB201X**		
A3	A10	U3RXVD DQ	I	SSRXM	SSRX-			NC		
A4	B10	U3RXVD DQ	I	SSRXP	SSRX+			NC		
A6	A8	U3TXVD DQ	O	SSTXM	SSTX-			NC		
A5	B8	U3TXVD DQ	O	SSTXP	SSTX+			NC		
B3	B9	U3TXVD DQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND)			NC		
C9	C3	VBUS/ VBATT	I	OTG_ID	OTG_ID					
A9	A4	VBUS/V BATT	I/O	DP	D+					
A10	A2	VBUS/V BATT	I/O	DM	D–					
C8	B3	VBUS/VBAT T	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)					
					Clock and Reset					
B2	A7	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	B6	AVDD	I/O	XTALIN	XTALIN					
C7	B5	AVDD	I/O	XTALOUT	XTALOUT					
B4	F9	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	B7	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	C5	CVDDQ	I	CLKIN	CLKIN					

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
D6	C6	CVDDQ	I	CLKIN_32	CLKIN_32
C5	D8	CVDDQ	I	RESET#	RESET#
					I2C and JTAG
D9	D6	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL
D10	D2	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA
E7	F8	VIO5	I	TDI	TDI
C10	C2	VIO5	O	TDO	TDO
B11	C1	VIO5	I	TRST#	TRST#
E8	D5	VIO5	I	TMS	TMS
F6	D3	VIO5	I	TCK	TCK
D11	E8	VIO5	O	O[60]	Charger detect output
					Power
E10	E2	–	PWR	VBATT	–
B10	B1	–	PWR	VDD	–
–	A1	–	PWR	VDD	–
A1	C9	–	PWR	U3VSSQ	–
E11	E1	–	PWR	VBUS	–
D8	C4	–	PWR	VSS	–
H11	H1	–	PWR	VIO1	–
E2	K1	–	PWR	VSS	–
L9	L4	–	PWR	VIO1	–
G1	L5	–	PWR	VSS	–
–	L7	–	PWR	VIO1	–
–	L1	–	PWR	VSS	–
F1	J12	–	PWR	VIO2	–
G11	H12	–	PWR	VSS	–
	G12	–	PWR	VIO2	–
E3	C11	–	PWR	VIO3	–
L1	F12	–	PWR	VSS	–
B1	B11	–	PWR	VIO4	–
L6	A11	–	PWR	VSS	–
–	A12	–	PWR	VSS	–
B6	C7	–	PWR	CVDDQ	–
B5	C8	–	PWR	U3TXVDDQ	–
A2	C10	–	PWR	U3RXVDDQ	–
C11	D4	–	PWR	VIO5	–
L11	A3	–	PWR	VSS	–
A7	A5	–	PWR	AVDD	–
B7	A6	–	PWR	AVSS	–
C3	F4	–	PWR	VDD	–
B8	D1	–	PWR	VSS	–
E9	F5	–	PWR	VDD	–

AC Timing Parameters

GPIF II Timing

Figure 9. GPIF II Timing in Synchronous Mode

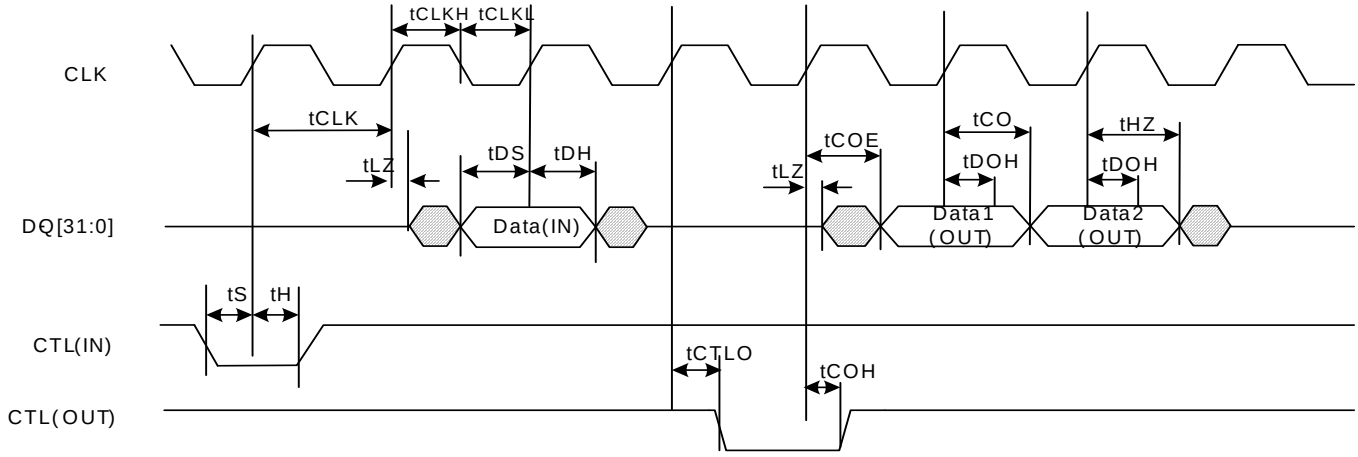


Table 9. GPIF II Timing Parameters in Synchronous Mode [2]

Parameter	Description	Min	Max	Units
Frequency	Interface clock frequency	–	100	MHz
tCLK	Interface clock period	10	–	ns
tCLKH	Clock high time	4	–	ns
tCLKL	Clock low time	4	–	ns
tS	CTL input to clock setup time	2	–	ns
tH	CTL input to clock hold time	0.5	–	ns
tDS	Data in to clock setup time	2	–	ns
tDH	Data in to clock hold time	0.5	–	ns
tCO	Clock to data out propagation delay when DQ bus is already in output direction	–	7	ns
tCOE	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus	–	9	ns
tCTLO	Clock to CTL out propagation delay	–	8	ns
tDOH	Clock to data out hold	2	–	ns
tCOH	Clock to CTL out hold	0	–	ns
tHZ	Clock to high-Z	–	8	ns
tLZ	Clock to low-Z	0	–	ns

Note
2. All parameters guaranteed by design and validated through characterization.

Figure 10. GPIF II Timing in Asynchronous Mode

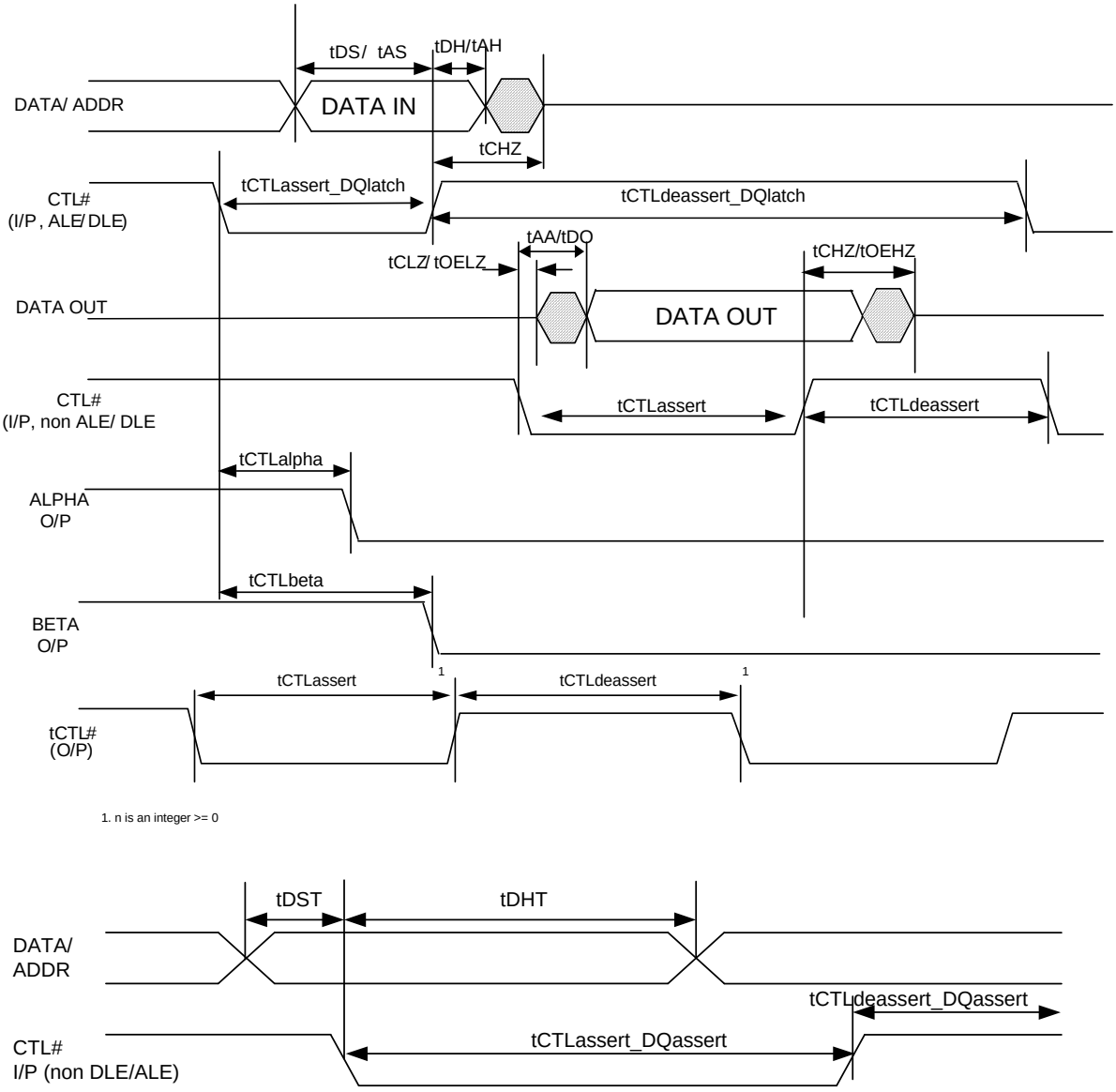


Figure 11. GPIF II Timing in Asynchronous DDR Mode

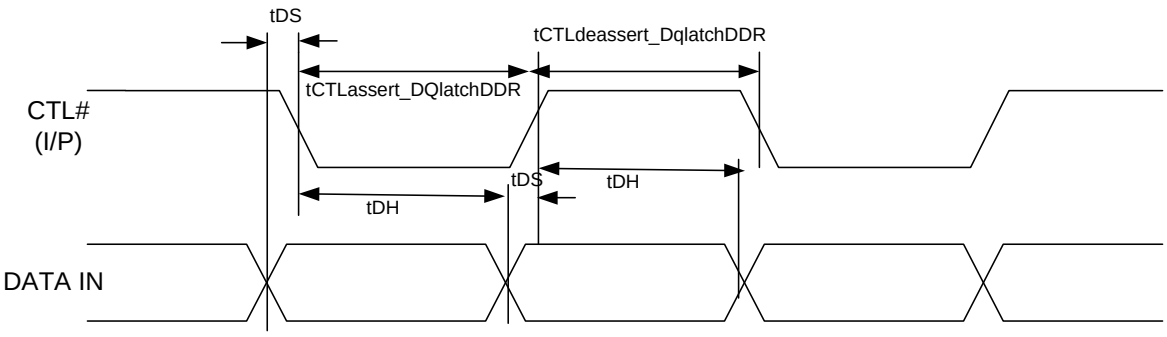


Table 10. GPIF II Timing in Asynchronous Mode[3, 4]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Notes
3. All parameters guaranteed by design and validated through characterization.
4. "alpha" output corresponds to "early output" and "beta" corresponds to "delayed output". Please refer to the GPIFII Designer Tool for the use of these outputs.

Synchronous Slave FIFO Write Sequence Description

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of t_{WFLG} from the rising edge of the clock

The same sequence of events is also applicable for burst write

Note For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a Zero-Length Packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in Figure 13.

Figure 13. Synchronous Slave FIFO Write Mode

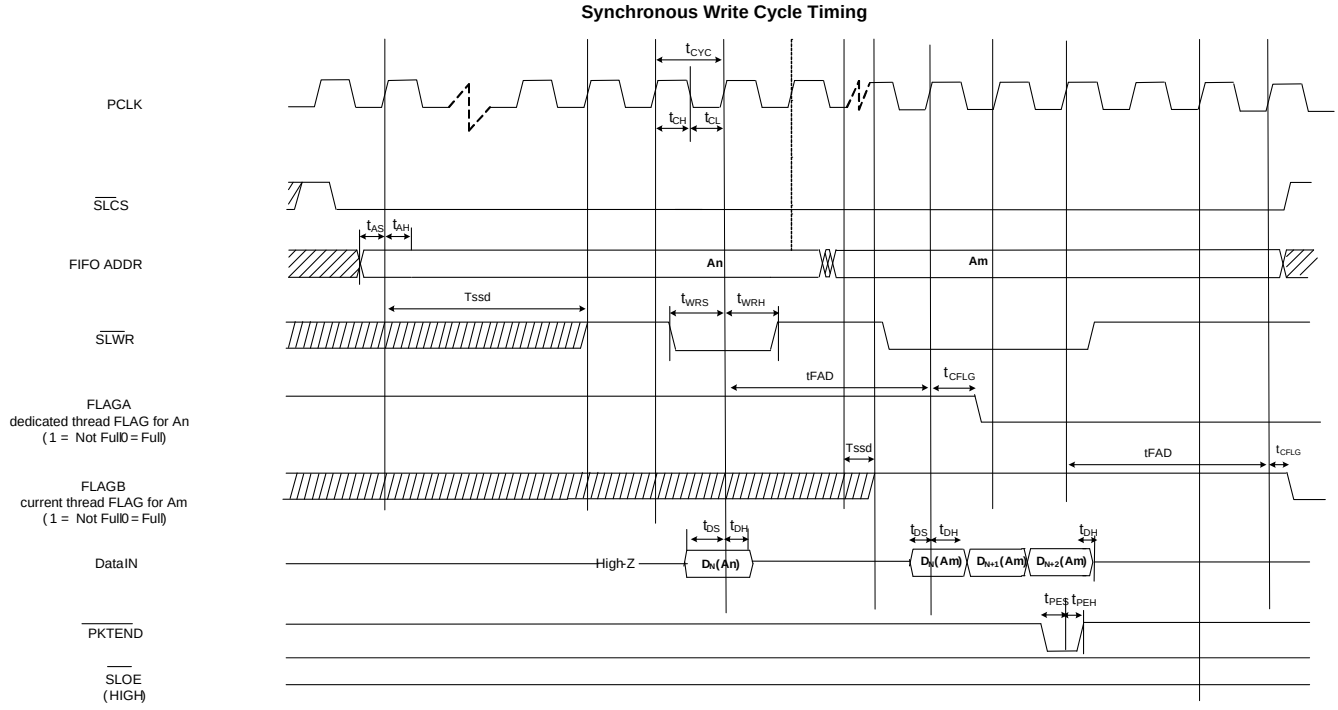


Figure 17. Asynchronous ZLP Write Cycle Timing

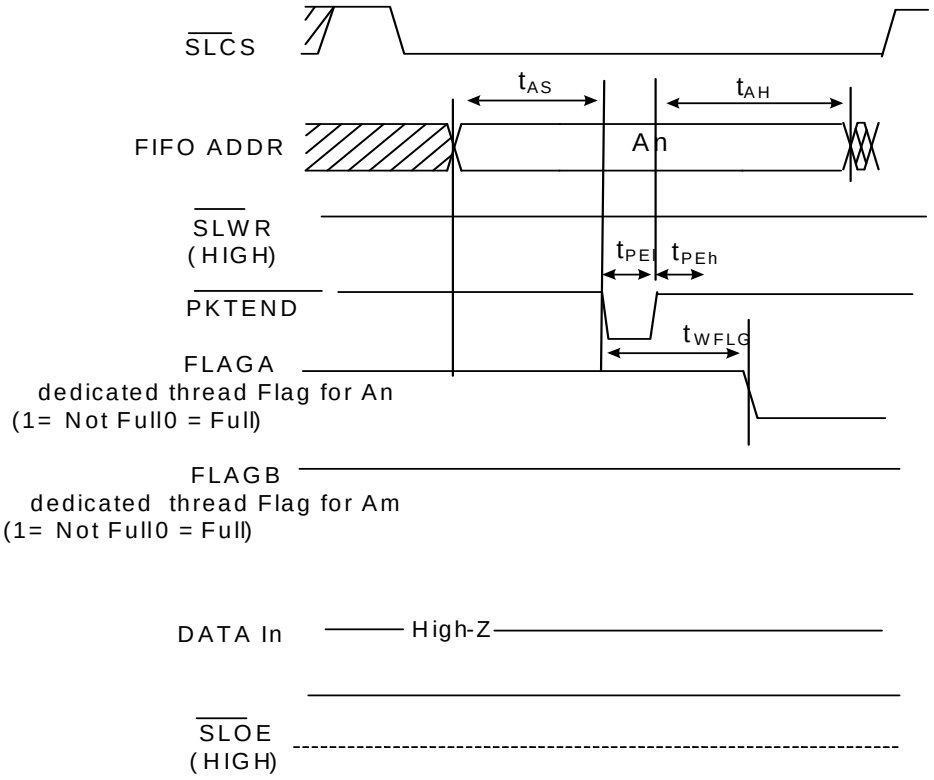


Table 12. Asynchronous Slave FIFO Parameters[6]

Parameter	Description	Min	Max	Units
tRDI	SLRD# low	20	–	ns
tRDh	SLRD# high	10	–	ns
tAS	Address to SLRD#/SLWR# setup time	7	–	ns
tAH	SLRD#/SLWR#/PKTEND to address hold time	2	–	ns
tRFLG	SLRD# to FLAGS output propagation delay	–	35	ns
tFLG	ADDR to FLAGS output propagation delay	–	22.5	ns
tRDO	SLRD# to data valid	–	25	ns
tOE	OE# low to data valid	–	25	ns
tLZ	OE# low to data low-Z	0	–	ns
tOH	SLOE# deassert data output hold	–	22.5	ns
tWRI	SLWR# low	20	–	ns
tWRh	SLWR# high	10	–	ns
tWRS	Data to SLWR# setup time	7	–	ns
tWRH	SLWR# to Data Hold time	2	–	ns
tWFLG	SLWR#/PKTEND to Flags output propagation delay	–	35	ns
tPEI	PKTEND low	20	–	ns
tPEh	PKTEND high	7.5	–	ns
tWRPE	SLWR# deassert to PKTEND deassert	2	–	ns

Note
6. All parameters guaranteed by design and validated through characterization.

Host Processor Interface (P-Port) Timing

Asynchronous SRAM Timing

Figure 18. Non-multiplexed Asynchronous SRAM Read Timing

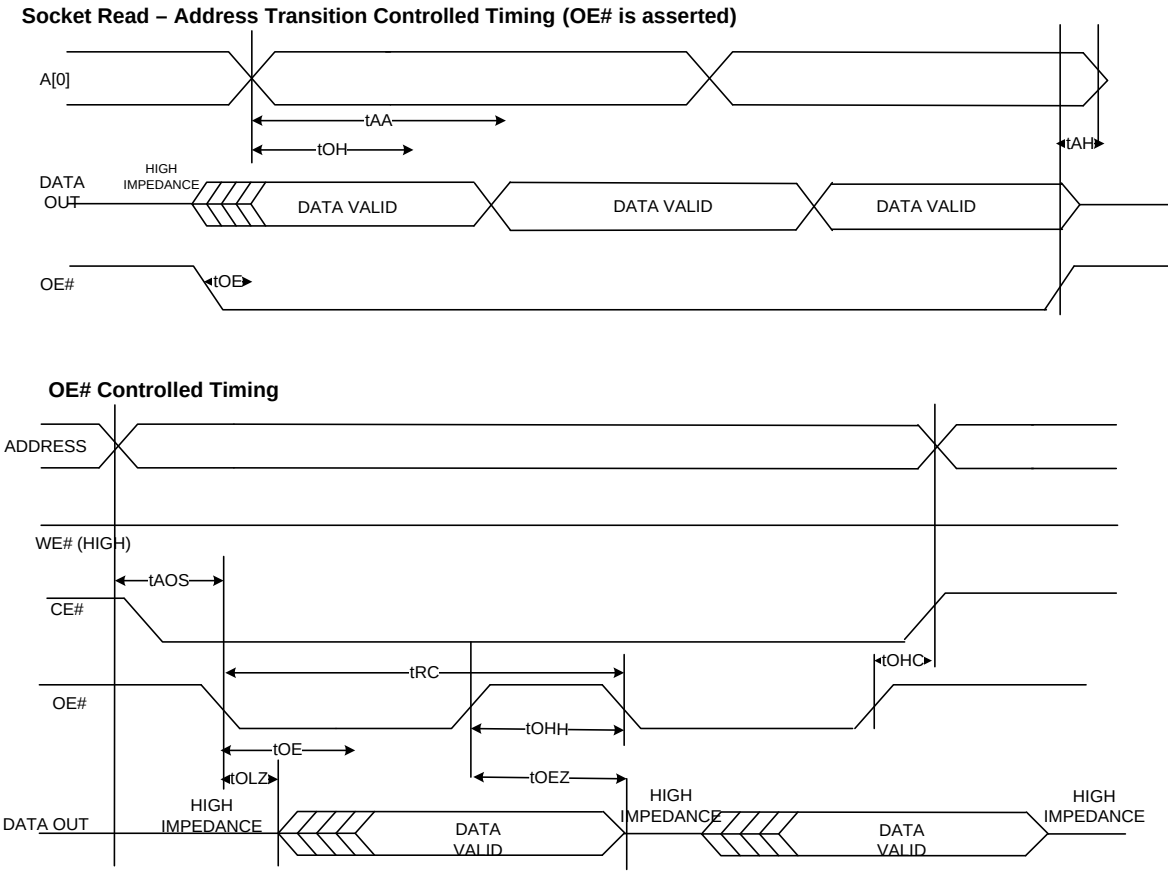


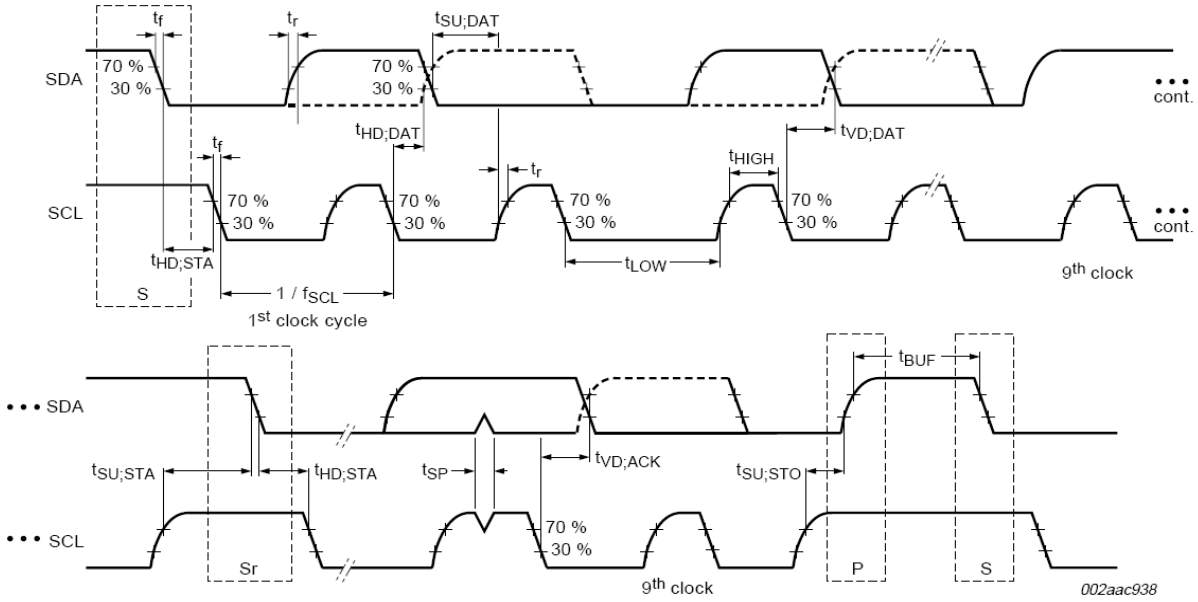
Table 15. Synchronous ADMux Timing Parameters[9]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Serial Peripherals Timing

I^2C Timing

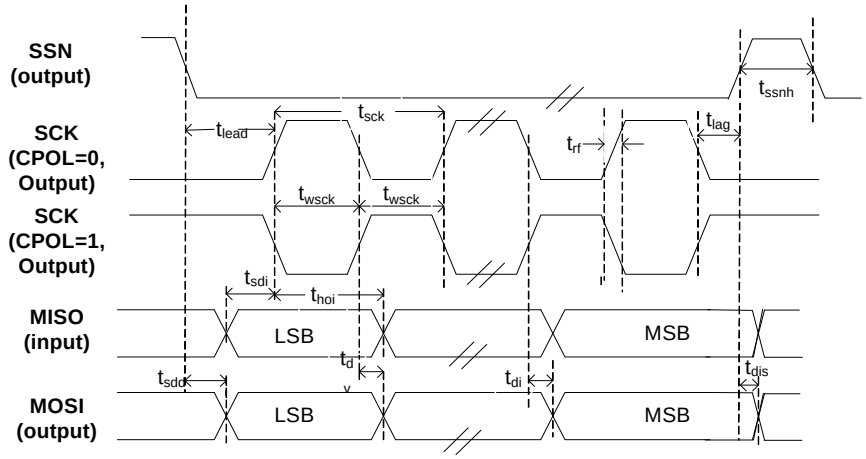
Figure 27. I^2C Timing Definition



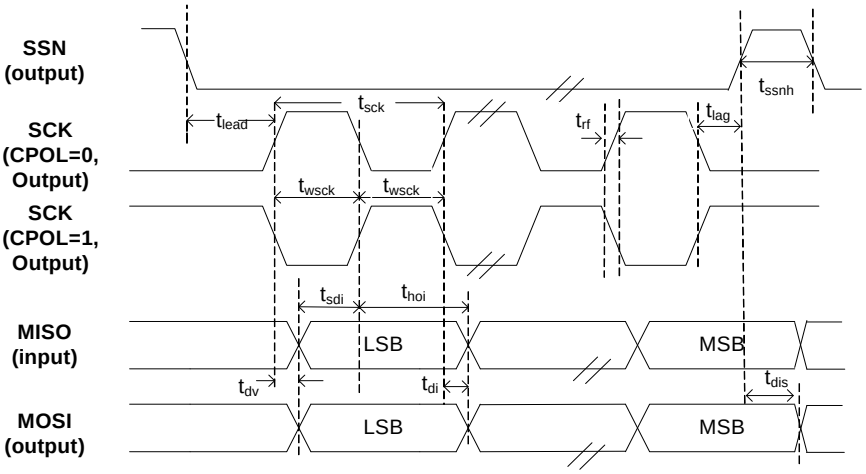
Note
9. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 29. SPI Timing

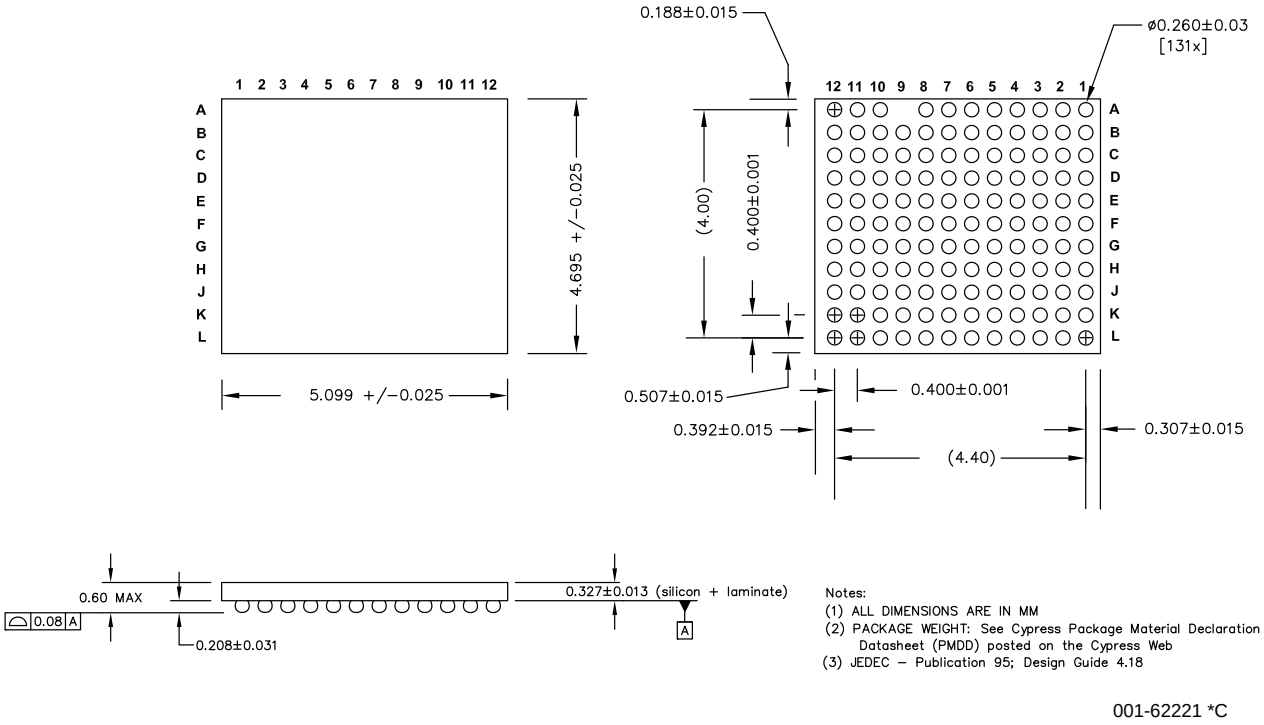


SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Figure 32. 131-ball WLCSP (5.099 × 4.695 × 0.60 mm) Package Diagram



Note Underfill is required on the board design. Contact fx3@cypress.com for details.

Acronyms

Acronym	Description
DMA	direct memory access
FIFO	first in, first out
GPIF	general programmable interface
HNP	host negotiation protocol
I^2C	inter-integrated circuit
I^2S	inter IC sound
MISO	master in, slave out
MOSI	master out, slave in
MMC	multimedia card
MSC	mass storage class
MTP	media transfer protocol
OTG	on-the-go
OVP	overvoltage protection
PHY	physical layer
PLL	phase locked loop
PMIC	power management IC
PVT	process voltage temperature
RTOS	real-time operating system
SCL	serial clock line
SCLK	serial clock
SD	secure digital
SD	secure digital
SDA	serial data clock
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
SSN	SPI slave select (Active low)
UART	universal asynchronous receiver transmitter
UVC	USB Video Class
USB	universal serial bus
WLCSP	wafer level chip scale package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Document History Page

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2669761	VSO / PYRS	03/06/2009	New data sheet
*A	2758370	VSO	09/01/2009	Updated the part# from CYX01XXBB to CYUSB3011-BZXI Changed the title from “ADVANCE” to “ADVANCE INFORMATION” In page 1, the second bullet (Flexible Host Interface), add “32-bit, 100 MHz” to first sub bullet. In page 1, changed the second bullet “Flexible Host Interface” to General Programmable Interface”. In page 1, the second bullet (Flexible Host Interface), removed "DMA Slave Support” and "MMC Slave support with Pass through Boot" sub bullets. In page 1, third bullet, changed "50 µA with Core Power" to "60 µA with Core Power" In page 1, fifth bullet, added "at 1 MHz" In page 1, seventh bullet, added "up to 4MHz" to UART In page 1, Applications Section, move “Digital Still Cameras” to second line. In page 1, Applications Section, added “Machine Vision” and Industrial Cameras” Added ™ to GPIF and FX3. In page 1, updated Logic Block Diagram. In page 2, section of “Functional Overview”, updated the whole section. In page 2, removed the section of “Product Interface” In page 2, removed the section of “Processor Interface (P-Port)” In page 2, removed the section of “USB Interface (U-Port)” In page 2, removed the section of “Other Interfaces” In page 2, added a section of "GPIF II" In page 2, added a section of "CPU" In page 2, added a section of "JTAG Interface" In page 2, added a section of "Boot Options" In page 2, added a section of "ReNumeration" In page 2, added a section of "Power" In the section of “Package”, replaced “West Bridge USB 3.0 Platform” by FX3. In the section of “Package”, added 0.8 mm pitch in front of BGA. Added Pin List (Table 1)
*B	2779196	VSO/PYRS	09/29/2009	Features: Added the thrid bullet “Fully accessible 32-bit ARM9 core with 512kB of embedded SRAM” Added the thrid line “EZ USB™ Software and DVK for easy code development” Table 1: Pin 74, corrected to NC - No Connect. Changed title to EZ-USB™ FX3: SuperSpeed USB Controller
*C	2823531	OSG	12/08/2009	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.
*D	3080927	OSG	11/08/2010	Changed status from Advance to Preliminary Changed part number from CYUSB3011 to CYUSB3014 Added the following sections: Power, Digital I/Os, Digital I/Os, System-level ESD, Electrical Specifications, AC Timing Parameters, Reset Sequence, Package Diagram Added DC Specifications table Updated feature list Updated Pin List Added support for selectable clock input frequencies. Updated block diagram Updated part number Updated package diagram

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Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	4368374	RSKV	05/02/2014	Updated Package Diagram: spec 001-62221 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*P	4474200	ANOP	08/14/2014	Added CYUSB201x MPNs, ball map, and pin list to the datasheet.
*Q	4668496	DBIR	02/24/2015	Updated Features. Updated Logic Block Diagram. Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Added More Information. Updated Functional Overview: Updated Application Examples: Updated Figure 1. Updated Figure 2. Updated USB Interface: Updated description. Removed Figure “USB Interface Signals”. Updated Pin Configurations: Updated Figure 6. Updated Reset: Updated Hard Reset: Updated description. Updated Pin Description: Updated Table 7: Updated entire table. Modified CVDDQ power domain description. Removed Table “CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width)”. Removed Table “CYUSB2014 Pin List (GPIF II with 32-bit Data Bus Width)”. Updated Electrical Specifications: Updated DC Specifications: Added ISS parameter and its details. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11. Updated AC Timing Parameters: Added Host Processor Interface (P-Port) Timing. Updated Acronyms. Added Errata. Replaced West Bridge Benicia with FX3.
*R	4703347	AMDK	03/27/2015	Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11: Updated minimum value of tSSD parameter. Added tACCD, tFAD parameters and their details.
*S	5160624	AJAI	04/07/2016	Removed ISS parameter. Added item 6 in Errata.

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Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*T	5306567	MDDD	06/29/2016	Updated AC Timing Parameters: Updated GPIF II Timing: Updated Table 9: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Write Sequence Description: Updated Table 11: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated to new template.
*U	5703914	GNKK	04/20/2017	Updated the Cypress logo and copyright information.

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