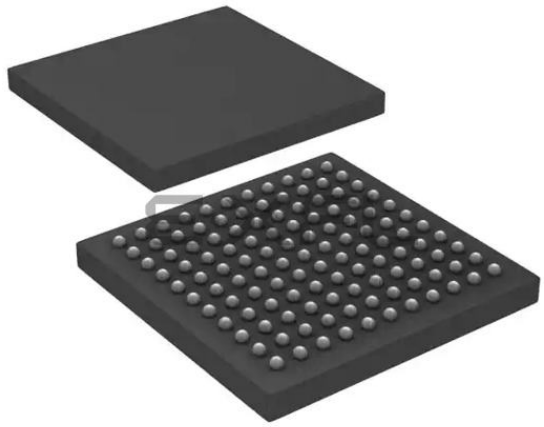

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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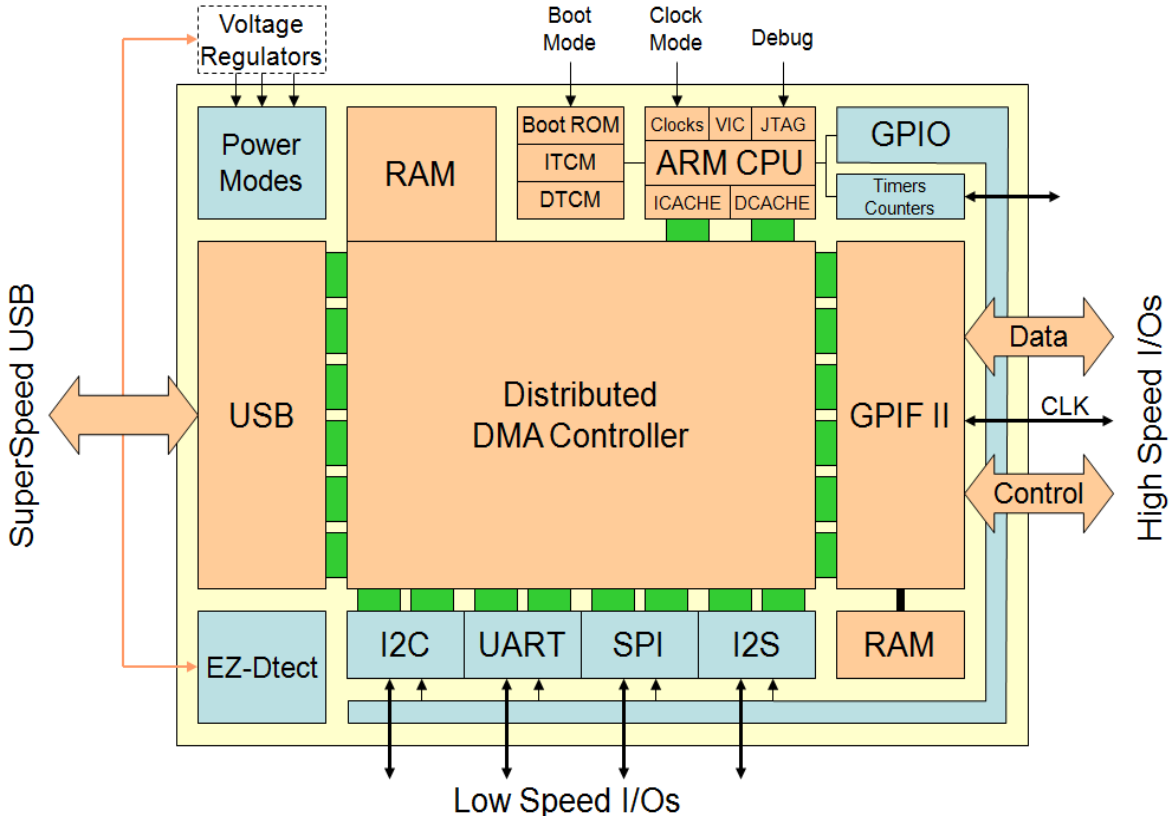
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	256K x 8
Interface	GPIF, I²C, I²S, SPI, UART, USB
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3012-bzxc

Logic Block Diagram



Functional Overview

Cypress's EZ-USB FX3 is a SuperSpeed peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.1 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see Ordering Information on page 45) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I^2S.

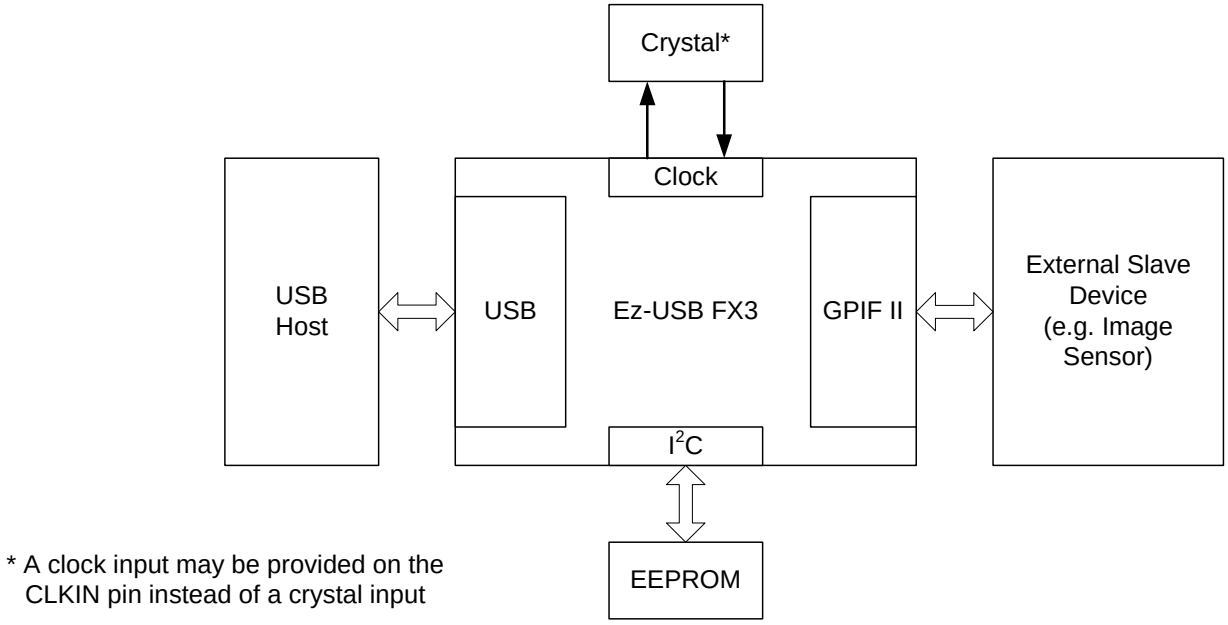
FX3 comes with application development tools. The software development kit comes with firmware and host application examples for accelerating time to market.

FX3 complies with the USB 3.1, Gen 1.0 specification and is also backward compatible with USB 2.0. It also complies with the Battery Charging Specification v1.1 and USB 2.0 OTG Specification v2.0.

Application Examples

In a typical application (see Figure 1), the FX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection. Additionally, FX3 can function as a coprocessor connecting via the GPIF II interface to an application processor (see Figure 2) and operates as a subsystem providing SuperSpeed USB connectivity to the application processor.

Figure 1. EZ-USB FX3 as Main Processor



ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

EZ-Dtect

FX3 supports USB Charger and accessory detection (EZ-Dtect). The charger detection mechanism complies with the Battery Charging Specification Revision 1.1. In addition to supporting this version of the specification, FX3 also provides hardware support to detect the resistance values on the ID pin.

FX3 can detect the following resistance ranges:

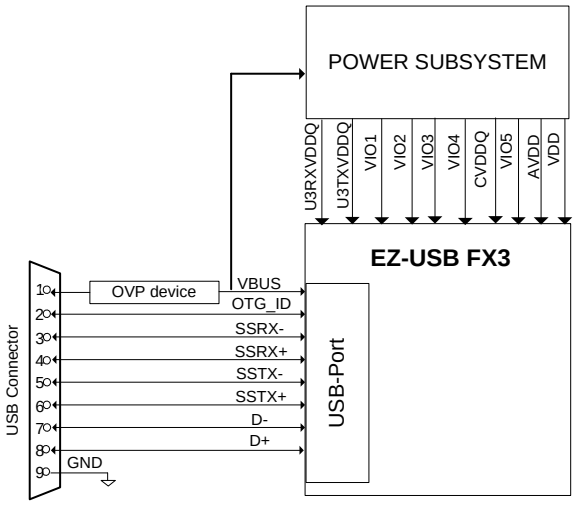
- Less than 10 Ω
- Less than 1 kΩ
- 65 kΩ to 72 kΩ
- 35 kΩ to 39 kΩ
- 99.96 kΩ to 104.4 kΩ (102 kΩ ± 2%)
- 119 kΩ to 132 kΩ
- Higher than 220 kΩ
- 431.2 kΩ to 448.8 kΩ (440 kΩ ± 2%)

FX3's charger detects a dedicated wall charger, Host/Hub charger, and Host/Hub.

VBUS Overvoltage Protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. Figure 3 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 8 for the operating range of VBUS and VBATT.

Figure 3. System Diagram with OVP Device For VBUS



Carkit UART Mode

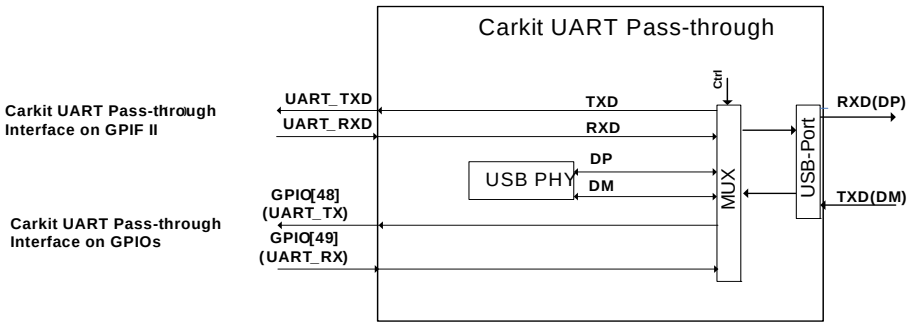
The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in Figure on page 8.

In this mode, FX3 supports a rate of up to 9600 bps.

Figure 4. Carkit UART Pass-through Block Diagram



UART Interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

I²C Interface

FX3's I²C interface is compatible with the I²C Bus Specification Revision 3. This I²C interface is capable of operating only as I²C master; therefore, it may be used to communicate with other I²C slave devices. For example, FX3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

FX3's I²C Master Controller also supports multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports clock-stretching to enable slower devices to exercise flow control.

The I²C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

I²S Interface

FX3 has an I²S port to support external audio codec devices. FX3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I²S interface are 32 kHz, 44.1 kHz, and 48 kHz.

Boot Options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I²C
- Boot from SPI (SPI devices supported are M25P32 (32 Mbit), M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode

Table 2. FX3 Booting Options

PMODE[2:0][1]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I²C, On Failure, USB Boot is Enabled
1FF	I²C only
0F1	SPI, On Failure, USB Boot is Enabled

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in Figure 30 on page 42 and Table 19 on page 42. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB® FX3™ Boot Options for more details.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Note
1. F indicates Floating.

Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 3.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in Table 4 on page 10.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4. FX3 Input Clock Specifications

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	
	10-kHz offset	–	–120	
	100-kHz offset	–	–128	
	1-MHz offset	–	–130	
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	
Undershoot	–	–	–3	
Rise time/fall time	–	–	3	ns

32-kHz Watchdog Timer Clock Input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer. Requirements for the optional 32-kHz clock input are listed in Table 5.

Table 5. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Disabled (L2)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode ■ External Processor, through the use of mailbox registers can put FX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#
Standby Mode (L3)	■ The power consumption in this mode does not exceed ISB3 ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting FX3 into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	■ Detection of VBUS ■ Level detect on UART_CTS (Programmable Polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Ambient temperature with power supplied (Commercial) ..... 0 °C to +70 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} .....1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} .....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ .....1.25 V

DC input voltage to any input pin ..... V_{CC} + 0.3 V

DC voltage applied to outputs in high Z state ..... V_{CC} + 0.3 V

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current .....> 200 mA

Maximum output short-circuit current for all I/Os (cumulative).....–100 mA

Maximum output current per I/O (source or sink)..... .....20 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

Commercial ..... 0 °C to +70 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage .....1.15 V to 1.25 V

V_{BATT} supply voltage .....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage .....1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

DC Specifications

Table 8. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC – 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.

Figure 10. GPIF II Timing in Asynchronous Mode

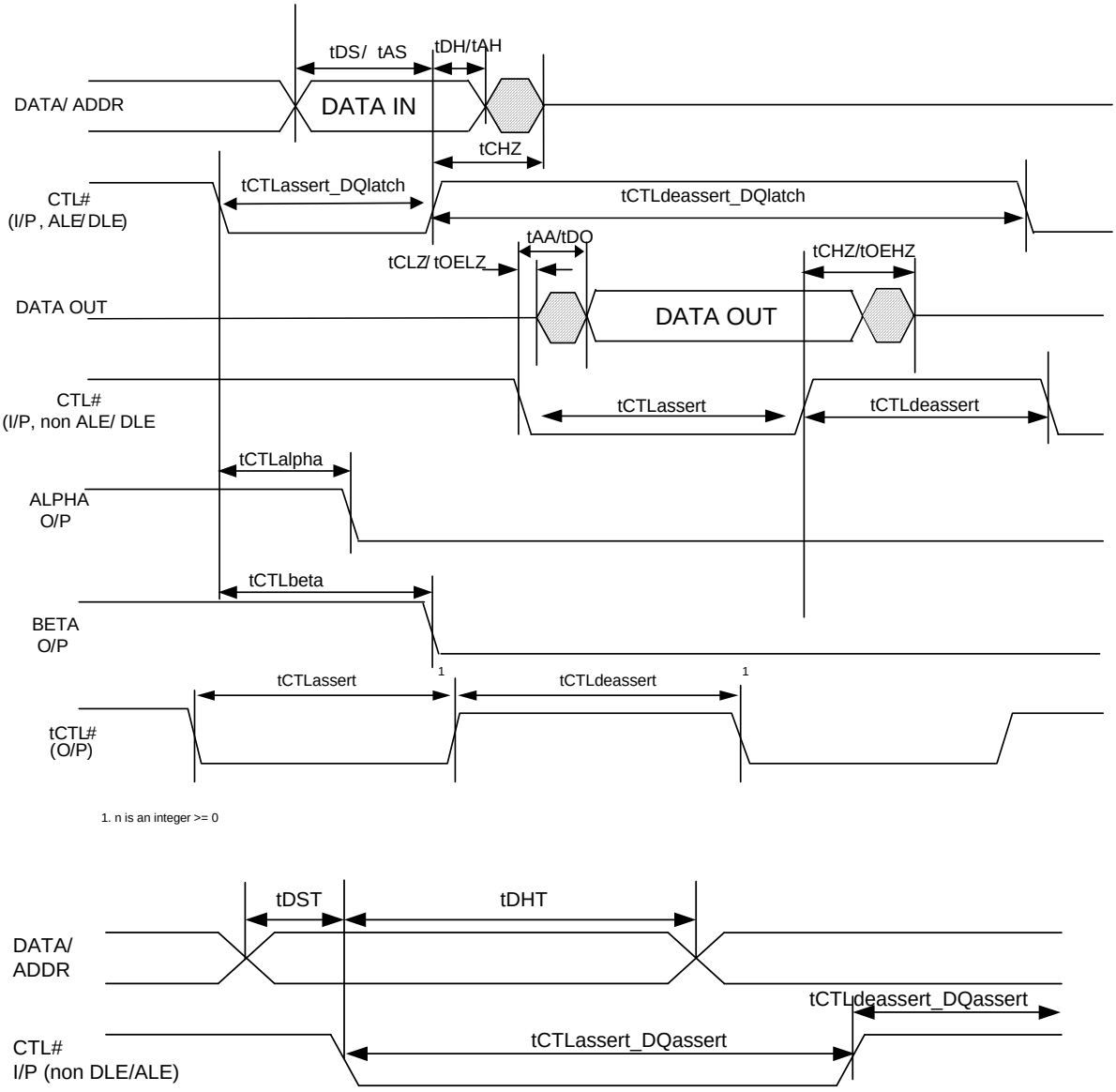


Figure 11. GPIF II Timing in Asynchronous DDR Mode

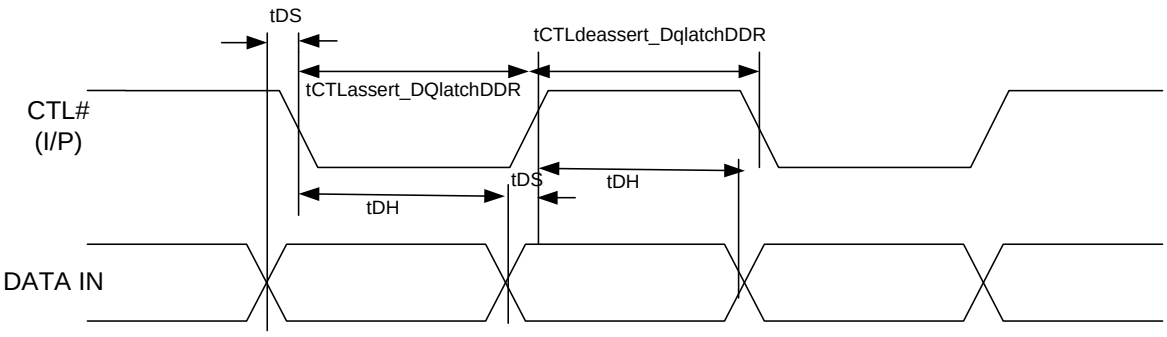


Table 10. GPIF II Timing in Asynchronous Mode[3, 4]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Notes
3. All parameters guaranteed by design and validated through characterization.
4. "alpha" output corresponds to "early output" and "beta" corresponds to "delayed output". Please refer to the GPIFII Designer Tool for the use of these outputs.

Asynchronous Slave FIFO Read Sequence Description

- FIFO address is stable and the SLCS# signal is asserted.
- SLOE# is asserted. This results in driving the data bus.
- SLRD # is asserted.
- Data from the FIFO is driven after assertion of SLRD#. This data is valid after a propagation delay of tRDO from the falling edge of SLRD#.
- FIFO pointer is incremented on deassertion of SLRD#

In Figure 15, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle, SLOE# must be in an asserted state. SLRD# and SLOE# can also be tied.

The same sequence of events is also shown for a burst read.

Note In the burst read mode, during SLOE# assertion, the data bus is in a driven state (data is driven from a previously addressed FIFO). After assertion of SLRD# data from the FIFO is driven on the data bus (SLOE# must also be asserted). The FIFO pointer is incremented after deassertion of SLRD#.

Figure 15. Asynchronous Slave FIFO Read Mode

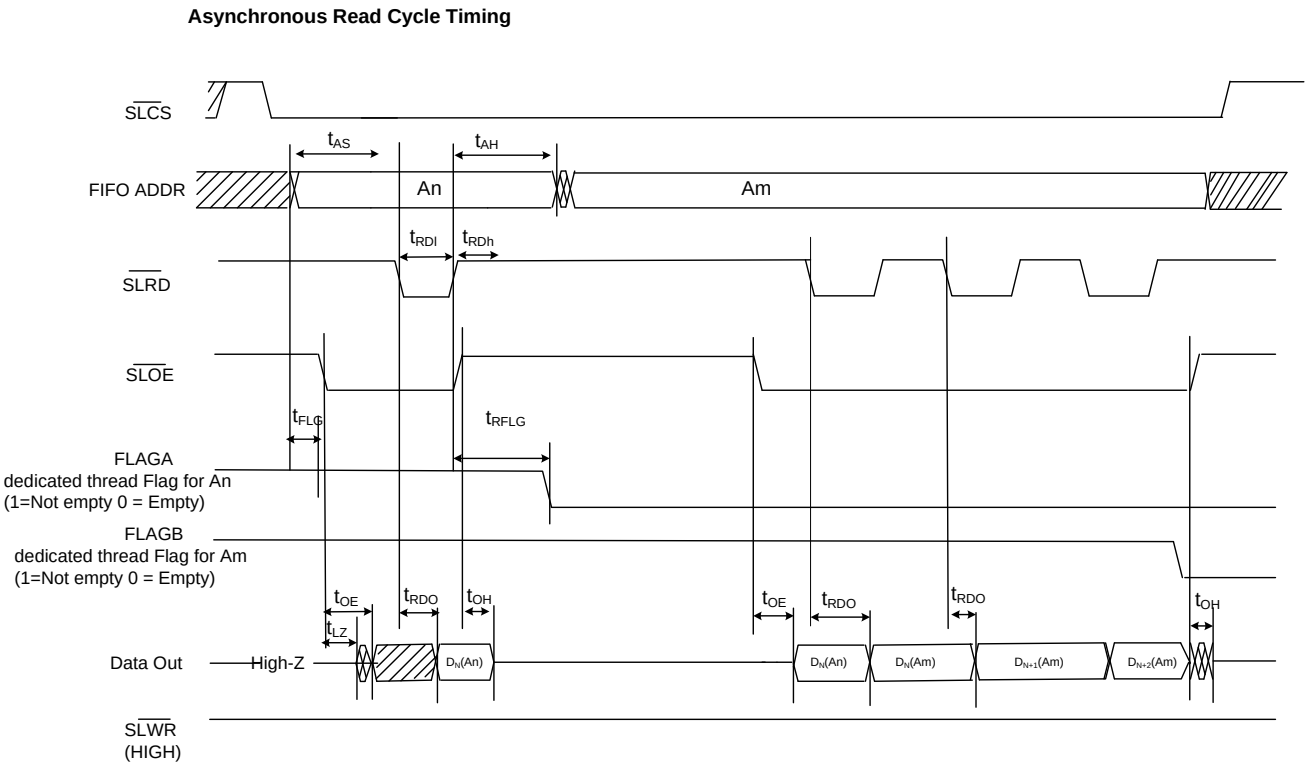
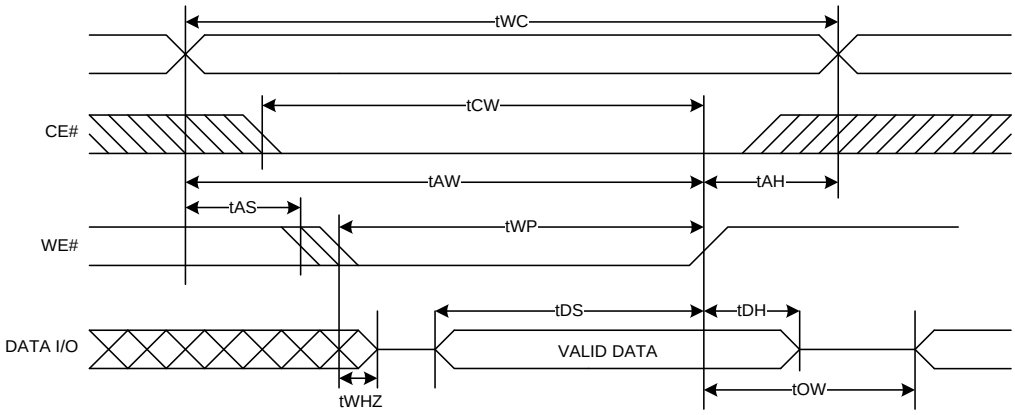


Figure 20. Non-multiplexed Asynchronous SRAM Write Timing (WE# controlled, OE# LOW)

Write Cycle 3 WE# Controlled. OE# Low



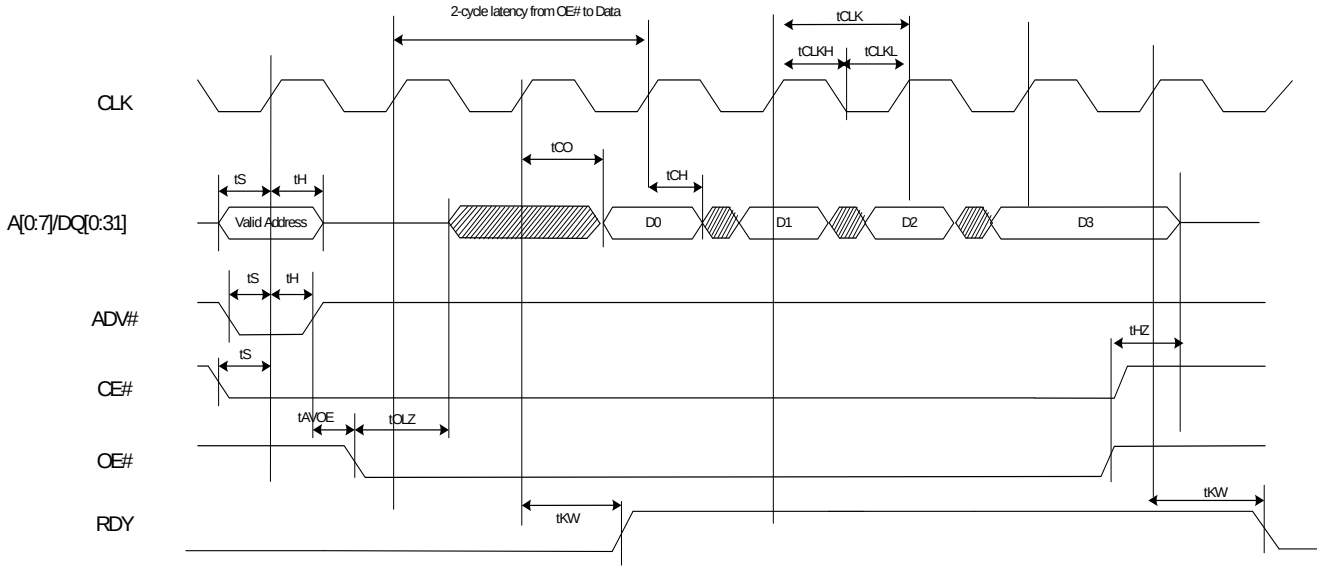
Note: tWP must be adjusted such that tWP > tWHZ + tDS

Table 13. Asynchronous SRAM Timing Parameters[7]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	Mbps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to LOW-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ HIGH-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ HIGH-Z output	–	22.5	ns
tOW	End of write to LOW-Z output	0	–	ns

Note
7. All parameters guaranteed by design and validated through characterization.

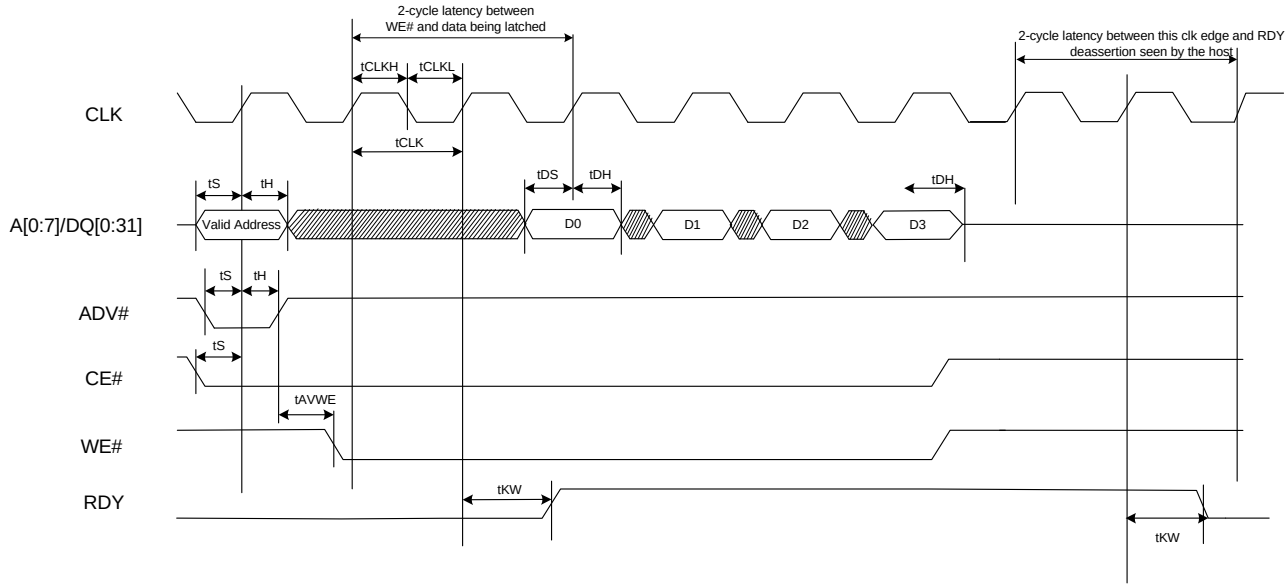
Figure 25. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 26. Sync ADMux Interface – Burst Write Timing

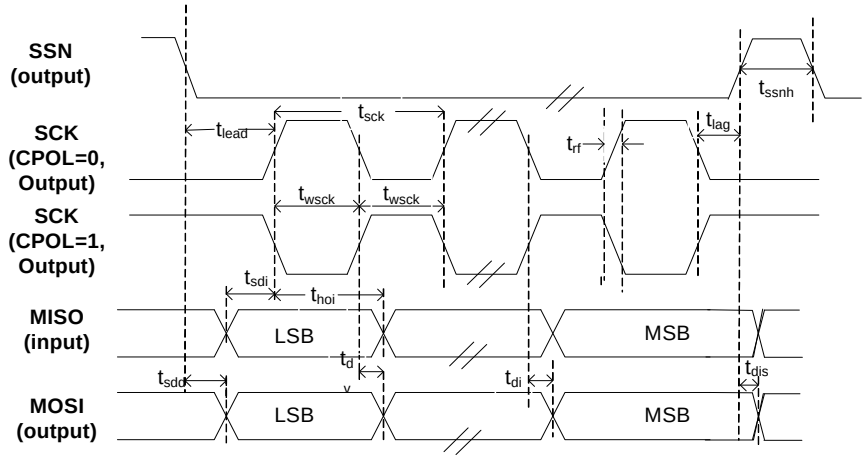


Note:

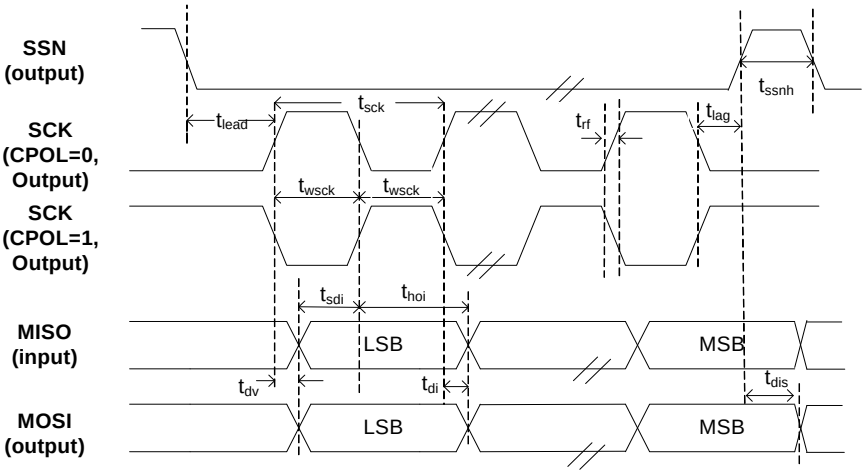
1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

SPI Timing Specification

Figure 29. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 18. SPI Timing Parameters[12]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[13]-5	1.5 tsck[13]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[13]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
12. All parameters guaranteed by design and validated through characterization.
13. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Reset Sequence

FX3's hard reset sequence requirements are specified in this section.

Table 19. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#	–	5	–
tRR	Reset recovery time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter standby/suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

Figure 30. Reset Sequence

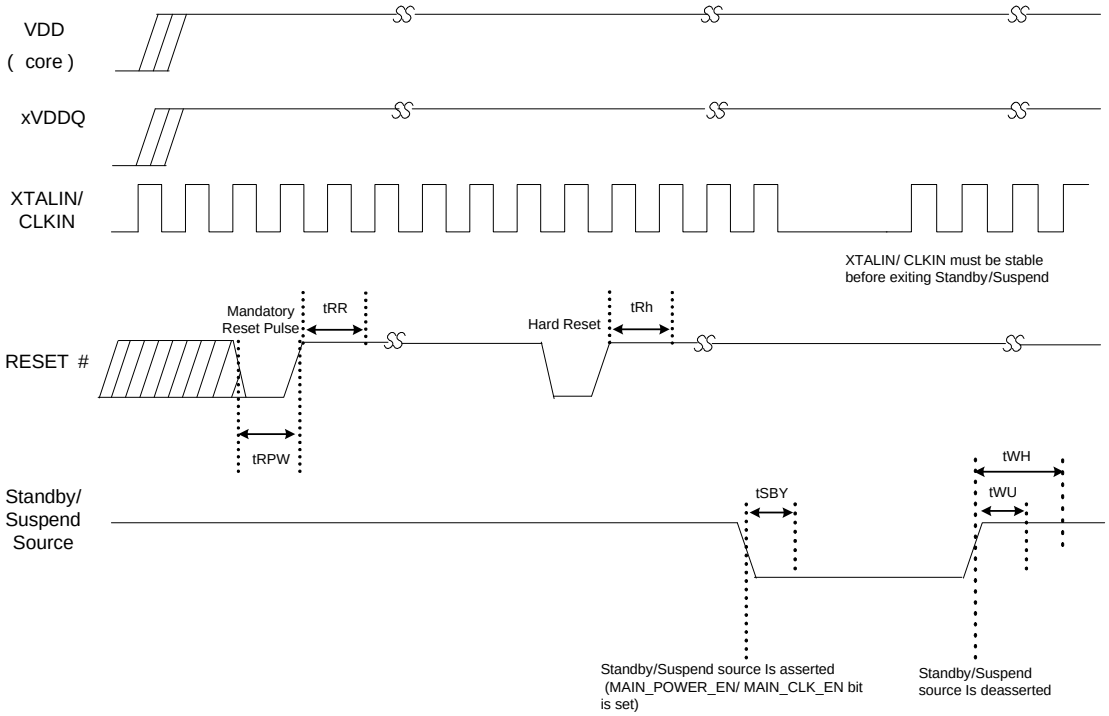
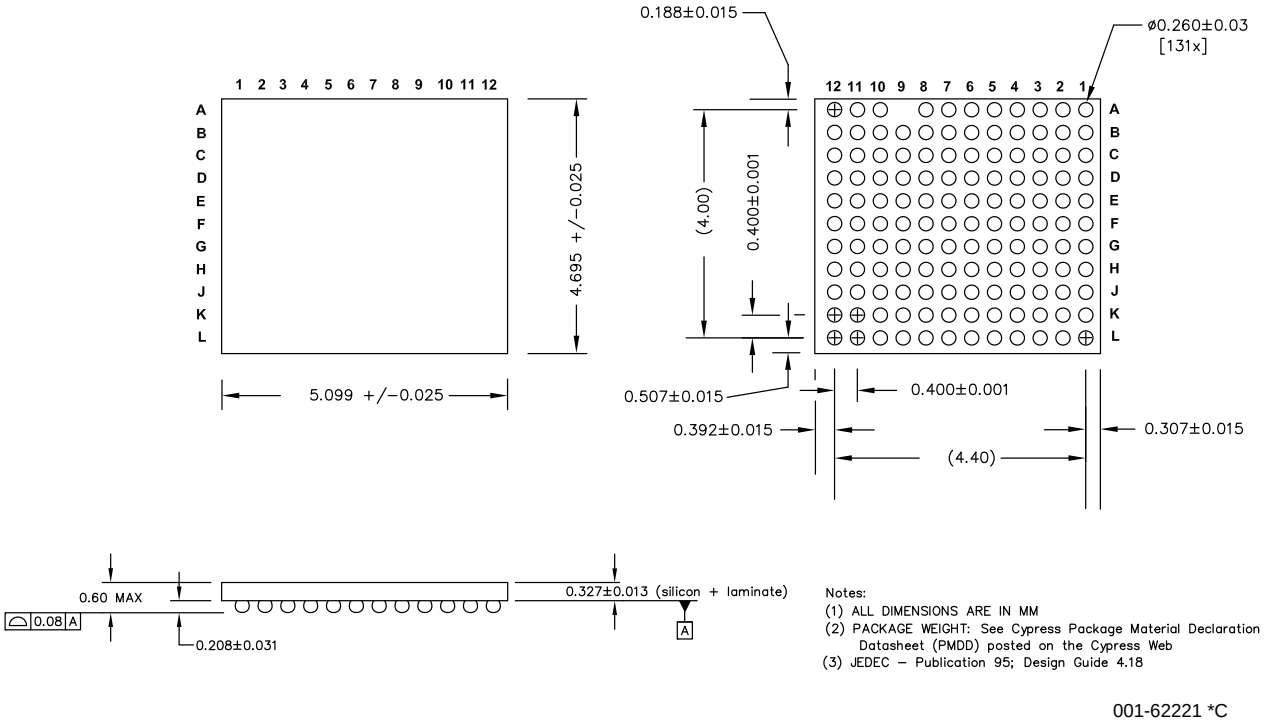


Figure 32. 131-ball WLCSP (5.099 × 4.695 × 0.60 mm) Package Diagram



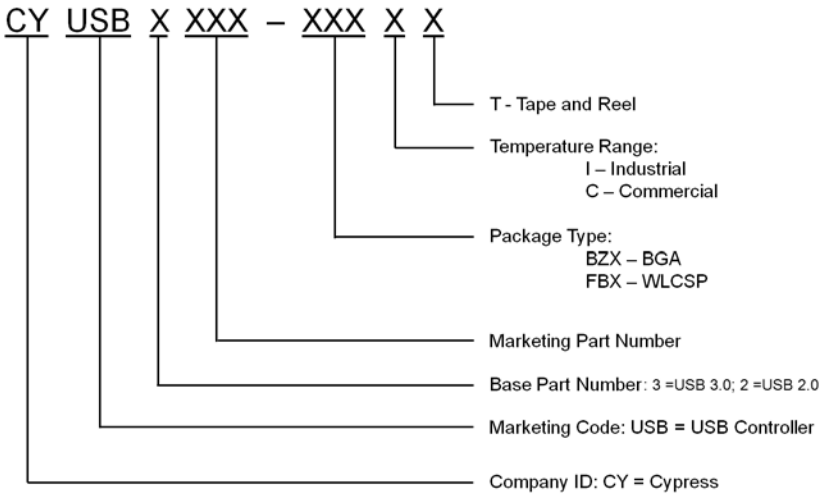
Note Underfill is required on the board design. Contact fx3@cypress.com for details.

Ordering Information

Table 20. Ordering Information

Ordering Code	USB	SRAM (kB)	GPIF II Data Bus Width	Operating Temperature	Package Type
CYUSB3011-BZXC	USB 3.0	256	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3012-BZXC	USB 3.0	256	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3013-BZXC	USB 3.0	512	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXC	USB 3.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXI	USB 3.0	512	32-bit	–40°C to +85°C	121-ball BGA
CYUSB3014-FBXCT	USB 3.0	512	32-bit	0 °C to +70 °C	131-ball WLCSP
CYUSB3014-FBXIT	USB 3.0	512	32-bit	–40 °C to +85 °C	131-ball WLCSP
CYUSB2014-BZXC	USB 2.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB2014-BZXI	USB 2.0	512	32-bit	–40 °C to +85 °C	121-ball BGA

Ordering Code Definitions



■**Trigger Conditions**
This condition is triggered when FX3 is self-powered in USB boot mode.

■**Scope Of Impact**
Device does not enumerate

■**Workaround**
Reset the device after connecting to USB host.

■**Fix Status**
No fix. Workaround is required.

3. **Extra ZLP is generated by the COMMIT action in the GPIF II state.**

■**Problem Definition**
When COMMIT action is used in a GPIF-II state without IN_DATA action then an extra Zero Length Packet (ZLP) is committed along with the data packets.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when COMMIT action is used in a state without IN_DATA action.

■**Scope Of Impact**
Extra ZLP is generated.

■**Workaround**
Use IN_DATA action along with COMMIT action in the same state.

■**Fix Status**
No fix. Workaround is required.

4. **Invalid PID Sequence in USB 2.0 ISOC data transfer.**

■**Problem Definition**
When the FX3 device is functioning as a high speed USB device with high bandwidth isochronous endpoints, the PID sequence of the ISO data packets is governed solely by the isomult setting. The length of the data packet is not considered while generating the PID sequence during each microframe. For example, even if a short packet is being sent on an endpoint with MULT set to 2; the PID used will be DATA2

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered when high bandwidth ISOC transfer endpoints are used.

■**Scope Of Impact**
ISOC data transfers failure.

■**Workaround**
This problem can be worked around by reconfiguring the endpoint with a lower isomult setting prior to sending short packets, and then switching back to the original value.

■**Fix Status**
No fix. Workaround is required.

5. **USB data transfer errors are seen when ZLP is followed by data packet within same microframe.**

■**Problem Definition**
Some data transfer errors may be seen if a Zero Length Packet is followed very quickly (within one microframe or 125 us) by another data packet on a burst enabled USB IN endpoint operating at super speed.

■**Parameters Affected**
N/A

■**Trigger Conditions**
This condition is triggered in SuperSpeed transfer with ZLPs

■**Scope Of Impact**
Data failure and lower data speed.

■**Workaround**
The solution is to ensure that some time is allowed to elapse between a ZLP and the next data packet on burst enabled USB IN endpoints. If this cannot be ensured at the data source, the CyU3PDmaChannelSetSuspend() API can be used to suspend the

Document History Page

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2669761	VSO / PYRS	03/06/2009	New data sheet
*A	2758370	VSO	09/01/2009	Updated the part# from CYX01XXBB to CYUSB3011-BZXI Changed the title from “ADVANCE” to “ADVANCE INFORMATION” In page 1, the second bullet (Flexible Host Interface), add “32-bit, 100 MHz” to first sub bullet. In page 1, changed the second bullet “Flexible Host Interface” to General Programmable Interface”. In page 1, the second bullet (Flexible Host Interface), removed "DMA Slave Support” and "MMC Slave support with Pass through Boot" sub bullets. In page 1, third bullet, changed "50 µA with Core Power" to "60 µA with Core Power" In page 1, fifth bullet, added "at 1 MHz" In page 1, seventh bullet, added "up to 4MHz" to UART In page 1, Applications Section, move “Digital Still Cameras” to second line. In page 1, Applications Section, added “Machine Vision” and Industrial Cameras” Added ™ to GPIF and FX3. In page 1, updated Logic Block Diagram. In page 2, section of “Functional Overview”, updated the whole section. In page 2, removed the section of “Product Interface” In page 2, removed the section of “Processor Interface (P-Port)” In page 2, removed the section of “USB Interface (U-Port)” In page 2, removed the section of “Other Interfaces” In page 2, added a section of "GPIF II" In page 2, added a section of "CPU" In page 2, added a section of "JTAG Interface" In page 2, added a section of "Boot Options" In page 2, added a section of "ReNumeration" In page 2, added a section of "Power" In the section of “Package”, replaced “West Bridge USB 3.0 Platform” by FX3. In the section of “Package”, added 0.8 mm pitch in front of BGA. Added Pin List (Table 1)
*B	2779196	VSO/PYRS	09/29/2009	Features: Added the thrid bullet “Fully accessible 32-bit ARM9 core with 512kB of embedded SRAM” Added the thrid line “EZ USB™ Software and DVK for easy code development” Table 1: Pin 74, corrected to NC - No Connect. Changed title to EZ-USB™ FX3: SuperSpeed USB Controller
*C	2823531	OSG	12/08/2009	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.
*D	3080927	OSG	11/08/2010	Changed status from Advance to Preliminary Changed part number from CYUSB3011 to CYUSB3014 Added the following sections: Power, Digital I/Os, Digital I/Os, System-level ESD, Electrical Specifications, AC Timing Parameters, Reset Sequence, Package Diagram Added DC Specifications table Updated feature list Updated Pin List Added support for selectable clock input frequencies. Updated block diagram Updated part number Updated package diagram

Document History Page (continued)

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	3204393	OSG	03/24/2011	Updated Slave FIFO protocol and added ZLP signaling protocol Changed GPIFII asynchronous tDO parameter Changed Async Slave FIFO tOE parameter Changed Async Slave FIFO tRDO parameter Added tCOE parameter to GPIFII Sync mode timing parameters Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0 Modified description of GPIFII Sync tCO (previously tDO) parameter Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge. Correspondingly, changed the tAH number. Removed 24 bit data bus support for GPIFII.
*F	3219493	OSG	04/07/2011	Minor ECN - Release to web. No content changes.
*G	3235250	GSZ	04/20/2011	Minor updates in Features.
*H	3217917	OSG	04/06/2011	Updated GPIFII Synchronous Timing diagram. Added SPI Boot option. Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams. Corrected Synchronous Slave FIFO tDH parameter.
*I	3305568	DSG	07/07/2011	Minor ECN - Correct ECN number in revision *F. No content changes.
*J	3369042	OSG	12/06/2011	Changed datasheet status from Preliminary to Final. Changed tWRPE parameter to 2ns Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated Sync SLave FIFO Read timing diagram Updated SPI timing diagram Removed tGRANULARITY parameter Updated I2S Timing diagram and tTd parameter Updated 121-ball BGA package diagram. Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated tPEI parameter in Async Slave FIFO timing table Updated Sync Slave FIFO write and read timing diagrams Updated I2C interface tVD:ACK parameter for 1MHz operation Clarified that CTL[15] is not usable as a GPIO
*K	3534275	OSG	02/24/2012	Corrected typo in the block diagram.
*L	3649782	OSG	08/16/2012	Changed part number to CYUSB301X. Added 256 KB range for embedded SRAM. Updated Functional Overview, Other Interfaces, and Clocking sections. Added Pin List for CYUSB3011 and CYUSB3013 parts. Updated Ordering Information with new part numbers.
*M	3848148	OSG	12/20/2012	Updated 121-ball BGA package diagram to current revision.
*N	4016006	OSG	05/31/2013	Updated Features (Added 131-ball WLCSP under Package option). Updated Pin Configurations (Added FX3 131-ball WLCSP Ball Map (Figure 7)). Updated Pin Description (Updated Table 7). Updated Electrical Specifications (Included Commercial Temperature Range related information). Updated Operating Conditions (Included Commercial Temperature Range related information). Updated Package Diagram (Added 131-ball WLCSP Package Diagram (Figure 32)). Updated Ordering Information (Updated part numbers).