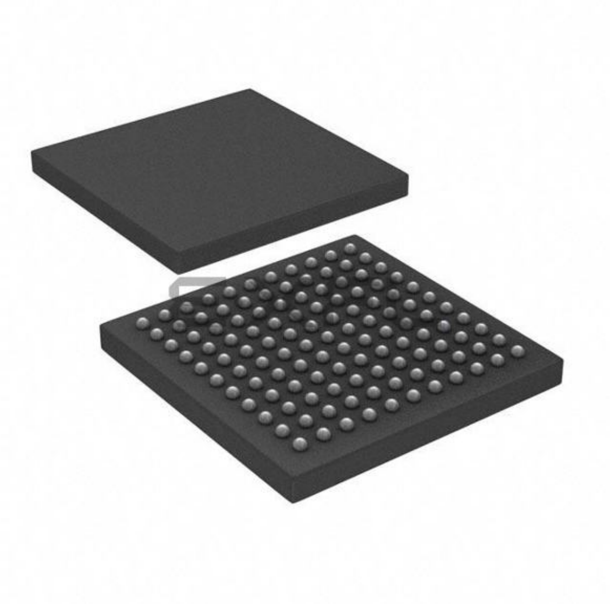

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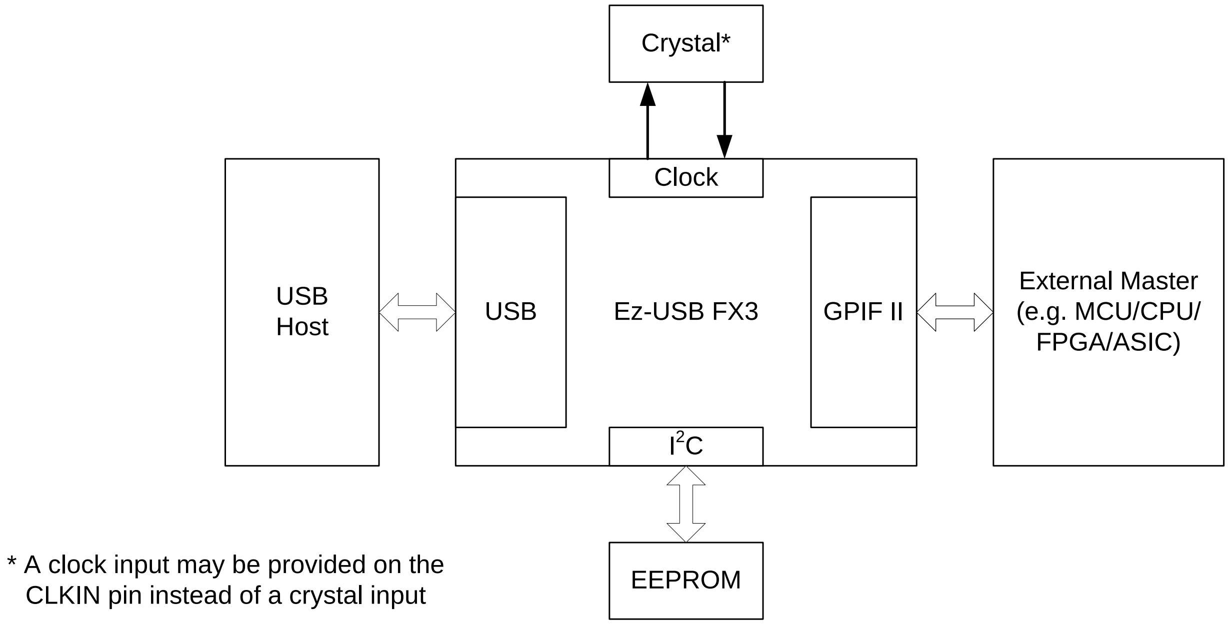
What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	GPIF, I²C, I²S, SPI, UART, USB
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3014-bzxit

Figure 2. EZ-USB FX3 as a Coprocessor



USB Interface

FX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.1 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- FX3 Hi-Speed parts (CYUSB201X) only support USB 2.0.
- Complies with OTG Supplement Revision 2.0. It supports High-Speed, Full-Speed, and Low-Speed OTG dual-role device capability. As a peripheral, FX3 is capable of SuperSpeed, High-Speed, and Full-Speed. As a host, it is capable of High-Speed, Full-Speed, and Low-Speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, application examples show that the FX3 supports UAS, USB Video Class (UVC), and Mass Storage Class (MSC) USB peripheral classes. All other device classes can be supported by customer firmware; a template example is provided as a starting point.
- As an OTG host, application examples show that FX3 supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

OTG

FX3 is compliant with the OTG Specification Revision 2.0. In OTG mode, FX3 supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3 requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3 does not support Attach Detection Protocol (ADP).

OTG Connectivity

In OTG mode, FX3 can be configured to be an A, B, or dual-role device. It can connect to the following:

- ACA device
- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

UART Interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

I^2C Interface

FX3's I^2C interface is compatible with the I^2C Bus Specification Revision 3. This I^2C interface is capable of operating only as I^2C master; therefore, it may be used to communicate with other I^2C slave devices. For example, FX3 may boot from an EEPROM connected to the I^2C interface, as a selectable boot option.

FX3's I^2C Master Controller also supports multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I^2C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I^2C controller supports clock-stretching to enable slower devices to exercise flow control.

The I^2C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

I^2S Interface

FX3 has an I^2S port to support external audio codec devices. FX3 functions as I^2S Master as transmitter only. The I^2S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I^2S interface are 32 kHz, 44.1 kHz, and 48 kHz.

Boot Options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I^2C
- Boot from SPI (SPI devices supported are M25P32 (32 Mbit), M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode

Table 2. FX3 Booting Options

PMODE[2:0][1]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I^2C, On Failure, USB Boot is Enabled
1FF	I^2C only
0F1	SPI, On Failure, USB Boot is Enabled

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in Figure 30 on page 42 and Table 19 on page 42. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB® FX3™ Boot Options for more details.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Note

1. F indicates Floating.

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See Pin Configurations for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Pin Configurations

Figure 6. FX3 121-ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 7. FX3 131-Ball WLCSP Ball Map (Bottom View)

	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	SSRXM		SSTXM	FSLC[0]	AVSS	AVDD	DP	VSS	DM	VDD
B	GPIO[55]	VIO4	SSRXP	R_USB3	SSTXP	FSLC[2]	XTALIN	XTALOUT	NC	R_USB2	NC	VDD
C	GPIO[56]	VIO3	U3RXVDDQ	U3VSSQ	U3TXVDDQ	CVDDQ	CLKIN_32	CLKIN	VSS	OTG_ID	TDO	TRST#
D	GPIO[49]	GPIO[50]	GPIO[53]	GPIO[54]	RESET#	VDD	I2C_GPIO[58]	TMS	VIO5	TCK	I2C_GPIO[59]	VSS
E	GPIO[57]	GPIO[48]	GPIO[51]	GPIO[52]	O[60]	VSS	VSS	VSS	VSS	GPIO[3]	VBATT	VBUS
F	VSS	GPIO[46]	GPIO[47]	FSLC[1]	TDI	VDD	VDD	VDD	VDD	GPIO[4]	GPIO[1]	GPIO[0]
G	VIO2	GPIO[43]	GPIO[44]	GPIO[45]	VSS	VSS	VDD	VSS	GPIO[9]	GPIO[7]	GPIO[6]	GPIO[2]
H	VSS	GPIO[40]	GPIO[41]	GPIO[42]	GPIO[39]	VSS	GPIO[20]	GPIO[18]	GPIO[14]	GPIO[12]	GPIO[8]	VIO1
J	VIO2	GPIO[38]	GPIO[37]	GPIO[36]	GPIO[31]	GPIO[27]	GPIO[25]	GPIO[22]	GPIO[19]	GPIO[15]	GPIO[10]	GPIO[5]
K	GPIO[35]	GPIO[34]	GPIO[33]	GPIO[32]	GPIO[28]	GPIO[26]	GPIO[16]	GPIO[21]	INT#	GPIO[24]	GPIO[11]	VSS
L	VDD	VSS	VDD	GPIO[30]	GPIO[29]	VIO1	GPIO[23]	VSS	VIO1	GPIO[17]	GPIO[13]	VSS

Note No ball is populated at location A9.

Figure 8. FX3 Hi-Speed 121-Ball BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	VDD	NC	NC	NC	NC	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	NC	FSLC[1]	VDD	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) .... –40 °C to +85 °C

Ambient temperature with power supplied (Commercial) .... 0 °C to +70 °C

Supply voltage to ground potential

V_{DD}, A_{VDDQ} ....1.25 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} ....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ....1.25 V

DC input voltage to any input pin .... V_{CC} + 0.3 V

DC voltage applied to outputs in high Z state .... V_{CC} + 0.3 V

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ....> 200 mA

Maximum output short-circuit current for all I/Os (cumulative)..–100 mA

Maximum output current per I/O (source or sink)....................... ....20 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial .... –40 °C to +85 °C

Commercial .... 0 °C to +70 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage ....1.15 V to 1.25 V

V_{BATT} supply voltage ....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage ....1.7 V to 3.6 V

V_{IO5} supply voltage .... 1.15 V to 3.6 V

DC Specifications

Table 8. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC – 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.

Figure 10. GPIF II Timing in Asynchronous Mode

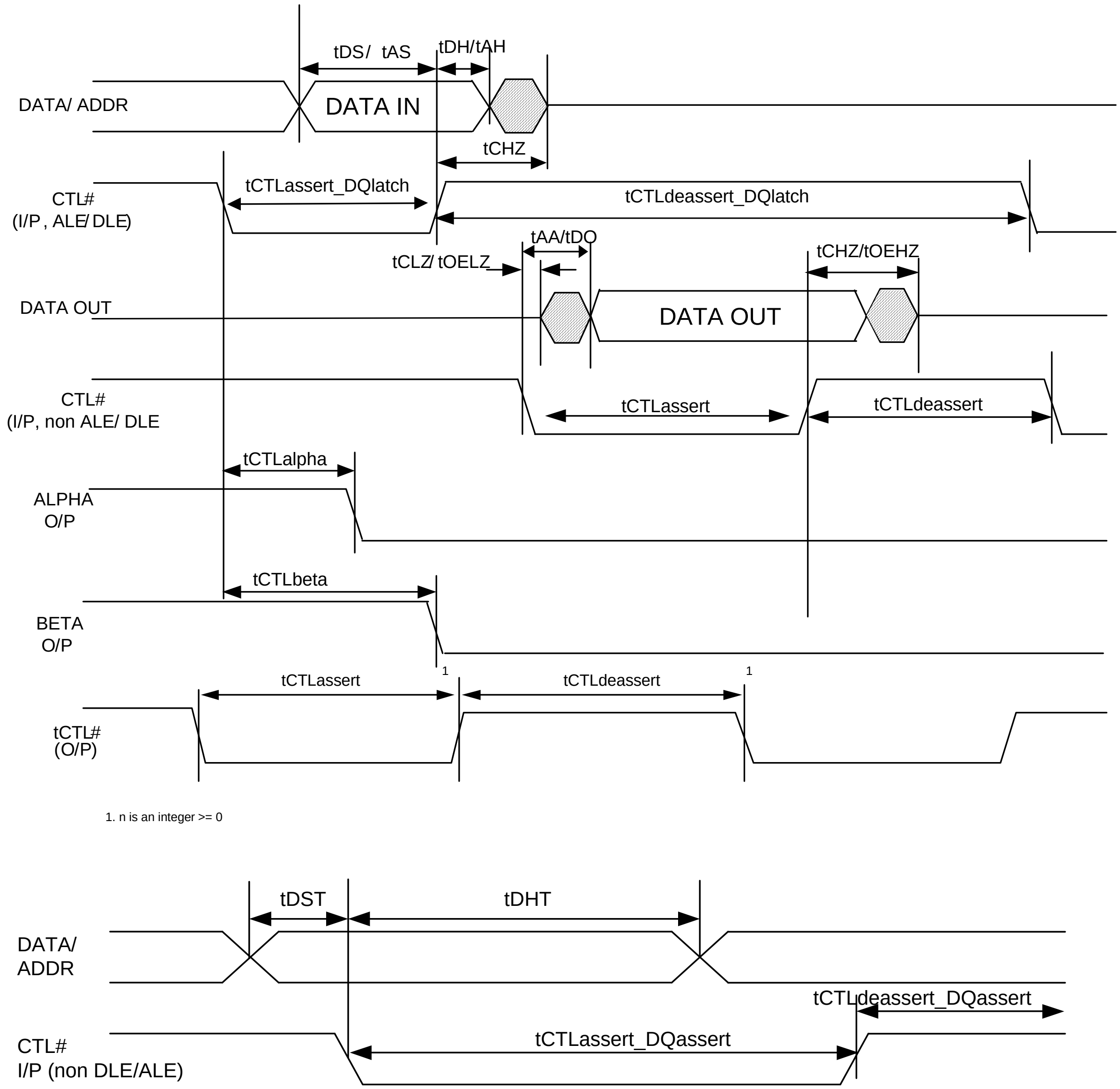
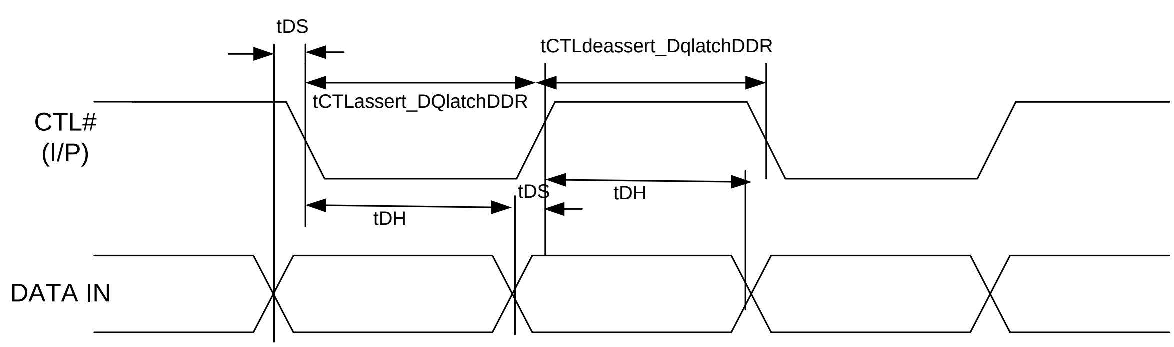


Figure 11. GPIF II Timing in Asynchronous DDR Mode



Asynchronous Slave FIFO Read Sequence Description

- FIFO address is stable and the SLCS# signal is asserted.
- SLOE# is asserted. This results in driving the data bus.
- SLRD # is asserted.
- Data from the FIFO is driven after assertion of SLRD#. This data is valid after a propagation delay of tRDO from the falling edge of SLRD#.
- FIFO pointer is incremented on deassertion of SLRD#

In Figure 15, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle, SLOE# must be in an asserted state. SLRD# and SLOE# can also be tied.

The same sequence of events is also shown for a burst read.

Note In the burst read mode, during SLOE# assertion, the data bus is in a driven state (data is driven from a previously addressed FIFO). After assertion of SLRD# data from the FIFO is driven on the data bus (SLOE# must also be asserted). The FIFO pointer is incremented after deassertion of SLRD#.

Figure 15. Asynchronous Slave FIFO Read Mode

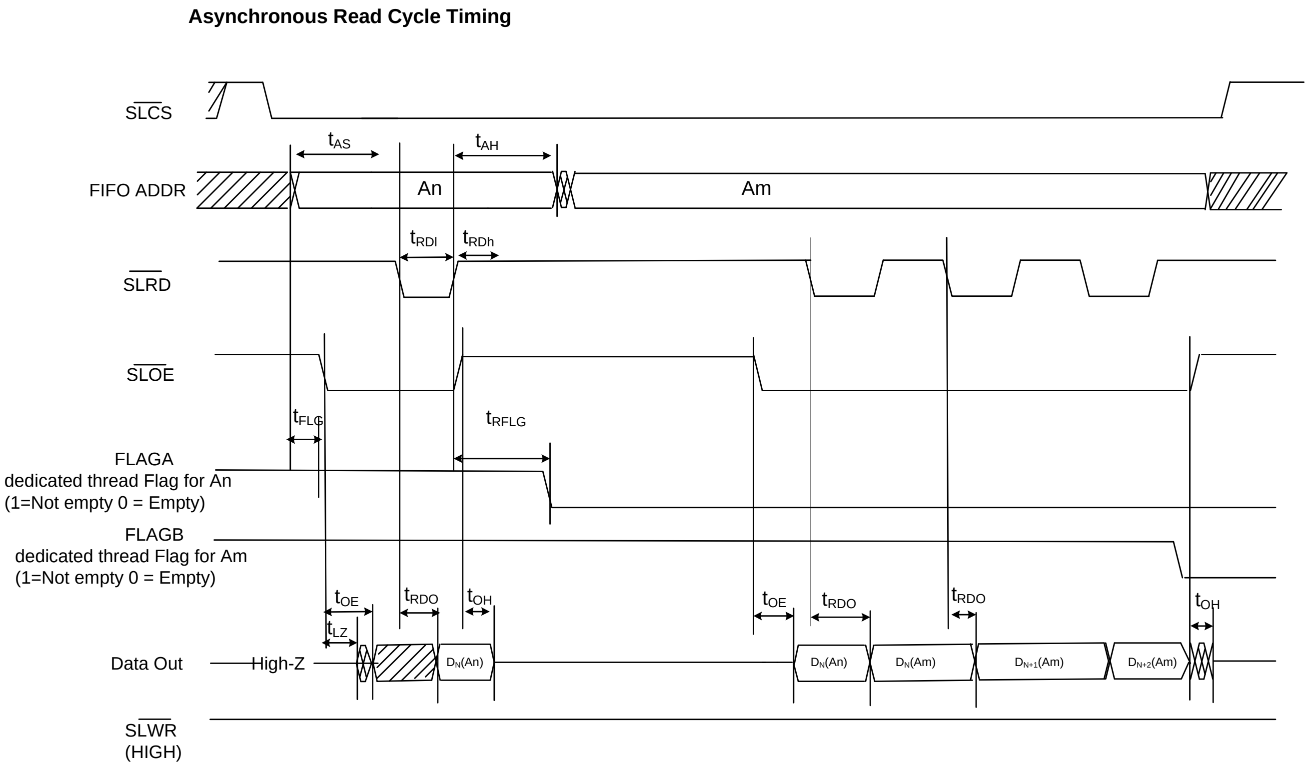
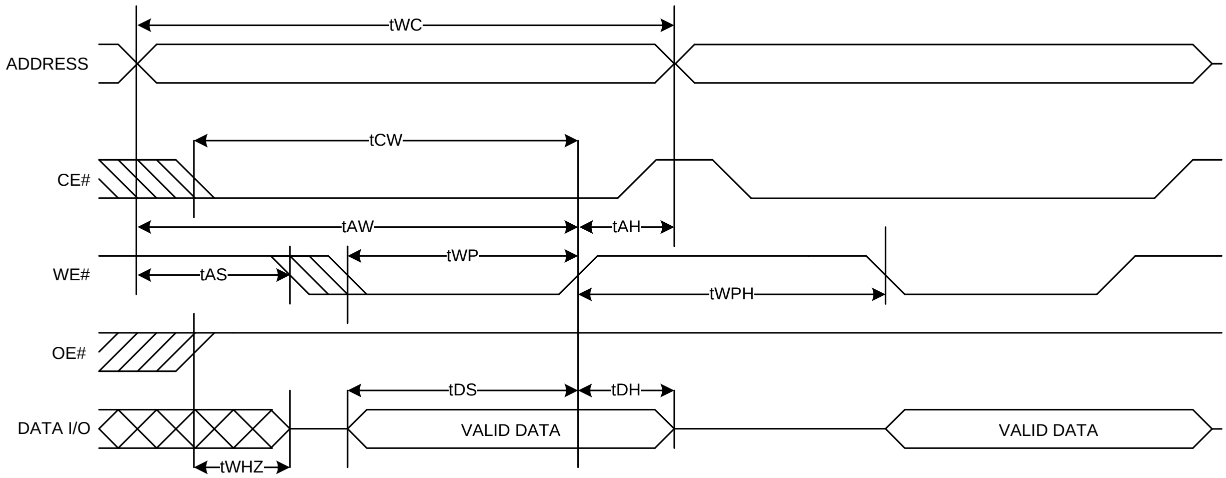
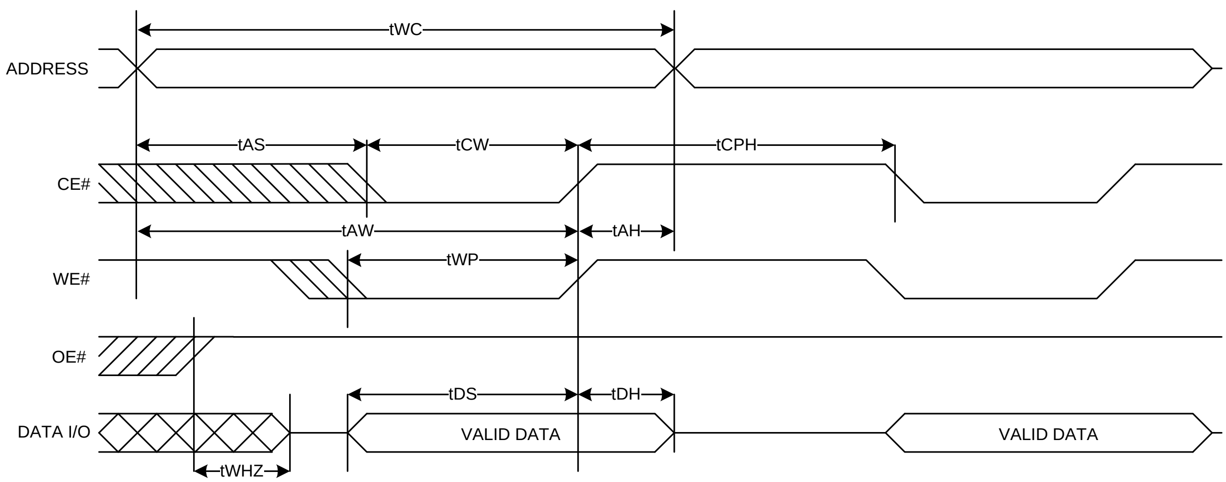


Figure 19. Non-multiplexed Asynchronous SRAM Write Timing (WE# and CE# Controlled)

Write Cycle 1 WE# Controlled, OE# High During Write

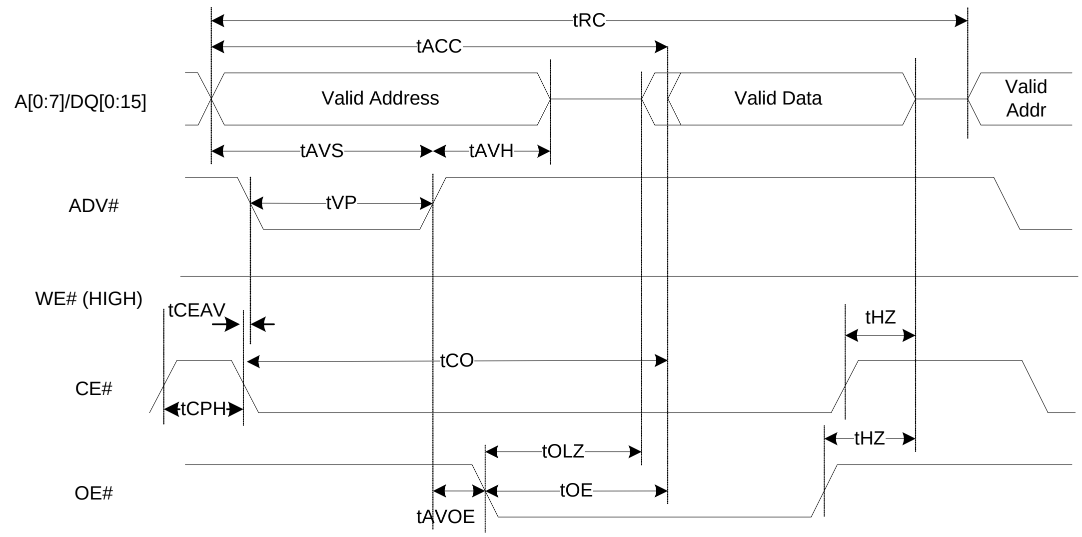


Write Cycle 2 CE# Controlled, OE# High During Write



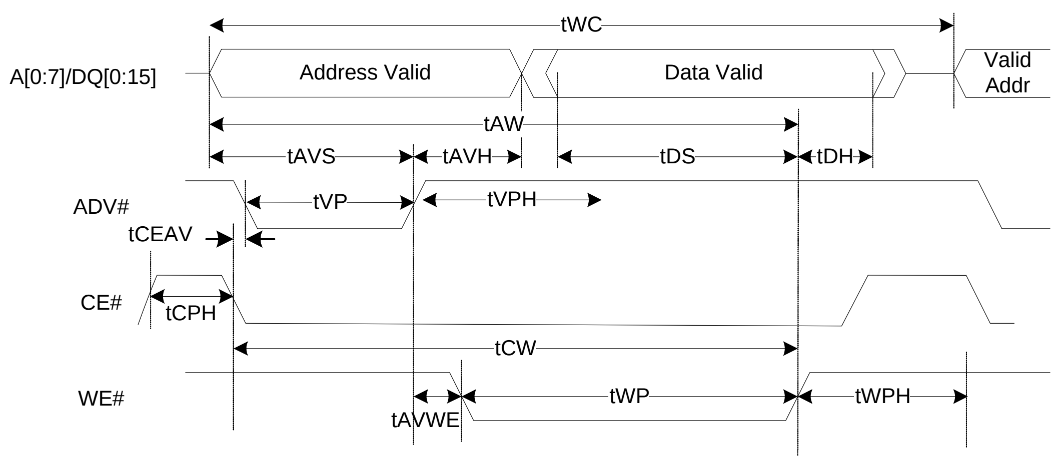
ADMux Timing for Asynchronous Access

Figure 21. ADMux Asynchronous Random Read



Note:
1. Multiple read cycles can be executed while keeping CE# low.
2. Read operation ends with either de-assertion of either OE# or CE#, whichever comes earlier.

Figure 22. ADMux Asynchronous Random Write



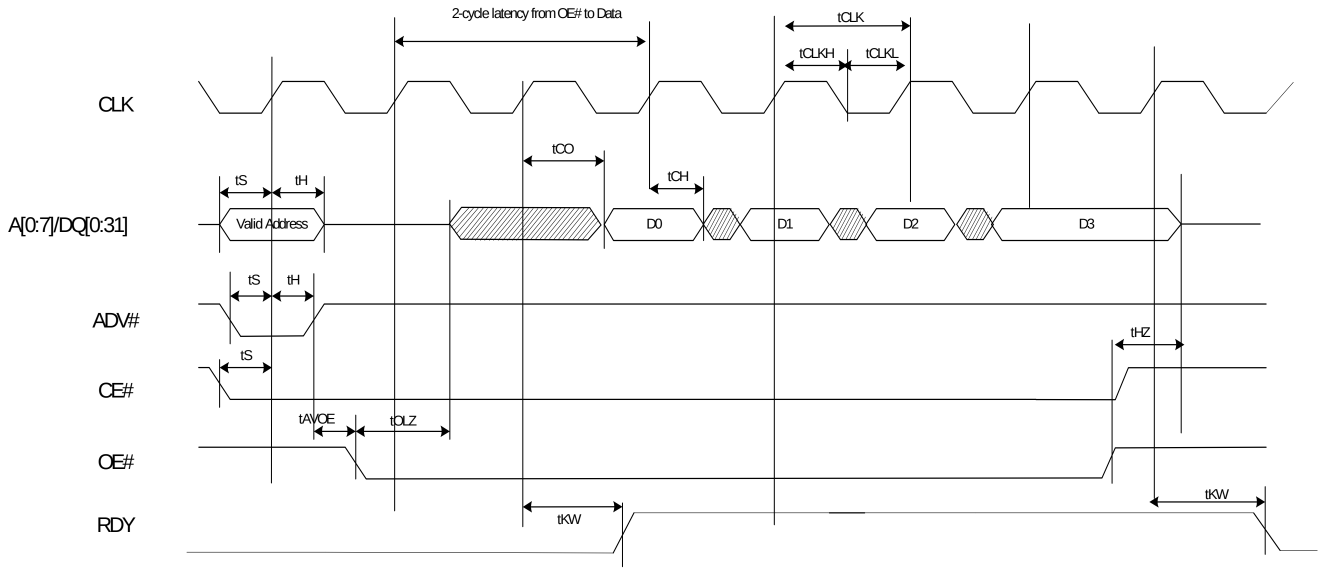
Note:
1. Multiple write cycles can be executed while keeping CE# low.
2. Write operation ends with de-assertion of either WE# or CE#, whichever comes earlier.

Table 14. Asynchronous ADMux Timing Parameters[8]

Parameter	Description	Min	Max	Units	Notes
ADMux Asynchronous READ Access Timing Parameters					
tRC	Read cycle time (address valid to address valid)	54.5	–	ns	This parameter is dependent on when the P-port processors deasserts OE#
tACC	Address valid to data valid	–	32	ns	–
tCO	CE# assert to data valid	–	34.5	ns	–
tAVOE	ADV# deassert to OE# assert	2	–	ns	–
tOLZ	OE# assert to data LOW-Z	0	–	ns	–
tOE	OE# assert to data valid	–	25	ns	–
tHZ	Read cycle end to data HIGH-Z	–	22.5	ns	–
ADMux Asynchronous WRITE Access Timing Parameters					
tWC	Write cycle time (Address Valid to Address Valid)	–	52.5	ns	–
tAW	Address valid to write end	30	–	ns	–
tCW	CE# assert to write end	30	–	ns	–
tAVWE	ADV# deassert to WE# assert	2	–	ns	–
tWP	WE# LOW pulse width	20	–	ns	–
tWPH	WE# HIGH pulse width	10	–	ns	–
tDS	Data valid setup to WE# deassert	18	–	ns	–
tDH	Data valid hold from WE# deassert	2	–	ns	–
ADMux Asynchronous Common READ/WRITE Access Timing Parameters					
tAVS	Address valid setup to ADV# deassert	5	–	ns	–
tAVH	Address valid hold from ADV# deassert	2	–	ns	–
tVP	ADV# LOW pulse width	7.5	–	ns	–
tCPH	CE# HIGH pulse width	10	–	ns	–
tVPH	ADV# HIGH pulse width	15	–	ns	–
tCEAV	CE# assert to ADV# assert	0	–	ns	–

Note
8. All parameters guaranteed by design and validated through characterization.

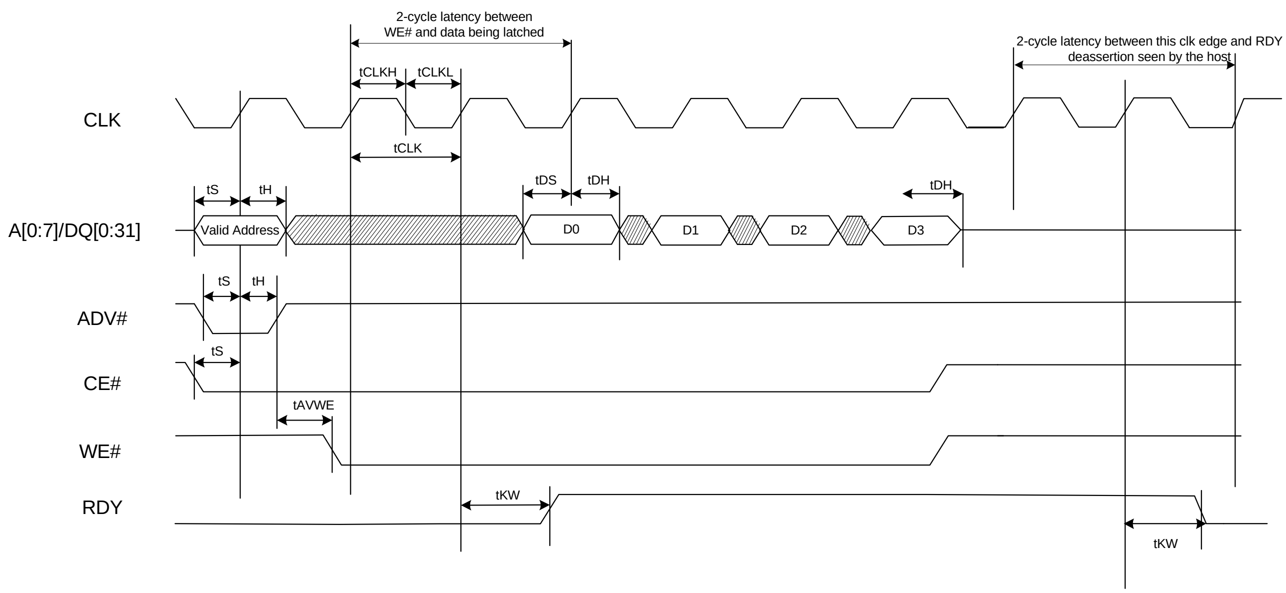
Figure 25. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 26. Sync ADMux Interface – Burst Write Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

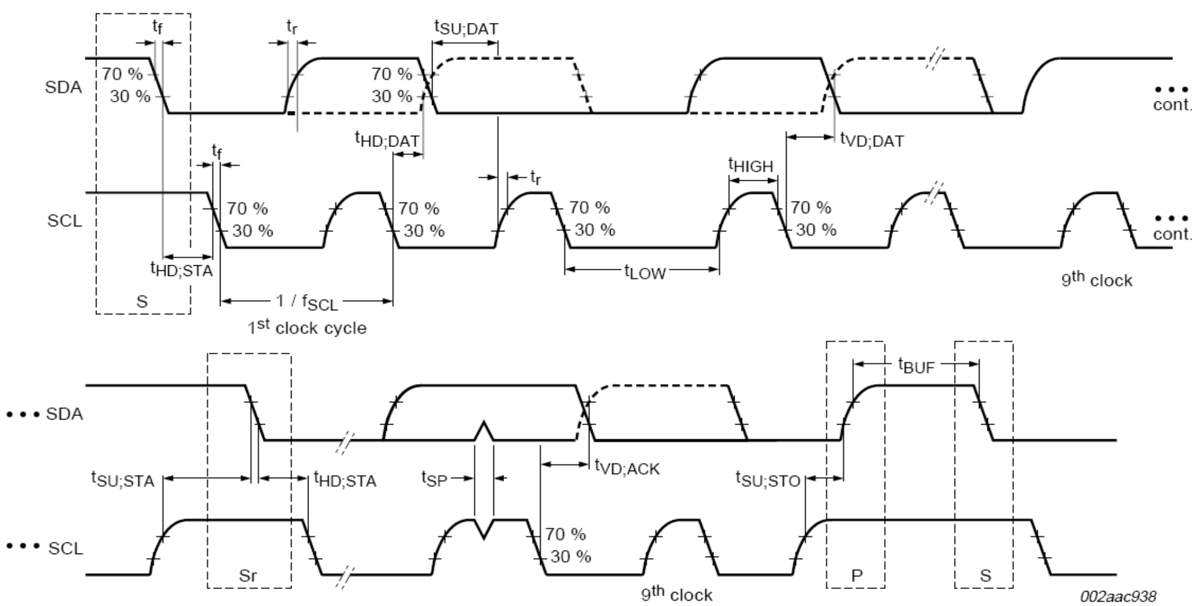
Table 15. Synchronous ADMux Timing Parameters[9]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Serial Peripherals Timing

I²C Timing

Figure 27. I²C Timing Definition



Note

9. All parameters guaranteed by design and validated through characterization.

Table 16. I2C Timing Parameters[10]

Parameter	Description	Min	Max	Units
I2C Standard Mode Parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I2C Fast Mode Parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

Note
10. All parameters guaranteed by design and validated through characterization.

Table 16. I^2C Timing Parameters[10] (continued)

Parameter	Description	Min	Max	Units
I^2C Fast Mode Plus Parameters (Not supported at I2C_VDDQ=1.2 V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	ns
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus-free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I^2S Timing Diagram

Figure 28. I^2S Transmit Cycle

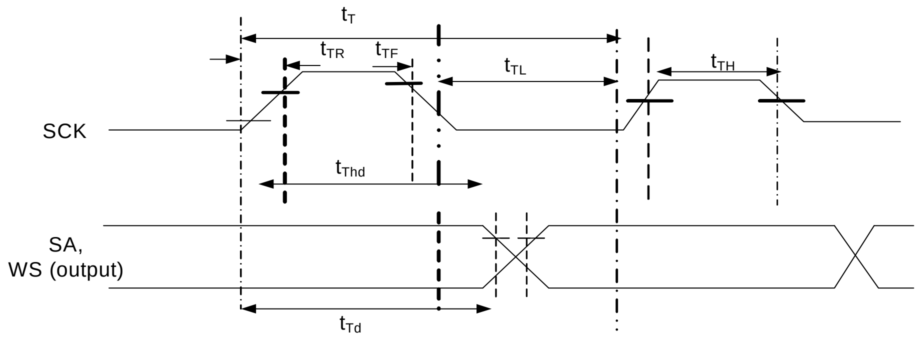


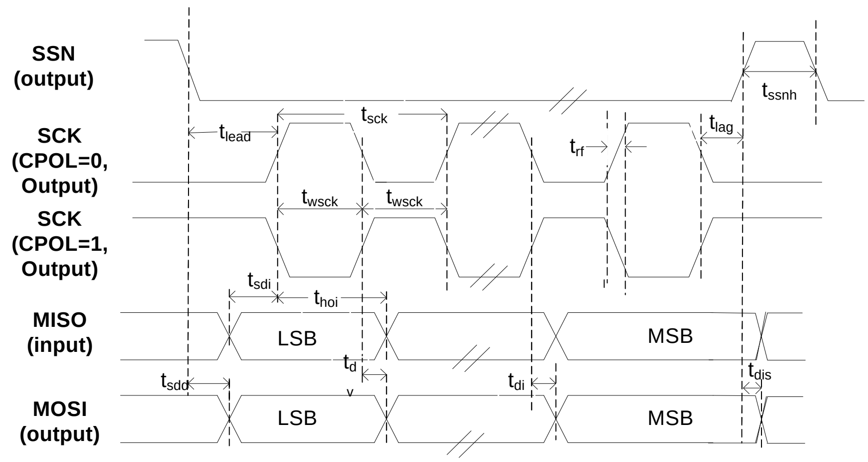
Table 17. I^2S Timing Parameters[11]

Parameter	Description	Min	Max	Units
tT	I^2S transmitter clock cycle	Ttr	–	ns
tTL	I^2S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I^2S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I^2S transmitter rise time	–	0.15 Ttr	ns
tTF	I^2S transmitter fall time	–	0.15 Ttr	ns
tThd	I^2S transmitter data hold time	0	–	ns
tTd	I^2S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

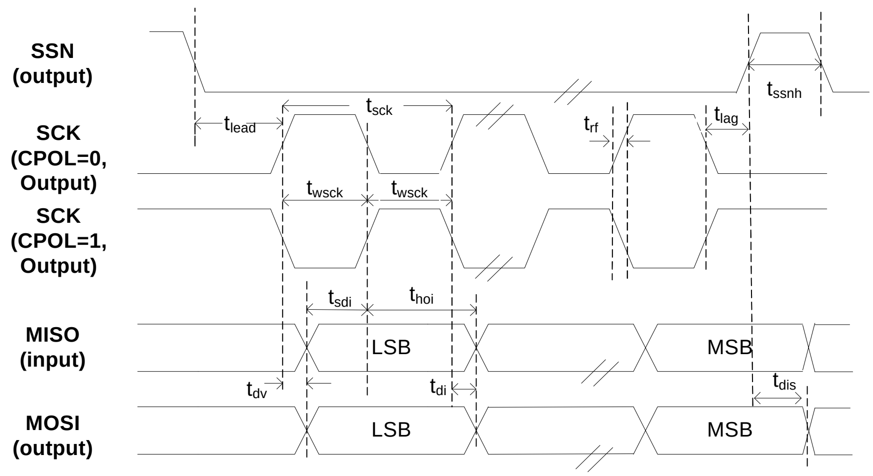
Note
11. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 29. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 18. SPI Timing Parameters[12]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[13]-5	1.5 tsck[13]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[13]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes

12. All parameters guaranteed by design and validated through characterization.
13. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Acronyms

Acronym	Description
DMA	direct memory access
FIFO	first in, first out
GPIF	general programmable interface
HNP	host negotiation protocol
I^2C	inter-integrated circuit
I^2S	inter IC sound
MISO	master in, slave out
MOSI	master out, slave in
MMC	multimedia card
MSC	mass storage class
MTP	media transfer protocol
OTG	on-the-go
OVP	overvoltage protection
PHY	physical layer
PLL	phase locked loop
PMIC	power management IC
PVT	process voltage temperature
RTOS	real-time operating system
SCL	serial clock line
SCLK	serial clock
SD	secure digital
SD	secure digital
SDA	serial data clock
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
SSN	SPI slave select (Active low)
UART	universal asynchronous receiver transmitter
UVC	USB Video Class
USB	universal serial bus
WLCSP	wafer level chip scale package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Errata

This section describes the errata for Revision C of the FX3. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYUSB301x-xxxx	All Variants
CYUSB201x-xxxx	All Variants

Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available Rev. C EZ-USB FX3 SuperSpeed USB Controller family devices.

Items	[Part Number]	Silicon Revision	Fix Status
1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
2. USB enumeration failure in USB boot mode when FX3 is self-powered.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
3. Extra ZLP is generated by the COMMIT action in the GPIF II state.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
4. Invalid PID Sequence in USB 2.0 ISOC data transfer.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
5. USB data transfer errors are seen when ZLP is followed by data packet within same microframe.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
6. Bus collision is seen when the I2C block is used as a master in the I2C Multi-master configuration.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Use FX3 in single-master configuration

1. **Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.**

   ■**Problem Definition**
   Turning off the VIO1 during Normal, Suspend, and Standby modes will cause the FX3 to stop working.

   ■**Parameters Affected**
   N/A

   ■**Trigger Conditions**
   This condition is triggered when the VIO1 is turned off during Normal, Suspend, and Standby modes.

   ■**Scope Of Impact**
   FX3 stops working.

   ■**Workaround**
   VIO1 must stay on during Normal, Suspend, and Standby modes.

   ■**Fix Status**
   No fix. Workaround is required.

2. **USB enumeration failure in USB boot mode when FX3 is self-powered.**

   ■**Problem Definition**
   FX3 device may not enumerate in USB boot mode when it is self-powered. The bootloader is designed for bus power mode. It does not make use of the VBUS pin on the USB connector to detect the USB connection and expect that USB bus is connected to host if it is powered. If FX3 is not already connected to the USB host when it is powered, then it enters into low-power mode and does not wake up when connected to USB host.

   ■**Parameters Affected**
   N/A

corresponding USB DMA socket on seeing the EOP condition. The channel operation can then be resumed as soon as the suspend callback is received.

- **Fix Status**
  No fix. Workaround is required.

6. Bus collision is seen when the I^{2}C block is used as a master in the I^{2}C Multi-master configuration.

- Problem definition
  When FX3 is used as a master in the I^{2}C multi-master configuration, there can be occasional bus collisions.
- Parameters affected
  NA
- Trigger Conditions
  This condition is triggered only when the FX3 I^{2}C block operates in Multi-master configuration.
- Scope Of Impact
  The FX3 I^{2}C block can transmit data when the I^{2}C bus is not idle leading to bus collision.
- Workaround
  Use FX3 as a single master.
- Fix Status
  No fix.

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