Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	SuperSpeed USB Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	GPIF, I²C, I²S, SPI, UART, USB
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	131-UFBGA, WLCSP
Supplier Device Package	131-WLCSP (5.1x4.7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3014-fbxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right <product> device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA87889, How to design with FX3/FX3S.

- Overview: USB Portfolio, USB Roadmap
- USB 3.0 Product Selectors: FX3, FX3S, CX3, HX3, West Bridge Benicia
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX3 are:
  - AN75705 - Getting Started with EZ-USB FX3
  - AN76405 - EZ-USB FX3 Boot Options
  - AN70707 - EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist
  - AN65974 - Designing with the EZ-USB FX3 Slave FIFO Interface
  - AN75779 - How to Implement an Image Sensor Interface with EZ-USB FX3 in a USB Video Class (UVC) Framework
  - AN86947 - Optimizing USB 3.0 Throughput with EZ-USB FX3
  - AN84868 - Configuring an FPGA over USB Using Cypress EZ-USB FX3
  - AN68829 - Slave FIFO Interface for EZ-USB FX3: 5-Bit Address Mode
  - AN73609 - EZ-USB FX2LP/ FX3 Developing Bulk-Loop Example on Linux
  - AN77960 - Introduction to EZ-USB FX3 High-Speed USB Host Controller
  - AN76348 - Differences in Implementation of EZ-USB FX2LP and EZ-USB FX3 Applications
  - AN89661 - USB RAID 1 Disk Design Using EZ-USB FX3S
- Code Examples: < Modify as required >
  - USB Hi-Speed
  - USB Full-Speed
  - USB SuperSpeed
- Technical Reference Manual (TRM):
  - EZ-USB FX3 Technical Reference Manual
- Development Kits:
  - CYUSB3KIT-003, EZ-USB FX3 SuperSpeed Explorer Kit
  - CYUSB3KIT-001, EZ-USB FX3 Development Kit
- Models: IBIS

EZ-USB FX3 Software Development Kit

Cypress delivers the complete software and firmware stack for FX3, in order to easily integrate SuperSpeed USB into any embedded application. The Software Development Kit (SDK) comes with tools, drivers and application examples, which help accelerate application development.

GPIF™ II Designer

The GPIF II Designer is a graphical software that allows designers to configure the GPIF II interface of the EZ-USB FX3 USB 3.0 Device Controller.

The tool allows users the ability to select from one of five Cypress supplied interfaces, or choose to create their own GPIF II interface from scratch. Cypress has supplied industry standard interfaces such as Asynchronous and Synchronous Slave FIFO, Asynchronous and Synchronous SRAM, and Asynchronous SRAM. Designers who already have one of these pre-defined interfaces in their system can simply select the interface of choice, choose from a set of standard parameters such as bus width (x8, 16, x32) endianess, clock settings, and compile the interface. The tool has a streamlined three step GPIF interface development process for users who need a customized interface. Users are able to first select their pin configuration and standard parameters. Secondly, they can design a virtual state machine using configurable actions. Finally, users can view output timing to verify that it matches the expected timing. Once the three step process is complete, the interface can be compiled and integrated with FX3.

Functional Overview

Cypress's EZ-USB FX3 is a SuperSpeed peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.1 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see Ordering Information on page 45) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I^2S.

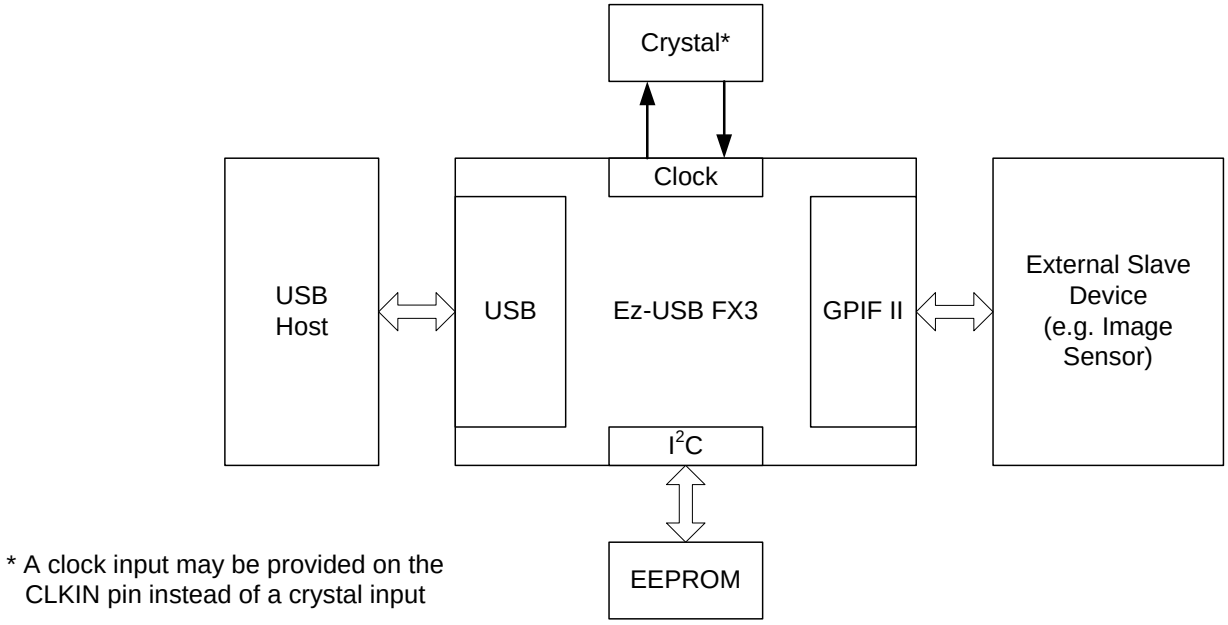
FX3 comes with application development tools. The software development kit comes with firmware and host application examples for accelerating time to market.

FX3 complies with the USB 3.1, Gen 1.0 specification and is also backward compatible with USB 2.0. It also complies with the Battery Charging Specification v1.1 and USB 2.0 OTG Specification v2.0.

Application Examples

In a typical application (see Figure 1), the FX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection. Additionally, FX3 can function as a coprocessor connecting via the GPIF II interface to an application processor (see Figure 2) and operates as a subsystem providing SuperSpeed USB connectivity to the application processor.

Figure 1. EZ-USB FX3 as Main Processor



ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

EZ-Dtect

FX3 supports USB Charger and accessory detection (EZ-Dtect). The charger detection mechanism complies with the Battery Charging Specification Revision 1.1. In addition to supporting this version of the specification, FX3 also provides hardware support to detect the resistance values on the ID pin.

FX3 can detect the following resistance ranges:

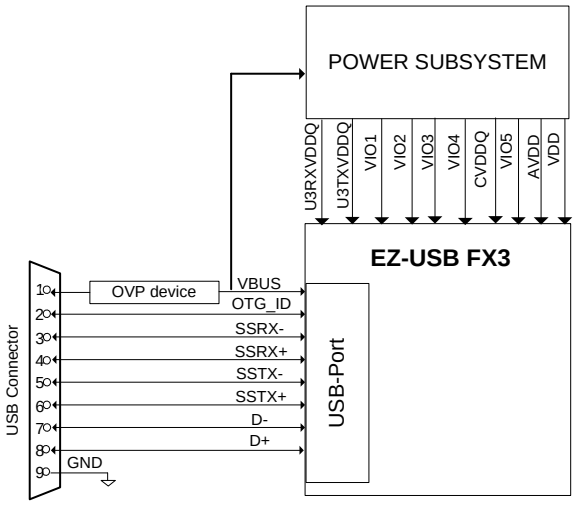
- Less than 10 Ω
- Less than 1 kΩ
- 65 kΩ to 72 kΩ
- 35 kΩ to 39 kΩ
- 99.96 kΩ to 104.4 kΩ (102 kΩ ± 2%)
- 119 kΩ to 132 kΩ
- Higher than 220 kΩ
- 431.2 kΩ to 448.8 kΩ (440 kΩ ± 2%)

FX3's charger detects a dedicated wall charger, Host/Hub charger, and Host/Hub.

VBUS Overvoltage Protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. Figure 3 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 8 for the operating range of VBUS and VBATT.

Figure 3. System Diagram with OVP Device For VBUS



Carkit UART Mode

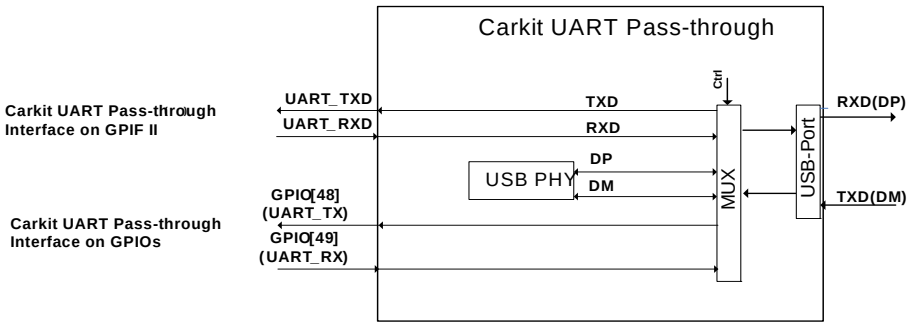
The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in Figure on page 8.

In this mode, FX3 supports a rate of up to 9600 bps.

Figure 4. Carkit UART Pass-through Block Diagram



Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 3.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in Table 4 on page 10.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4. FX3 Input Clock Specifications

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	
	10-kHz offset	–	–120	
	100-kHz offset	–	–128	
	1-MHz offset	–	–130	
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	
Undershoot	–	–	–3	
Rise time/fall time	–	–	3	ns

32-kHz Watchdog Timer Clock Input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer. Requirements for the optional 32-kHz clock input are listed in Table 5.

Table 5. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

Pin Description

Table 7. CYUSB3012 and CYUSB3014 Pin List

BGA	WLCSP	Power Domain	I/O	Name	Description					
					GPIF II Interface			Slave FIFO Interface		
F10	F1	VIO1	I/O	GPIO[0]	DQ[0]			DQ[0]		
F9	F2	VIO1	I/O	GPIO[1]	DQ[1]			DQ[1]		
F7	G1	VIO1	I/O	GPIO[2]	DQ[2]			DQ[2]		
G10	E3	VIO1	I/O	GPIO[3]	DQ[3]			DQ[3]		
G9	F3	VIO1	I/O	GPIO[4]	DQ[4]			DQ[4]		
F8	J1	VIO1	I/O	GPIO[5]	DQ[5]			DQ[5]		
H10	G2	VIO1	I/O	GPIO[6]	DQ[6]			DQ[6]		
H9	G3	VIO1	I/O	GPIO[7]	DQ[7]			DQ[7]		
J10	H2	VIO1	I/O	GPIO[8]	DQ[8]			DQ[8]		
J9	G4	VIO1	I/O	GPIO[9]	DQ[9]			DQ[9]		
K11	J2	VIO1	I/O	GPIO[10]	DQ[10]			DQ[10]		
L10	K2	VIO1	I/O	GPIO[11]	DQ[11]			DQ[11]		
K10	H3	VIO1	I/O	GPIO[12]	DQ[12]			DQ[12]		
K9	L2	VIO1	I/O	GPIO[13]	DQ[13]			DQ[13]		
J8	H4	VIO1	I/O	GPIO[14]	DQ[14]			DQ[14]		
G8	J3	VIO1	I/O	GPIO[15]	DQ[15]			DQ[15]		
J6	K6	VIO1	I/O	GPIO[16]	PCLK			CLK		
K8	L3	VIO1	I/O	GPIO[17]	CTL[0]			SLCS#		
K7	H5	VIO1	I/O	GPIO[18]	CTL[1]			SLWR#		
J7	J4	VIO1	I/O	GPIO[19]	CTL[2]			SLOE#		
H7	H6	VIO1	I/O	GPIO[20]	CTL[3]			SLRD#		
G7	K5	VIO1	I/O	GPIO[21]	CTL[4]			FLAGA		
G6	J5	VIO1	I/O	GPIO[22]	CTL[5]			FLAGB		
K6	L6	VIO1	I/O	GPIO[23]	CTL[6]			GPIO		
H8	K3	VIO1	I/O	GPIO[24]	CTL[7]			PKTEND#		
G5	J6	VIO1	I/O	GPIO[25]	CTL[8]			GPIO		
H6	K7	VIO1	I/O	GPIO[26]	CTL[9]			GPIO		
K5	J7	VIO1	I/O	GPIO[27]	CTL[10]			GPIO		
J5	K8	VIO1	I/O	GPIO[28]	CTL[11]			A1		
H5	L8	VIO1	I/O	GPIO[29]	CTL[12]			A0		
G4	L9	VIO1	I/O	GPIO[30]	PMODE[0]			PMODE[0]		
H4	J8	VIO1	I/O	GPIO[31]	PMODE[1]			PMODE[1]		
L4	K9	VIO1	I/O	GPIO[32]	PMODE[2]			PMODE[2]		
L8	K4	VIO1	I/O	INT#	INT#/CTL[15]			CTL[15]		
					32-bit Data Bus	16 - bit Data Bus + UART+SPI+I2S	16 - bit Data Bus + UART+GPIO	16 - bit Data Bus + SPI+GPIO	16 - bit Data Bus + I2S+GPIO	GPIO only
K2	K10	VIO2	I/O	GPIO[33]	DQ[16]	GPIO	GPIO	GPIO	GPIO	GPIO
J4	K11	VIO2	I/O	GPIO[34]	DQ[17]	GPIO	GPIO	GPIO	GPIO	GPIO
K1	K12	VIO2	I/O	GPIO[35]	DQ[18]	GPIO	GPIO	GPIO	GPIO	GPIO
J2	J9	VIO2	I/O	GPIO[36]	DQ[19]	GPIO	GPIO	GPIO	GPIO	GPIO
J3	J10	VIO2	I/O	GPIO[37]	DQ[20]	GPIO	GPIO	GPIO	GPIO	GPIO

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description					
J1	J11	VIO2	I/O	GPIO[38]	DQ[21]	GPIO	GPIO	GPIO	GPIO	GPIO
H2	H8	VIO2	I/O	GPIO[39]	DQ[22]	GPIO	GPIO	GPIO	GPIO	GPIO
H3	H11	VIO2	I/O	GPIO[40]	DQ[23]	GPIO	GPIO	GPIO	GPIO	GPIO
F4	H10	VIO2	I/O	GPIO[41]	DQ[24]	GPIO	GPIO	GPIO	GPIO	GPIO
G2	H9	VIO2	I/O	GPIO[42]	DQ[25]	GPIO	GPIO	GPIO	GPIO	GPIO
G3	G11	VIO2	I/O	GPIO[43]	DQ[26]	GPIO	GPIO	GPIO	GPIO	GPIO
F3	G10	VIO2	I/O	GPIO[44]	DQ[27]	GPIO	GPIO	GPIO	GPIO	GPIO
F2	G09	VIO2	I/O	GPIO[45]	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
F5	F11	VIO3	I/O	GPIO[46]	DQ[28]	UART_RT S	GPIO	GPIO	GPIO	GPIO
E1	F10	VIO3	I/O	GPIO[47]	DQ[29]	UART_CT S	GPIO	GPIO	GPIO	GPIO
E5	E11	VIO3	I/O	GPIO[48]	DQ[30]	UART_TX	GPIO	GPIO	GPIO	GPIO
E4	D12	VIO3	I/O	GPIO[49]	DQ[31]	UART_R X	GPIO	GPIO	GPIO	GPIO
D1	D11	VIO3	I/O	GPIO[50]	I2S_CLK	I2S_CLK	GPIO	GPIO	GPIO	GPIO
D2	E10	VIO3	I/O	GPIO[51]	I2S_SD	I2S_SD	GPIO	GPIO	GPIO	GPIO
D3	E9	VIO3	I/O	GPIO[52]	I2S_WS	I2S_WS	GPIO	GPIO	GPIO	GPIO
D4	D10	VIO4	I/O	GPIO[53]	UART_RTS	SPI_SCK	UART_RTS	SPI_SCK	GPIO	GPIO
C1	D9	VIO4	I/O	GPIO[54]	UART_CTS	SPI_SSN	UART_CTS	SPI_SSN	I2S_CLK	GPIO
C2	B12	VIO4	I/O	GPIO[55]	UART_TX	SPI_MIS O	UART_TX	SPI_MISO	I2S_SD	GPIO
D5	C12	VIO4	I/O	GPIO[56]	UART_RX	SPI_MOS I	UART_RX	SPI_MOSI	I2S_WS	GPIO
C4	E12	VIO4	I/O	GPIO[57]	I2S_MCLK	I2S_MCL K	GPIO	GPIO	I2S_MCL K	GPIO
					USB Port					
					CYUSB301X			**CYUSB201X**		
A3	A10	U3RXVD DQ	I	SSRXM	SSRX-			NC		
A4	B10	U3RXVD DQ	I	SSRXP	SSRX+			NC		
A6	A8	U3TXVD DQ	O	SSTXM	SSTX-			NC		
A5	B8	U3TXVD DQ	O	SSTXP	SSTX+			NC		
B3	B9	U3TXVD DQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND)			NC		
C9	C3	VBUS/ VBATT	I	OTG_ID	OTG_ID					
A9	A4	VBUS/V BATT	I/O	DP	D+					
A10	A2	VBUS/V BATT	I/O	DM	D–					
C8	B3	VBUS/VBAT T	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)					
					Clock and Reset					
B2	A7	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	B6	AVDD	I/O	XTALIN	XTALIN					
C7	B5	AVDD	I/O	XTALOUT	XTALOUT					
B4	F9	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	B7	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	C5	CVDDQ	I	CLKIN	CLKIN					

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
D6	C6	CVDDQ	I	CLKIN_32	CLKIN_32
C5	D8	CVDDQ	I	RESET#	RESET#
					I2C and JTAG
D9	D6	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL
D10	D2	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA
E7	F8	VIO5	I	TDI	TDI
C10	C2	VIO5	O	TDO	TDO
B11	C1	VIO5	I	TRST#	TRST#
E8	D5	VIO5	I	TMS	TMS
F6	D3	VIO5	I	TCK	TCK
D11	E8	VIO5	O	O[60]	Charger detect output
					Power
E10	E2	–	PWR	VBATT	–
B10	B1	–	PWR	VDD	–
–	A1	–	PWR	VDD	–
A1	C9	–	PWR	U3VSSQ	–
E11	E1	–	PWR	VBUS	–
D8	C4	–	PWR	VSS	–
H11	H1	–	PWR	VIO1	–
E2	K1	–	PWR	VSS	–
L9	L4	–	PWR	VIO1	–
G1	L5	–	PWR	VSS	–
–	L7	–	PWR	VIO1	–
–	L1	–	PWR	VSS	–
F1	J12	–	PWR	VIO2	–
G11	H12	–	PWR	VSS	–
	G12	–	PWR	VIO2	–
E3	C11	–	PWR	VIO3	–
L1	F12	–	PWR	VSS	–
B1	B11	–	PWR	VIO4	–
L6	A11	–	PWR	VSS	–
–	A12	–	PWR	VSS	–
B6	C7	–	PWR	CVDDQ	–
B5	C8	–	PWR	U3TXVDDQ	–
A2	C10	–	PWR	U3RXVDDQ	–
C11	D4	–	PWR	VIO5	–
L11	A3	–	PWR	VSS	–
A7	A5	–	PWR	AVDD	–
B7	A6	–	PWR	AVSS	–
C3	F4	–	PWR	VDD	–
B8	D1	–	PWR	VSS	–
E9	F5	–	PWR	VDD	–

Table 7. CYUSB3012 and CYUSB3014 Pin List (continued)

BGA	WLCSP	Power Domain	I/O	Name	Description
B9	E4	–	PWR	VSS	–
F11	F6	–	PWR	VDD	–
–	E5	–	PWR	VSS	**GND**
–	F7	–	PWR	VDD	–
–	E6	–	PWR	VSS	GND
–	E7	–	PWR	VSS	GND
H1	G6	–	PWR	VDD	–
L7	D7	–	PWR	VDD	–
J11	L10	–	PWR	VDD	–
L5	L12	–	PWR	VDD	–
K4	H7	–	PWR	VSS	–
L3	G7	–	PWR	VSS	–
K3	L11	–	PWR	VSS	–
L2	G8	–	PWR	VSS	–
A8	G5	–	PWR	VSS	–
–	B4	–	–	NC	No Connect
A11	B2	–	–	NC	No Connect

Table 8. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	–
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Figure 10. GPIF II Timing in Asynchronous Mode

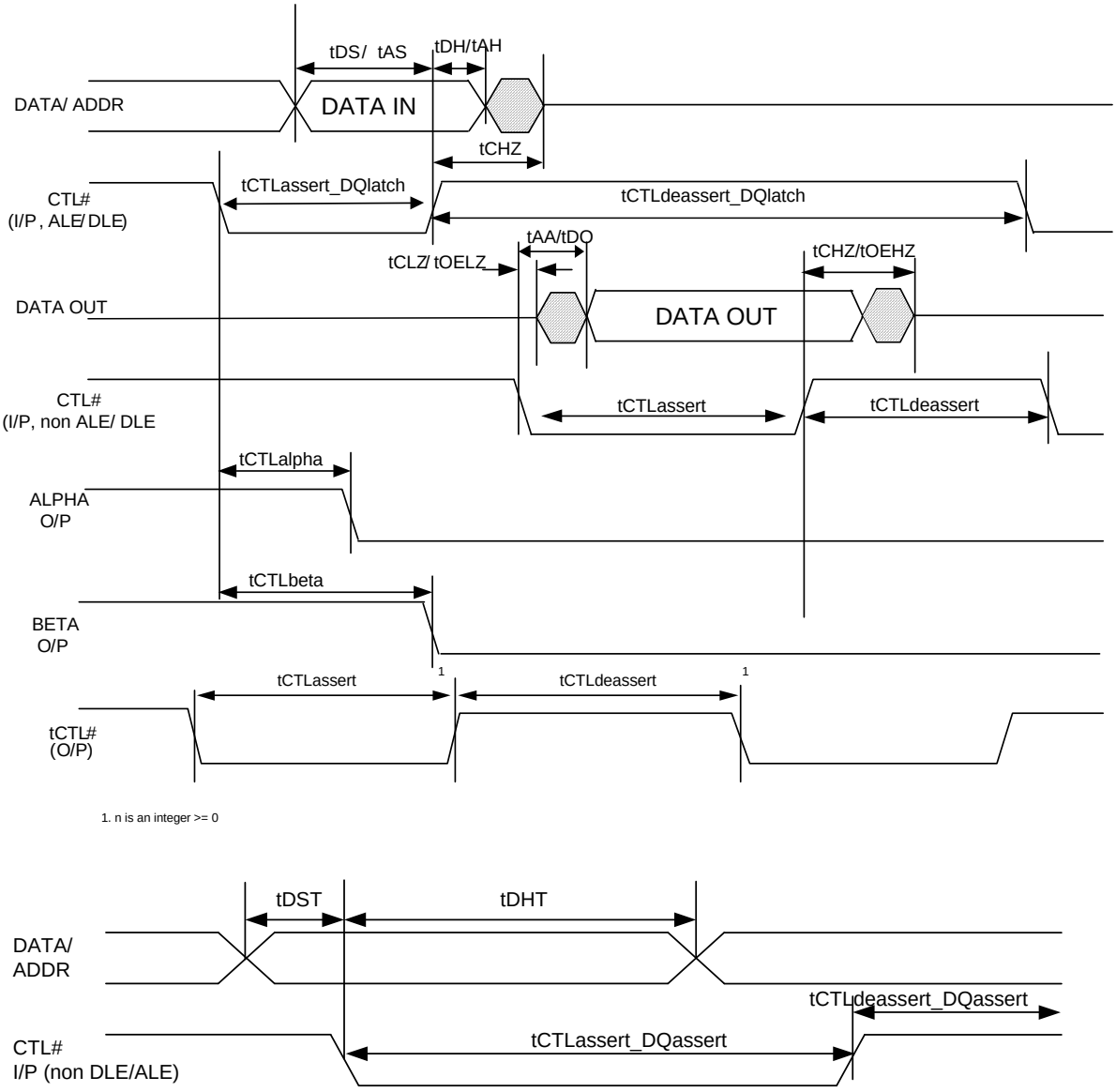


Figure 11. GPIF II Timing in Asynchronous DDR Mode

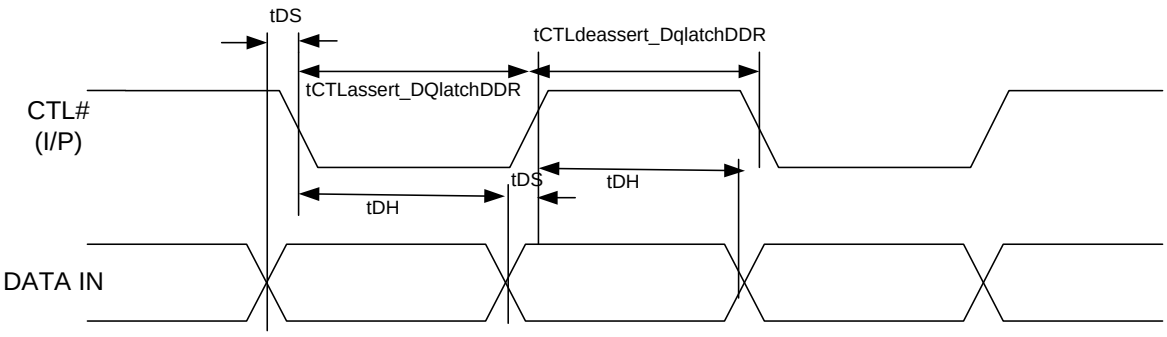


Table 10. GPIF II Timing in Asynchronous Mode[3, 4]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Notes
3. All parameters guaranteed by design and validated through characterization.
4. "alpha" output corresponds to "early output" and "beta" corresponds to "delayed output". Please refer to the GPIFII Designer Tool for the use of these outputs.

Asynchronous Slave FIFO Write Sequence Description

- FIFO address is driven and SLCS# is asserted
- SLWR# is asserted. SLCS# must be asserted with SLWR# or before SLWR# is asserted
- Data must be present on the tWRS bus before the deasserting edge of SLWR#
- Deassertion of SLWR# causes the data to be written from the data bus to the FIFO, and then the FIFO pointer is incremented
- The FIFO flag is updated after the tWFLG from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write.

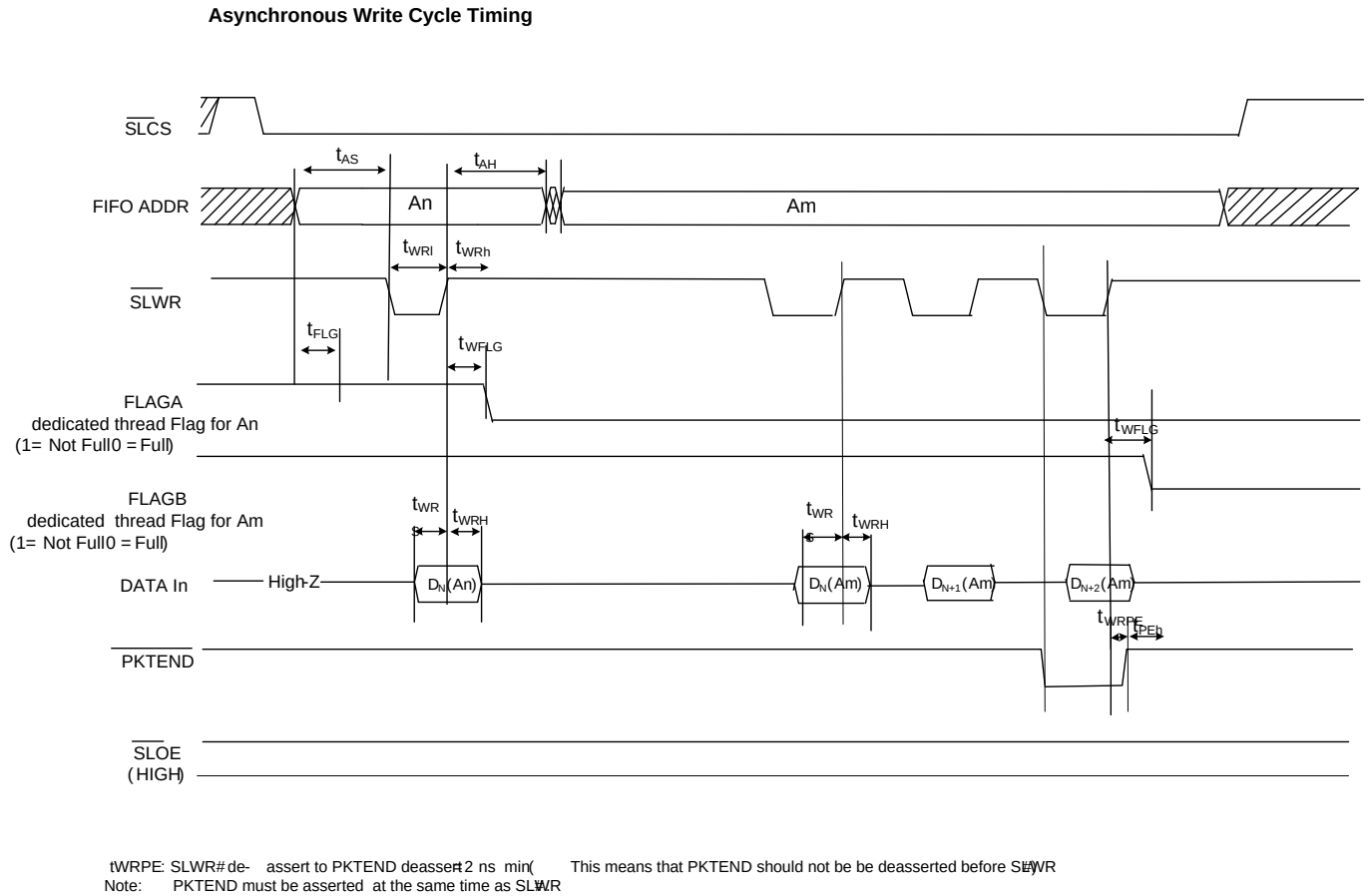
Note that in the burst write mode, after SLWR# deassertion, the data is written to the FIFO, and then the FIFO pointer is incremented.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a zero-length packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and the address must be driven as shown in Figure 17 on page 29.

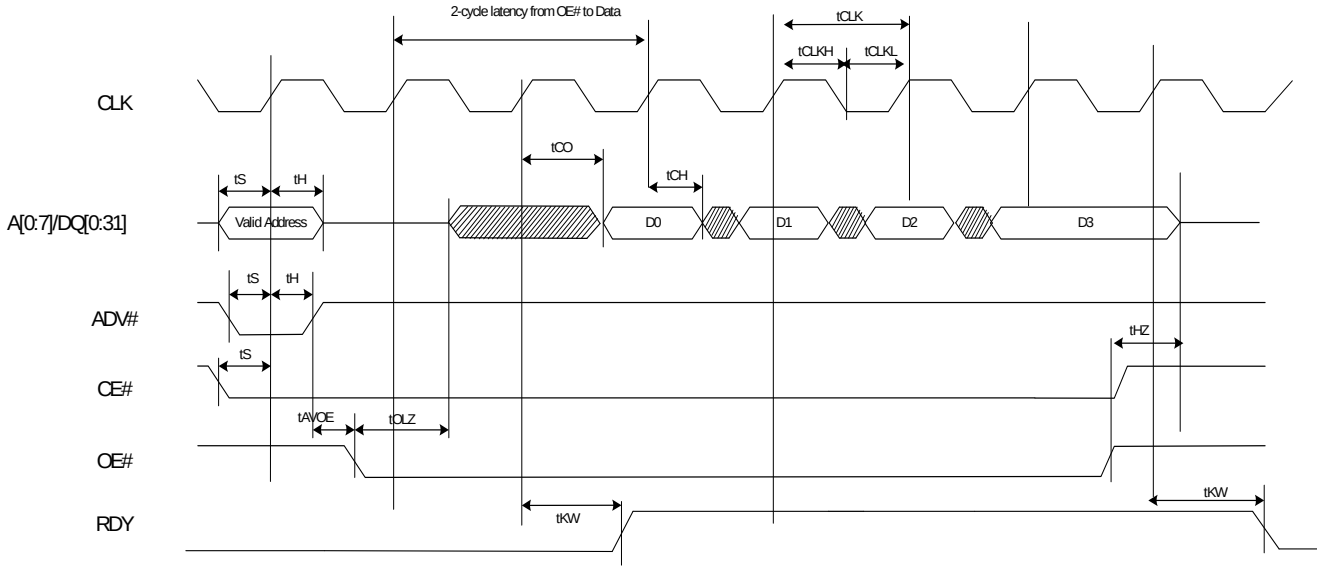
FLAG Usage: The FLAG signals are monitored by the external processor for flow control. FLAG signals are FX3 outputs that can be configured to show empty, full, and partial status for a dedicated address or the current address.

Figure 16. Asynchronous Slave FIFO Write Mode



tWRPE: SLWR# de- assert to PKTEND deasser+2 ns min(This means that PKTEND should not be be deasserted before SLWR
Note: PKTEND must be asserted at the same time as SLWR

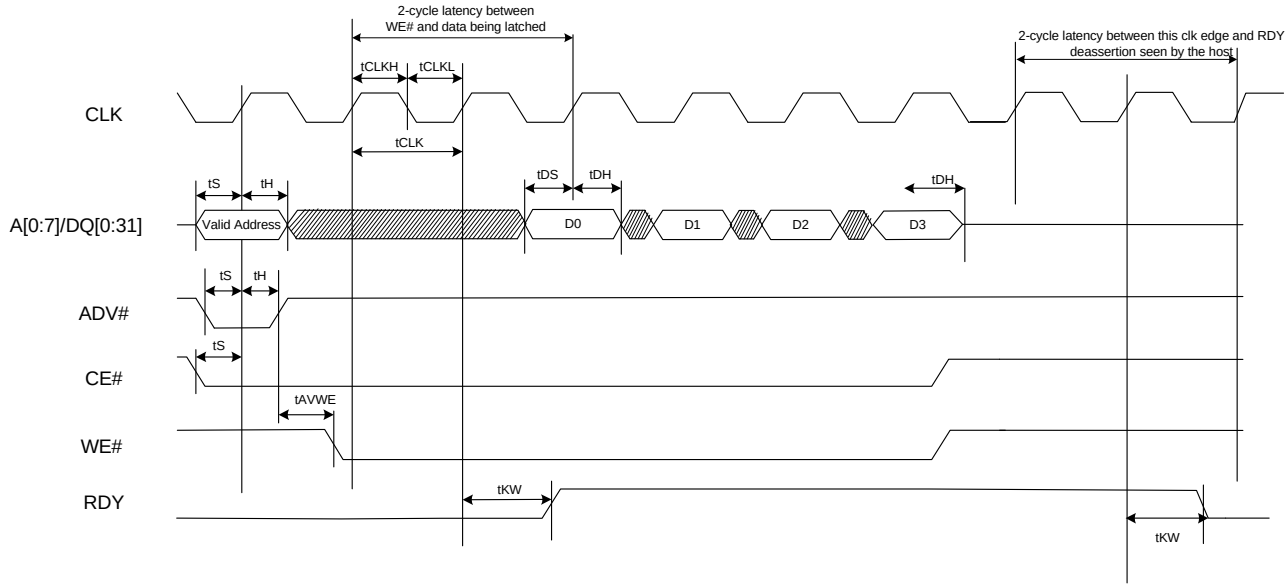
Figure 25. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 26. Sync ADMux Interface – Burst Write Timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

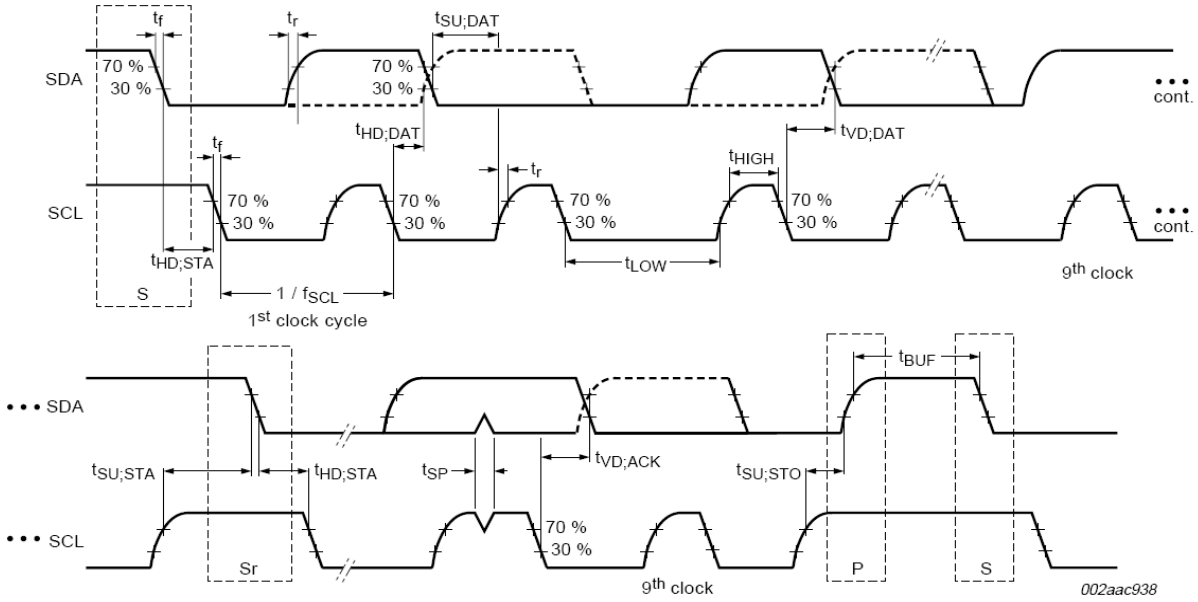
Table 15. Synchronous ADMux Timing Parameters[9]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Serial Peripherals Timing

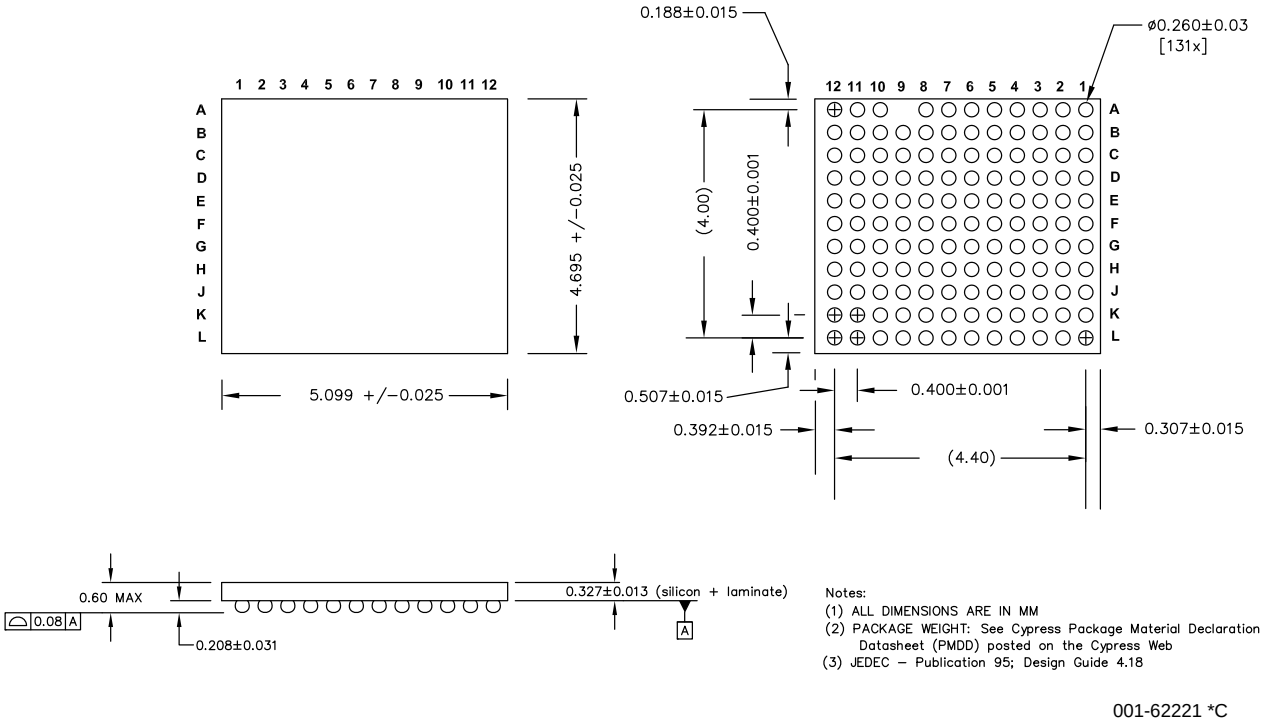
I^2C Timing

Figure 27. I^2C Timing Definition



Note
9. All parameters guaranteed by design and validated through characterization.

Figure 32. 131-ball WLCSP (5.099 × 4.695 × 0.60 mm) Package Diagram



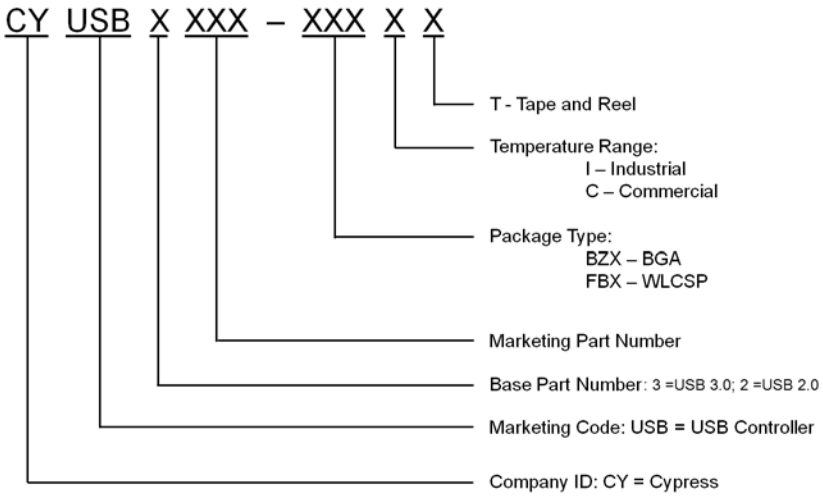
Note Underfill is required on the board design. Contact fx3@cypress.com for details.

Ordering Information

Table 20. Ordering Information

Ordering Code	USB	SRAM (kB)	GPIF II Data Bus Width	Operating Temperature	Package Type
CYUSB3011-BZXC	USB 3.0	256	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3012-BZXC	USB 3.0	256	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3013-BZXC	USB 3.0	512	16-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXC	USB 3.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB3014-BZXI	USB 3.0	512	32-bit	–40°C to +85°C	121-ball BGA
CYUSB3014-FBXCT	USB 3.0	512	32-bit	0 °C to +70 °C	131-ball WLCSP
CYUSB3014-FBXIT	USB 3.0	512	32-bit	–40 °C to +85 °C	131-ball WLCSP
CYUSB2014-BZXC	USB 2.0	512	32-bit	0 °C to +70 °C	121-ball BGA
CYUSB2014-BZXI	USB 2.0	512	32-bit	–40 °C to +85 °C	121-ball BGA

Ordering Code Definitions



Acronyms

Acronym	Description
DMA	direct memory access
FIFO	first in, first out
GPIF	general programmable interface
HNP	host negotiation protocol
I^2C	inter-integrated circuit
I^2S	inter IC sound
MISO	master in, slave out
MOSI	master out, slave in
MMC	multimedia card
MSC	mass storage class
MTP	media transfer protocol
OTG	on-the-go
OVP	overvoltage protection
PHY	physical layer
PLL	phase locked loop
PMIC	power management IC
PVT	process voltage temperature
RTOS	real-time operating system
SCL	serial clock line
SCLK	serial clock
SD	secure digital
SD	secure digital
SDA	serial data clock
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
SSN	SPI slave select (Active low)
UART	universal asynchronous receiver transmitter
UVC	USB Video Class
USB	universal serial bus
WLCSP	wafer level chip scale package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Errata

This section describes the errata for Revision C of the FX3. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYUSB301x-xxxx	All Variants
CYUSB201x-xxxx	All Variants

Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available Rev. C EZ-USB FX3 SuperSpeed USB Controller family devices.

Items	[Part Number]	Silicon Revision	Fix Status
1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
2. USB enumeration failure in USB boot mode when FX3 is self-powered.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
3. Extra ZLP is generated by the COMMIT action in the GPIF II state.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
4. Invalid PID Sequence in USB 2.0 ISOC data transfer.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
5. USB data transfer errors are seen when ZLP is followed by data packet within same microframe.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Workaround provided
6. Bus collision is seen when the I2C block is used as a master in the I2C Multi-master configuration.	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. C, B, ES	Use FX3 in single-master configuration

1. **Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.**

   ■Problem Definition
   Turning off the VIO1 during Normal, Suspend, and Standby modes will cause the FX3 to stop working.

   ■Parameters Affected
   N/A

   ■Trigger Conditions
   This condition is triggered when the VIO1 is turned off during Normal, Suspend, and Standby modes.

   ■Scope Of Impact
   FX3 stops working.

   ■Workaround
   VIO1 must stay on during Normal, Suspend, and Standby modes.

   ■Fix Status
   No fix. Workaround is required.

2. **USB enumeration failure in USB boot mode when FX3 is self-powered.**

   ■Problem Definition
   FX3 device may not enumerate in USB boot mode when it is self-powered. The bootloader is designed for bus power mode. It does not make use of the VBUS pin on the USB connector to detect the USB connection and expect that USB bus is connected to host if it is powered. If FX3 is not already connected to the USB host when it is powered, then it enters into low-power mode and does not wake up when connected to USB host.

   ■Parameters Affected
   N/A

Document History Page (continued)

Document Title: CYUSB301X/CYUSB201X, EZ-USB® FX3: SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	4368374	RSKV	05/02/2014	Updated Package Diagram: spec 001-62221 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*P	4474200	ANOP	08/14/2014	Added CYUSB201x MPNs, ball map, and pin list to the datasheet.
*Q	4668496	DBIR	02/24/2015	Updated Features. Updated Logic Block Diagram. Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Added More Information. Updated Functional Overview: Updated Application Examples: Updated Figure 1. Updated Figure 2. Updated USB Interface: Updated description. Removed Figure “USB Interface Signals”. Updated Pin Configurations: Updated Figure 6. Updated Reset: Updated Hard Reset: Updated description. Updated Pin Description: Updated Table 7: Updated entire table. Modified CVDDQ power domain description. Removed Table “CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width)”. Removed Table “CYUSB2014 Pin List (GPIF II with 32-bit Data Bus Width)”. Updated Electrical Specifications: Updated DC Specifications: Added ISS parameter and its details. Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11. Updated AC Timing Parameters: Added Host Processor Interface (P-Port) Timing. Updated Acronyms. Added Errata. Replaced West Bridge Benicia with FX3.
*R	4703347	AMDK	03/27/2015	Updated Slave FIFO Interface: Updated Synchronous Slave FIFO Read Sequence Description: Updated Figure 12. Updated Synchronous Slave FIFO Write Sequence Description: Updated Figure 13. Updated Table 11: Updated minimum value of tSSD parameter. Added tACCD, tFAD parameters and their details.
*S	5160624	AJAI	04/07/2016	Removed ISS parameter. Added item 6 in Errata.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support