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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21060ks-160

PARALLEL COMPUTATIONS

Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch

Multiply with add and subtract for accelerated FFT butterfly computation

UP TO 4M BIT ON-CHIP SRAM

Dual-ported for independent access by core processor and DMA

OFF-CHIP MEMORY INTERFACING

4 gigawords addressable

Programmable wait state generation, page-mode DRAM support

DMA CONTROLLER

10 DMA channels for transfers between ADSP-2106x internal memory and external memory, external peripherals, host processor, serial ports, or link ports

Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

HOST PROCESSOR INTERFACE TO 16- AND 32-BIT MICROPROCESSORS

Host can directly read/write ADSP-2106x internal memory and IOP registers

MULTIPROCESSING

Glueless connection for scalable DSP multiprocessing architecture

Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-2106xs plus host

Six link ports for point-to-point connectivity and array multiprocessing

240 MBps transfer rate over parallel bus

240 MBps transfer rate over link ports

SERIAL PORTS

Two 40 Mbps synchronous serial ports with companding hardware

Independent transmit and receive functions

Table 1. ADSP-2106x SHARC Processor Family Features

Feature	ADSP-21060	ADSP-21062	ADSP-21060L	ADSP-21062L	ADSP-21060C	ADSP-21060LC
SRAM	4M bits	2M bits	4M bits	2M bits	4M bits	4M bits
Operating Voltage	5 V	5 V	3.3 V	3.3 V	5 V	3.3 V
Instruction Rate	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz
Package	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	CQFP	CQFP

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-2106x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2106x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-2106x's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2106x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2106x can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2106x processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21062/ADSP-21062L contains two megabits of on-chip SRAM, and the ADSP-21060/ADSP-21060L contains 4M bits of on-chip SRAM. The internal memory is organized as two equal sized blocks of 1M bit each for the ADSP-21062/ADSP-21062L and two equal sized blocks of 2M bits each for the ADSP-21060/ADSP-21060L. Each can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

On the ADSP-21062/ADSP-21062L, the memory can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 40k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words.

On the ADSP-21060/ADSP-21060L, the memory can be configured as a maximum of 128k words of 32-bit data, 256k words of 16-bit data, 80k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-bit, 32-bit or 48-bit words.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

On-Chip Memory and Peripherals Interface

The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold and disable time requirements.

Host Processor Interface

The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-2106x's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where% is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	745	mA
	t_{CK} = 25 ns, V_{DD} = Max	850	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	575	mA
	t_{CK} = 25 ns, V_{DD} = Max	670	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	340	mA
	t_{CK} = 25 ns, V_{DD} = Max	390	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	200	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106x state during execution of IDLE instruction.

ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (3.3 V)

		A Grade		C Grade		K Grade		
Parameter	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{DD}	Supply Voltage	3.15	3.45	3.15	3.45	3.15	3.45	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	**Description**	**Test Conditions**	**Min**	**Max**	**Unit**
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	μA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	μA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\text{ V})$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 6. External Power Calculations (3.3 V Devices)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W
						P_{EXT} = 0.074 W

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed Table 7 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	ADSP-21060/ADSP-21060C ADSP-21062 5 V	ADSP-21060L/ADSP-21060LC ADSP-21062L 3.3 V
Supply Voltage (V_{DD})	–0.3 V to +7.0 V	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF	200 pF
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C
Lead Temperature (5 seconds)	280°C	280°C
Junction Temperature Under Bias	130°C	130°C

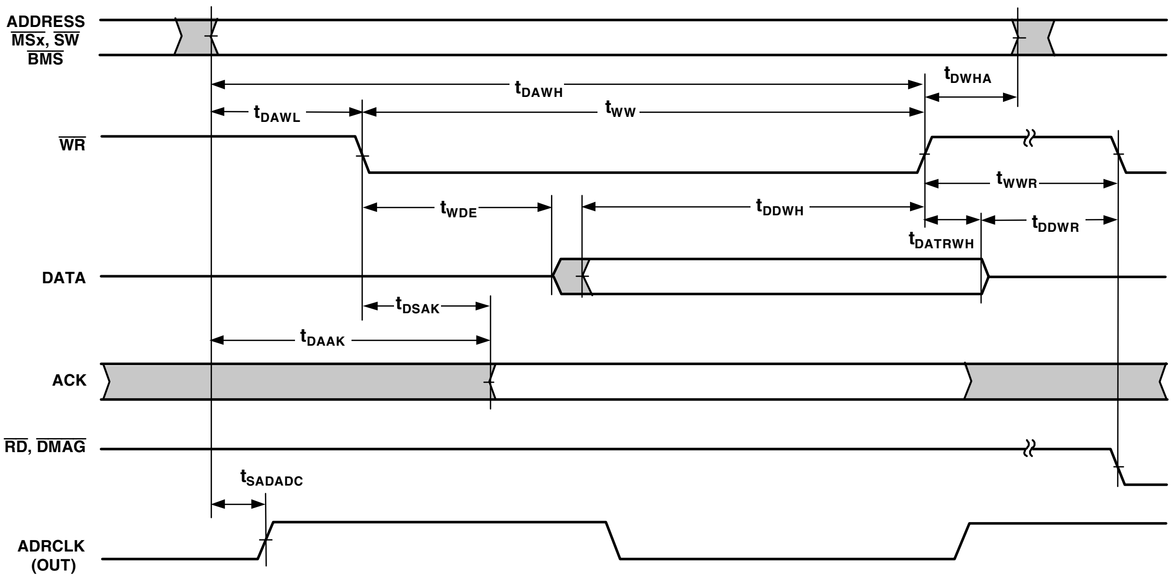

Figure 15. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 30). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 16. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	3 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[1, 2]		14 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[2]	6.5+DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{\text{MSx}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$ Delay After CLKIN[1]		7 – DT/8	ns
t_{HADRO}	Address, $\overline{\text{MSx}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{\text{RD}}$ High Delay After CLKIN	–2 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{\text{WR}}$ High Delay After CLKIN	–3 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Low Delay After CLKIN	8 + DT/4	12.5 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] The falling edge of $\overline{\text{MSx}}$, $\overline{\text{SW}}$, $\overline{\text{BMS}}$ is referenced.

[2] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

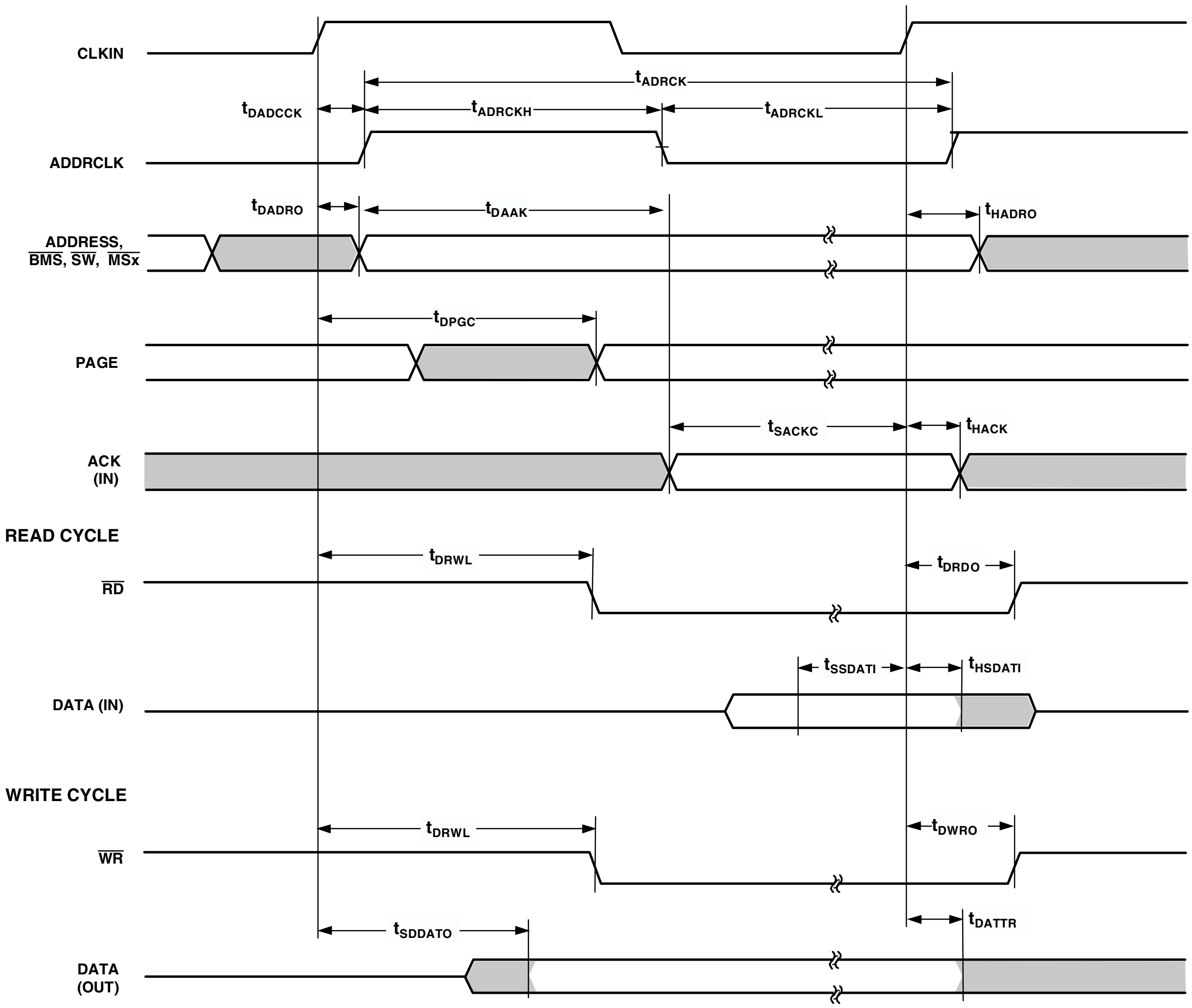

Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet the bus slave timing requirements.

Table 17. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{\text{SW}}$ Setup Before CLKIN	15 + DT/2		ns
t_{HADRI}	Address, $\overline{\text{SW}}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{\text{RD}}/\overline{\text{WR}}$ Low Setup Before CLKIN[1]	9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{\text{RD}}/\overline{\text{WR}}$ Low Hold After CLKIN[2]	–4 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{\text{RD}}/\overline{\text{WR}}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{\text{WR}}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{\text{WR}}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN[3]		18 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{\text{SW}}$[5]		9	ns
t_{ACKTR}	ACK Disable After CLKIN[5]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.
[2] For ADSP-21060C specification is –3.5 – 5DT/16 ns min, 8 + 7DT/16 ns max; for ADSP-21060LC specification is –3.75 – 5DT/16 ns min, 8 + 7DT/16 ns max.
[3] For ADSP-21062/ADSP-21062L/ADSP-21060C specification is 19 + 5DT/16 ns max; for ADSP-21060LC specification is 19.25 + 5DT/16 ns max.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] t_{DACKAD} is true only if the address and $\overline{\text{SW}}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

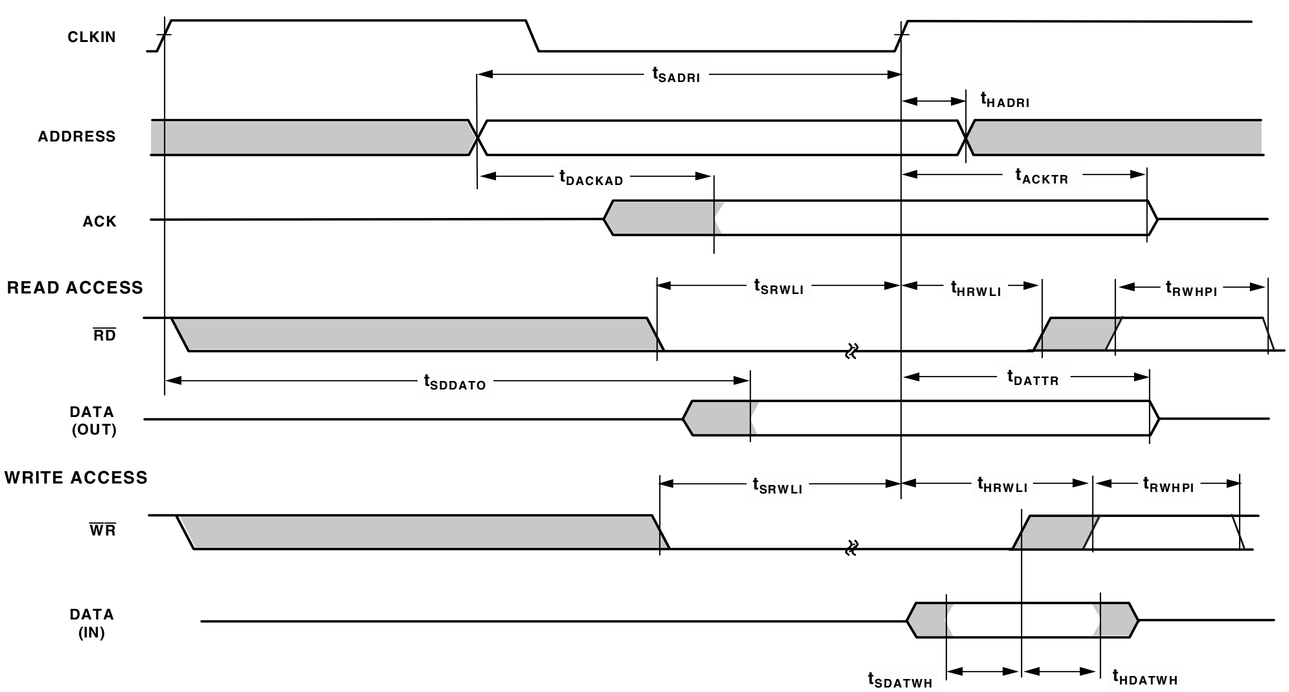

Figure 17. Synchronous Read/Write—Bus Slave

Asynchronous Read/Write—Host to ADSP-2106x

Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ (low). After $\overline{\text{HBG}}$ is returned by the ADSP-2106x, the host can drive the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins to access the ADSP-2106x's internal memory or IOP registers. $\overline{\text{HBR}}$ and $\overline{\text{HBG}}$ are assumed low for this timing. Not required if and address are valid $t_{HBGRCSV}$ after goes low. For first access after asserted, ADDR31–0 must be a non-MMS value 1/2 t_{CLK} before or goes low or by $t_{HBGRCSV}$ after goes low. This is easily accomplished by driving an upper address signal high when is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual*, Revision 2.1.

Table 19. Read Cycle

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{\text{CS}}$ Low Before $\overline{\text{RD}}$ Low[1]	0		ns
t_{HADRDH}	Address Hold/$\overline{\text{CS}}$ Hold Low After $\overline{\text{RD}}$	0		ns
t_{WRWH}	$\overline{\text{RD}}$/$\overline{\text{WR}}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{\text{RD}}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{\text{RD}}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{\text{RD}}$ Low[2]		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulse Width for Read	45 + 21DT/16		ns
t_{HDARWH}	Data Disable After $\overline{\text{RD}}$ High[3]	2	8	ns

[1] Not required if $\overline{\text{RD}}$ and address are valid $t_{HBGRCSV}$ after $\overline{\text{HBG}}$ goes low. For first access after $\overline{\text{HBR}}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CLK} before $\overline{\text{RD}}$ or $\overline{\text{WR}}$ goes low or by $t_{HBGRCSV}$ after $\overline{\text{HBG}}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{\text{HBG}}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual,* Revision 2.1.

[2] For ADSP-21060L, specification is 10.5 ns max; for ADSP-21060LC, specification is 12.5 ns max.

[3] For ADSP-21060L/ADSP-21060LC, specification is 2 ns min, 8.5 ns max.

Table 20. Write Cycle

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{\text{CS}}$ Low Setup Before $\overline{\text{WR}}$ Low	0		ns
t_{HCSWRH}	$\overline{\text{CS}}$ Low Hold After $\overline{\text{WR}}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{\text{WR}}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{\text{WR}}$ High	2		ns
t_{WWRL}	$\overline{\text{WR}}$ Low Width	7		ns
t_{WRWH}	$\overline{\text{RD}}$/$\overline{\text{WR}}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{\text{WR}}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{\text{WR}}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{\text{WR}}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{\text{WR}}$/$\overline{\text{CS}}$ Low		10	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulse Width for Write	15 + 7DT/16		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

Table 27. Link Ports—Transmit

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLACH}	LACK Setup Before LCLK High	19		19		ns
t_{HLACH}	LACK Hold After LCLK High	–6.75		–6.5		ns
Switching Characteristics						
t_{DLCLK}	Data Delay After CLKIN		8		8	ns
t_{DLDCH}	Data Delay After LCLK High[1]		2.25		2.25	ns
t_{HLDCH}	Data Hold After LCLK High[2]	–2.0		–2		ns
$t_{LCLKTWL}$	LCLK Width Low[3]	$(t_{CK}/4) - 1$	$(t_{CK}/4) + 1.25$	$(t_{CK}/4) - 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High[4]	$(t_{CK}/4) - 1.25$	$(t_{CK}/4) + 1$	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$(t_{CK}/4) + 9$	$(3 \times t_{CK}/4) + 16.5$	$(t_{CK}/4) + 9$	$(3 \times t_{CK}/4) + 16.5$	ns

[1] For ADSP-21060/ADSP-21060C, specification is 2.5 ns max.
[2] For ADSP-21062L, specification is –2.25 ns min.
[3] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C/ADSP-21062L, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1.5$ ns max.
[4] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C, specification is $(t_{CK}/4) - 1.5$ ns min, $(t_{CK}/4) + 1$ ns max.

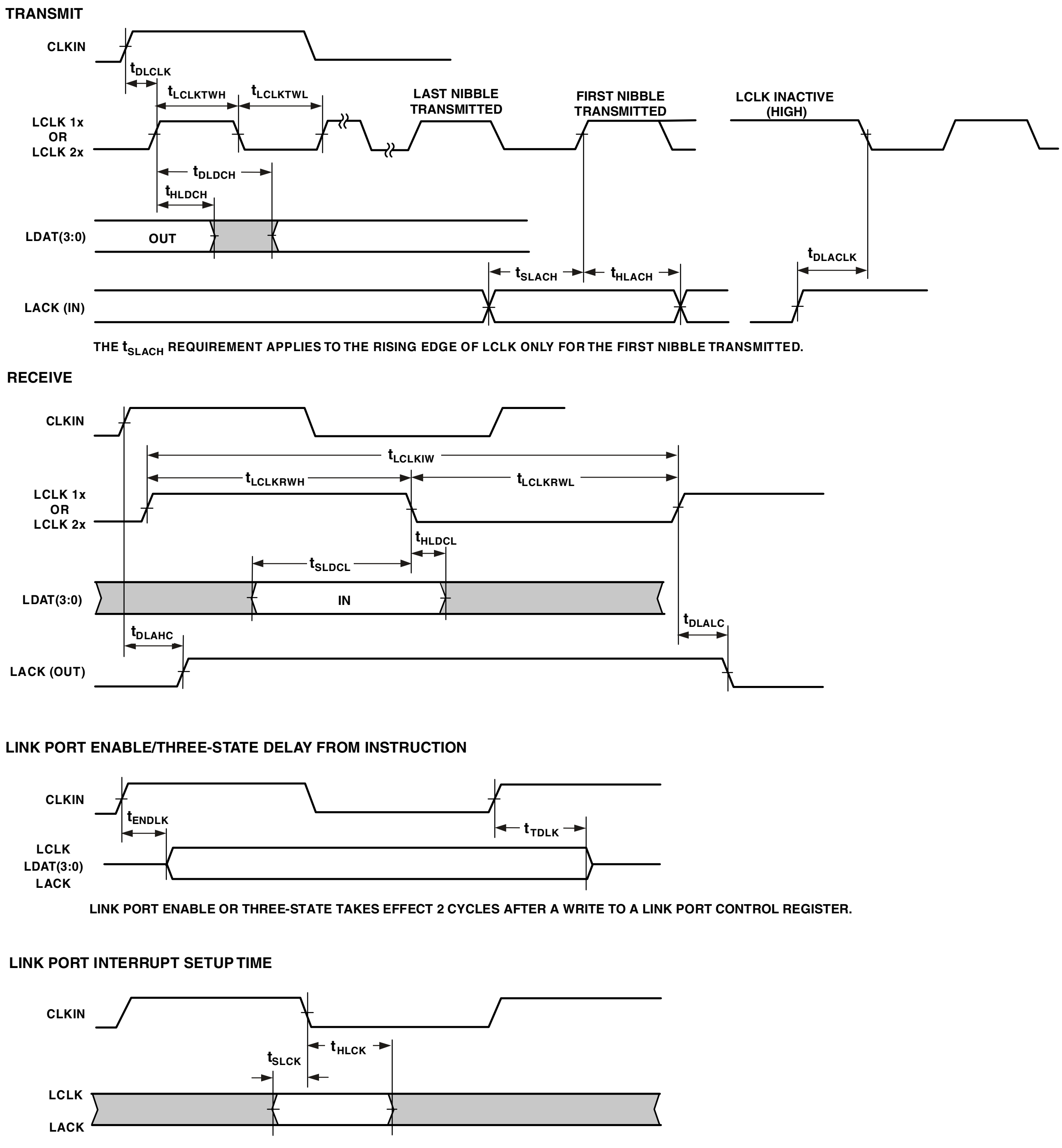

Figure 24. Link Ports—Receive

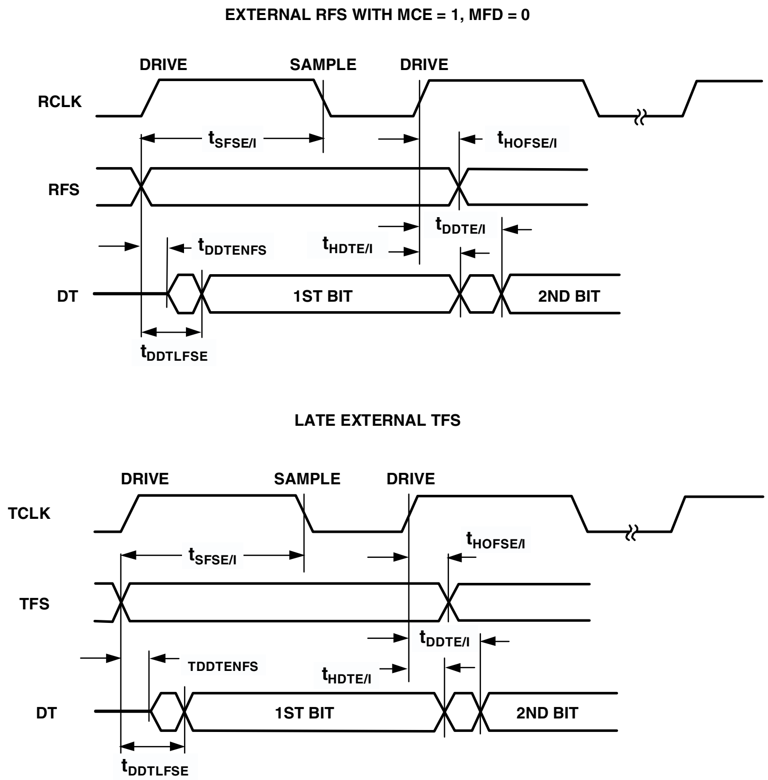

Figure 26. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see Table 36 and Figure 27.

Table 36. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1, 2]	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]		18.5	ns

[1] System Inputs = DATA63–0, ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ACK, $\overline{\text{SBTS}}$, $\overline{\text{HBR}}$, $\overline{\text{HBG}}$, $\overline{\text{CS}}$, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{BR6–1}}$, ID2–0, RPBA, $\overline{\text{IRQ2–0}}$, FLAG3–0, $\overline{\text{PA}}$, BRST, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{\text{BMS}}$, CLKIN, $\overline{\text{RESET}}$.

[2] For ADSP-21060L/ADSP-21060LC/ADSP-21062L, specification is 18.5 ns min.

[3] System Outputs = DATA63–0, ADDR31–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ACK, PAGE, CLKOUT, $\overline{\text{HBG}}$, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BR6–1}}$, $\overline{\text{PA}}$, BRST, $\overline{\text{CIF}}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, $\overline{\text{BMS}}$.

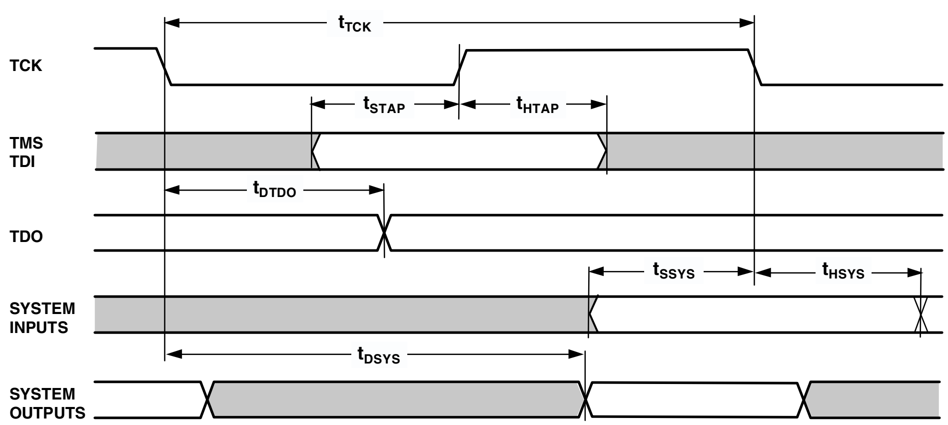

Figure 27. JTAG Test Access Port and Emulation

TEST CONDITIONS

For the ac signal specifications (timing parameters), see Timing Specifications on Page 21. These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 28.

Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

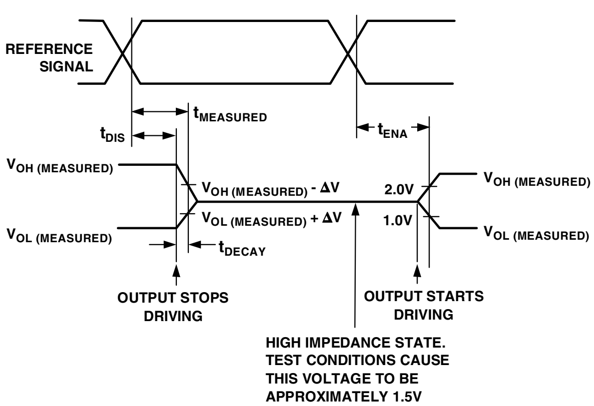

Figure 29. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 29). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 30). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 32, Figure 33, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 34 and Figure 36 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 32, Figure 33, Figure 37, and Figure 38 may not be linear outside the ranges shown.

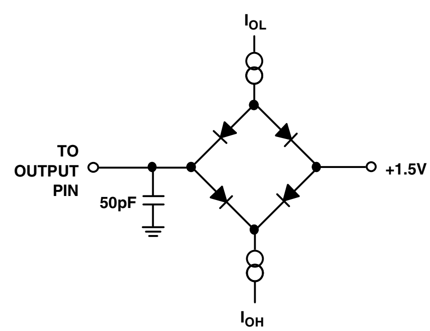

Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Output Drive Characteristics

Figure 31 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

Output Characteristics (5 V)

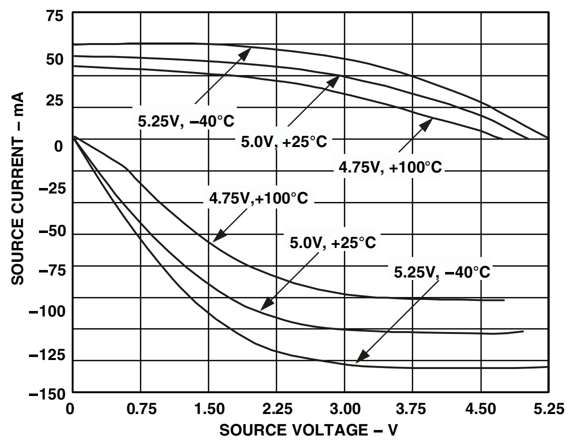

Figure 31. ADSP-21062 Typical Output Drive Currents (V_{DD} = 5 V)

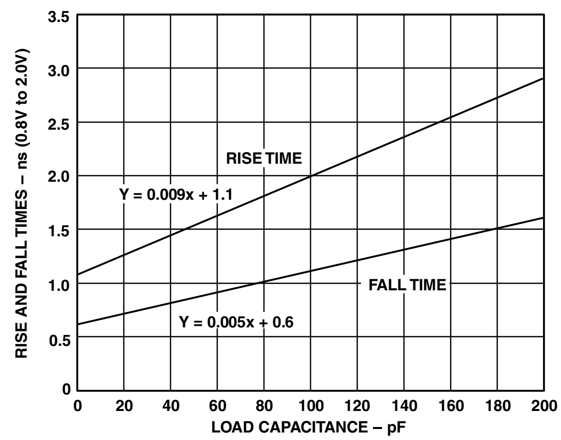

Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

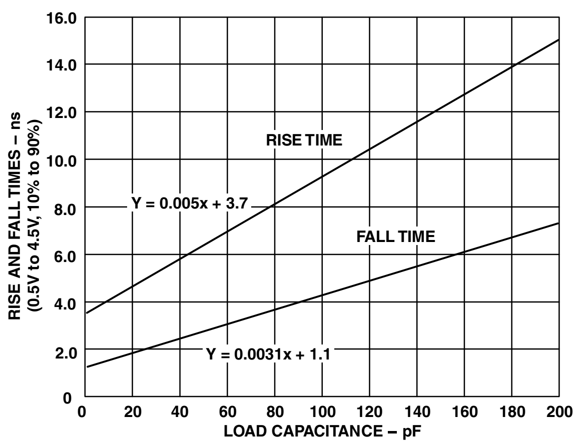

Figure 32. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

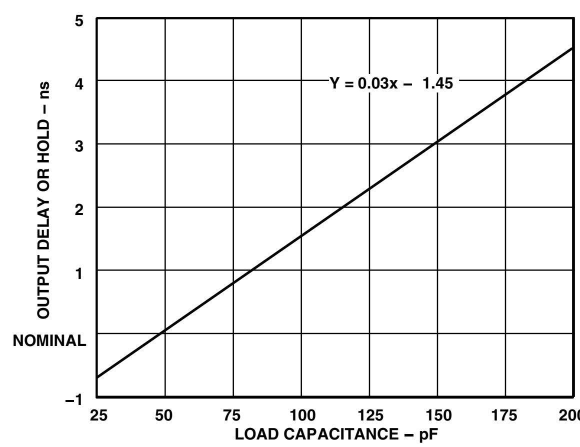

Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{\text{TRST}}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{\text{GND}}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{\text{EMU}}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{\text{HBG}}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{\text{CS}}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{\text{RD}}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{\text{MS3}}$	54	$\overline{\text{WR}}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{\text{MS2}}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{\text{MS1}}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{\text{MS0}}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{\text{SW}}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{\text{BMS}}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{\text{DMAG2}}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{\text{DMAG1}}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{\text{BR6}}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{\text{BR5}}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{\text{BR4}}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{\text{BR3}}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{\text{SBTS}}$	68	$\overline{\text{BR2}}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{\text{DMAR2}}$	69	$\overline{\text{BR1}}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{\text{DMAR1}}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{\text{HBR}}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{\text{RESET}}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{\text{IRQ2}}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{\text{IRQ1}}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{\text{IRQ0}}$	238
V_{DD}	39	$\overline{\text{CPA}}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

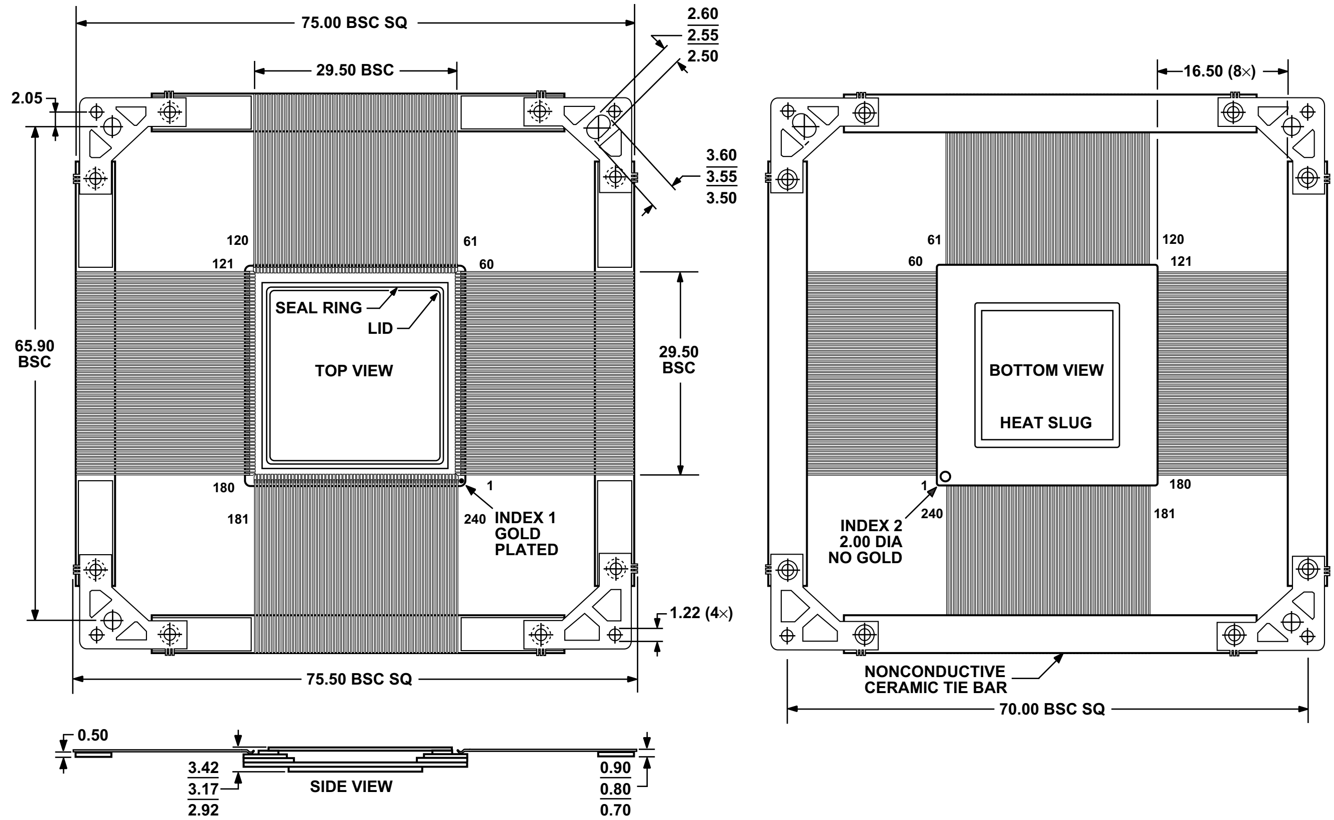

Figure 45. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Up [CQFP]
(QS-240-1B)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 43 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 43. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball Grid Array (PBGA)	Solder Mask Defined	0.63 mm diameter	0.76 mm diameter

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ASDP-21060CZ-133	1, 2	–40°C to +100°C	33 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Up]	QS-240-2A
ASDP-21060CZ-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Up]	QS-240-2A
ASDP-21060CW-133	1, 2	–40°C to +100°C	33 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ASDP-21060CW-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ADSP-21060KS-133		0°C to 85°C	33 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KSZ-133	2	0°C to 85°C	33 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KS-160		0°C to 85°C	40 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KSZ-160	2	0°C to 85°C	40 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KB-160		0°C to 85°C	40 MHz	4M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21060KBZ-160	2	0°C to 85°C	40 MHz	4M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21060LKSZ-133	2	0°C to 85°C	33 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKS-160		0°C to 85°C	40 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKSZ-160	2	0°C to 85°C	40 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKB-160		0°C to 85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LAB-160		–40°C to +85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LABZ-160	2	–40°C to +85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LCB-133		–40°C to +100°C	33 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LCBZ-133	2	–40°C to +100°C	33 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ASDP-21060LCW-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	3.3 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ADSP-21062KS-133		0°C to 85°C	33 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KSZ-133	2	0°C to 85°C	33 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KS-160		0°C to 85°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KSZ-160	2	0°C to 85°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KB-160		0°C to 85°C	40 MHz	2M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21062KBZ-160	2	0°C to 85°C	40 MHz	2M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21062CS-160		–40°C to +100°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062CSZ-160	2	–40°C to +100°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKSZ-133	2	0°C to 85°C	33 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKS-160		0°C to 85°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKSZ-160	2	0°C to 85°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKB-160		0°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LKBZ-160	2	0°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LAB-160		–40°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LABZ-160	2	–40°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LCS-160		–40°C to +100°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LCSZ-160	2	–40°C to +100°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2

[1] Model refers to package with formed leads. For model numbers of unformed lead versions (QS-240-1B, QS-240-2B), contact Analog Devices or an Analog Devices sales representative.

[2] RoHS compliant part.