**Welcome to E-XFL.COM**

## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Floating Point |
| Interface | Host Interface, Link Port, Serial Port |
| Clock Rate | 40MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 512kB |
| Voltage - I/O | 5.00V |
| Voltage - Core | 5.00V |
| Operating Temperature | 0°C ~ 85°C (TC) |
| Mounting Type | Surface Mount |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-MQFP-EP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-21060ksz-160 |

# CONTENTS

Summary ..... 1
General Description ..... 4
SHARC Family Core Architecture ..... 4
Memory and I/O Interface Features ..... 5
Development Tools ..... 8
Additional Information ..... 9
Related Signal Chains ..... 9
Pin Function Descriptions ..... 10
Target Board Connector for EZ-ICE Probe ..... 13
ADSP-21060/ADSP-21062 Specifications ..... 15
Operating Conditions (5 V) ..... 15
Electrical Characteristics (5 V) ..... 15
Internal Power Dissipation (5 V) ..... 16
External Power Dissipation (5 V) ..... 17
ADSP-21060L/ADSP-21062L Specifications ..... 18
Operating Conditions (3.3 V) ..... 18
Electrical Characteristics (3.3 V) ..... 18
Internal Power Dissipation (3.3 V) ..... 19
External Power Dissipation (3.3 V) ..... 20
Absolute Maximum Ratings ..... 20
ESD Caution ..... 21
Package Marking Information ..... 21
Timing Specifications ..... 21
Test Conditions ..... 48
Environmental Conditions ..... 51
225-Ball PBGA Ball Configuration ..... 52
240-Lead MQFP_PQ4/CQFP Pin Configuration ..... 54
Outline Dimensions ..... 56
Surface-Mount Design ..... 61
Ordering Guide ..... 62

## REVISION HISTORY

**3/13—Rev. G to Rev. H**

Updated Development Tools ..... 8

Corrected the power dissipation equation from $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$ to $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$
External Power Dissipation (3.3 V) ..... 20

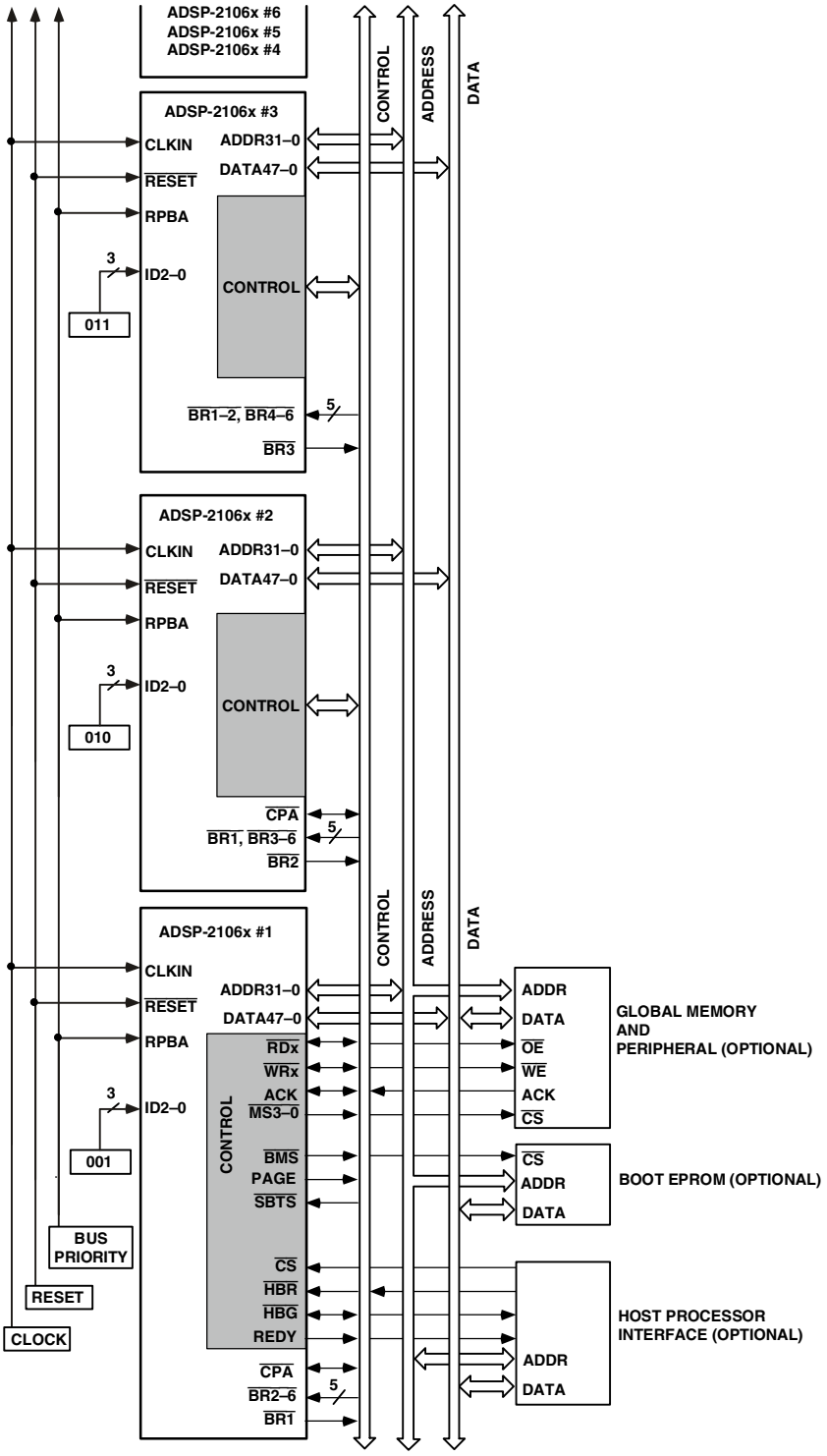



*Figure 3. Shared Memory Multiprocessing System*

### DMA Controller

The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-2106x's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

### Multiprocessing

The ADSP-2106x offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240M bytes/s over the link ports or external port. Broadcast writes allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

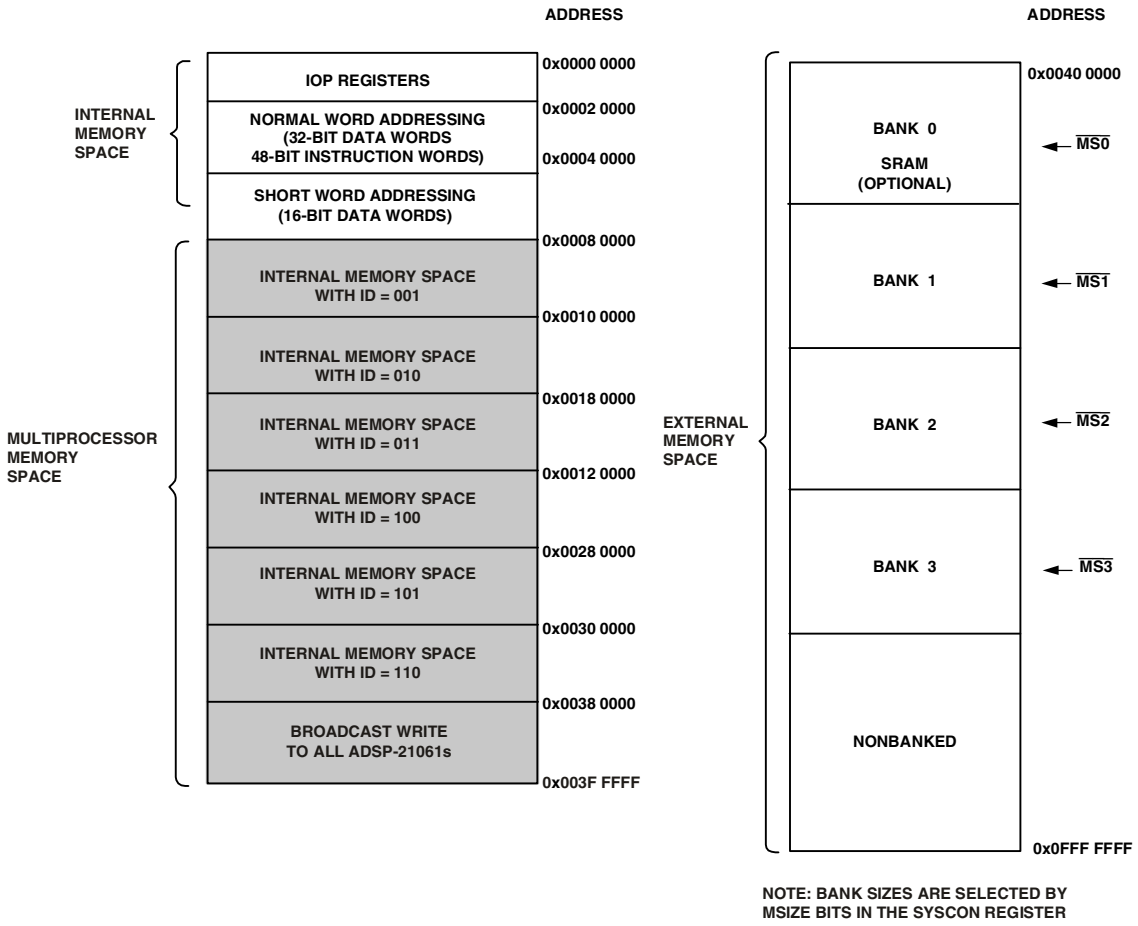



*Figure 4. Memory Map*

**Table 3. Pin Descriptions (Continued)**

| Pin | Type | Function |
|---|---|---|
| TFSx | I/O | **Transmit Frame Sync (Serial Ports 0, 1).** |
| RFSx | I/O | **Receive Frame Sync (Serial Ports 0, 1).** |
| LxDAT3–0 | I/O | **Link Port Data (Link Ports 0–5).** Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. |
| LxCLK | I/O | **Link Port Clock (Link Ports 0–5).** Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. |
| LxACK | I/O | **Link Port Acknowledge (Link Ports 0–5).** Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. |
| EBOOT | I | **EPROM Boot Select.** When EBOOT is high, the ADSP-2106x is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired. |
| LBOOT | I | **Link Boot.** When LBOOT is high, the ADSP-2106x is configured for link port booting. When LBOOT is low, the ADSP-2106x is configured for host processor booting or no booting. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired. |
| $\overline{\text{BMS}}$ | I/OT | **Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-2106x will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).<br>*EBOOT* *LBOOT* *$\overline{\text{BMS}}$* *Booting Mode*<br>1 0 Output EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)<br>0 0 1 (Input) Host Processor<br>0 1 1 (Input) Link Port<br>0 0 0 (Input) No Booting. Processor executes from external memory.<br>0 1 0 (Input) Reserved<br>1 1 x (Input) Reserved |
| CLKIN | I | **Clock In.** External clock input to the ADSP-2106x. The instruction cycle rate is equal to CLKIN. CLKIN should not be halted, changed, or operated below the minimum specified frequency. |
| $\overline{\text{RESET}}$ | I/A | **Processor Reset.** Resets the ADSP-2106x to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up. |
| TCK | I | **Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan. |
| TMS | I/S | **Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor. |
| TDI | I/S | **Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor. |
| TDO | O | **Test Data Output (JTAG).** Serial scan output of the boundary scan path. |
| $\overline{\text{TRST}}$ | I/A | **Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2106x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor. |
| $\overline{\text{EMU}}$ | O | **Emulation Status.** Must be connected to the ADSP-2106x EZ-ICE target board connector only. |
| ICSA | O | **Reserved,** leave unconnected. |
| VDD | P | **Power Supply;** nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices. (30 pins). |
| GND | G | **Power Supply Return.** (30 pins). |
| NC | | **Do Not Connect.** Reserved pins which must be left open and unconnected. |

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

# ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

## OPERATING CONDITIONS (3.3 V)

| Parameter | Description | A Grade Min | A Grade Max | C Grade Min | C Grade Max | K Grade Min | K Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.15 | 3.45 | 3.15 | 3.45 | 3.15 | 3.45 | V |
| $T_{CASE}$ | Case Operating Temperature | –40 | +85 | –40 | +100 | –40 | +85 | °C |
| $V_{IH}1$[1] | High Level Input Voltage @ $V_{DD}$ = Max | 2.0 | $V_{DD}$ + 0.5 | 2.0 | $V_{DD}$ + 0.5 | 2.0 | $V_{DD}$ + 0.5 | V |
| $V_{IH}2$[2] | High Level Input Voltage @ $V_{DD}$ = Max | 2.2 | $V_{DD}$ + 0.5 | 2.2 | $V_{DD}$ + 0.5 | 2.2 | $V_{DD}$ + 0.5 | V |
| $V_{IL}$[1, 2] | Low Level Input Voltage @ $V_{DD}$ = Min | –0.5 | +0.8 | –0.5 | +0.8 | –0.5 | +0.8 | V |

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

## ELECTRICAL CHARACTERISTICS (3.3 V)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$[1, 2] | High Level Output Voltage | @ $V_{DD}$ = Min, $I_{OH}$ = –2.0 mA | 2.4 | | V |
| $V_{OL}$[1, 2] | Low Level Output Voltage | @ $V_{DD}$ = Min, $I_{OL}$ = 4.0 mA | | 0.4 | V |
| $I_{IH}$[3, 4] | High Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 10 | µA |
| $I_{IL}$[3] | Low Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 10 | µA |
| $I_{ILP}$[4] | Low Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 150 | µA |
| $I_{OZH}$[5, 6, 7, 8] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 10 | µA |
| $I_{OZL}$[5, 9] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 10 | µA |
| $I_{OZHP}$[9] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 350 | µA |
| $I_{OZLC}$[7] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 1.5 | mA |
| $I_{OZLA}$[10] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 1.5 V | | 350 | µA |
| $I_{OZLAR}$[8] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 4.2 | mA |
| $I_{OZLS}$[6] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 150 | µA |
| $C_{IN}$[11, 12] | Input Capacitance | $f_{IN}$ = 1 MHz, $T_{CASE}$ = 25°C, $V_{IN}$ = 2.5 V | | 4.7 | pF |

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

## INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of $V_{DD}$ only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

| Operation | Peak Activity ($I_{DDINPEAK}$) | High Activity ($I_{DDINHIGH}$) | Low Activity ($I_{DDINLOW}$) |
|---|---|---|---|
| Instruction Type | Multifunction | Multifunction | Single Function |
| Instruction Fetch | Cache | Internal Memory | Internal Memory |
| Core memory Access | 2 Per Cycle (DM and PM) | 1 Per Cycle (DM) | None |
| Internal Memory DMA | 1 Per Cycle | 1 Per 2 Cycles | 1 Per 2 Cycles |

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

| Parameter | Test Conditions | Max | Unit |
|---|---|---|---|
| $I_{DDINPEAK}$ Supply Current (Internal)[1] | $t_{CK}$ = 30 ns, $V_{DD}$ = Max | 540 | mA |
| | $t_{CK}$ = 25 ns, $V_{DD}$ = Max | 600 | mA |
| $I_{DDINHIGH}$ Supply Current (Internal)[2] | $t_{CK}$ = 30 ns, $V_{DD}$ = Max | 425 | mA |
| | $t_{CK}$ = 25 ns, $V_{DD}$ = Max | 475 | mA |
| $I_{DDINLOW}$ Supply Current (Internal)[2] | $t_{CK}$ = 30 ns, $V_{DD}$ = Max | 250 | mA |
| | $t_{CK}$ = 25 ns, $V_{DD}$ = Max | 275 | mA |
| $I_{DDIDLE}$ Supply Current (Idle)[3] | $V_{DD}$ = Max | 180 | mA |

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106xL state during execution of IDLE instruction.

### *Clock Input*

**Table 9. Clock Input**

| Parameter | | ADSP-21060 ADSP-21062 40 MHz, 5 V Min | ADSP-21060 ADSP-21062 40 MHz, 5 V Max | ADSP-21060 ADSP-21062 33 MHz, 5 V Min | ADSP-21060 ADSP-21062 33 MHz, 5 V Max | ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Min | ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Max | ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Min | ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | | | |
| $t_{CK}$ | CLKIN Period | 25 | 100 | 30 | 100 | 25 | 100 | 30 | 100 | ns |
| $t_{CKL}$ | CLKIN Width Low | 7 | | 7 | | 8.75 | | 8.75[1] | | ns |
| $t_{CKH}$ | CLKIN Width High | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{CKRF}$ | CLKIN Rise/Fall (0.4 V to 2.0 V) | | 3 | | 3 | | 3 | | 3 | ns |

[1] For the ADSP-21060LC, this specification is 9.5 ns min.

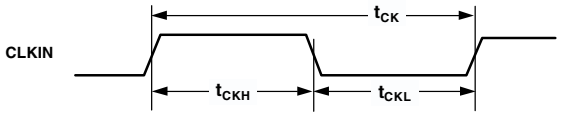



*Figure 9. Clock Input*

### *Reset*

**Table 10. Reset**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{WRST}$ | $\overline{\text{RESET}}$ Pulse Width Low[1] | $4t_{CK}$ | | ns |
| $t_{SRST}$ | $\overline{\text{RESET}}$ Setup Before CLKIN High[2] | 14 + DT/2 | $t_{CK}$ | ns |

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable $V_{DD}$ and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

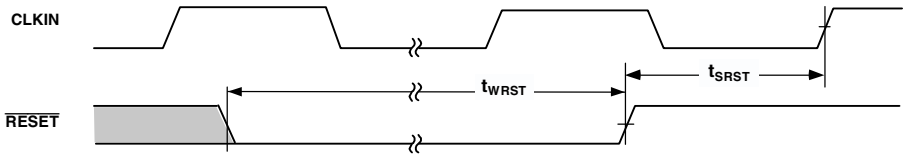



*Figure 10. Reset*

### *Interrupts*

**Table 11. Interrupts**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SIR}$ | $\overline{IRQ2–0}$ Setup Before CLKIN High[1] | 18 + 3DT/4 | | ns |
| $t_{HIR}$ | $\overline{IRQ2–0}$ Hold Before CLKIN High[1] | | 12 + 3DT/4 | ns |
| $t_{IPW}$ | $\overline{IRQ2–0}$ Pulse Width[2] | $2+t_{CK}$ | | ns |

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if $t_{SIR}$ and $t_{HIR}$ requirements are not met.

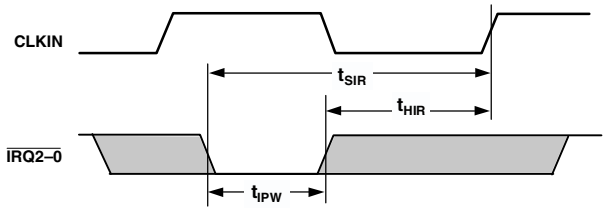



*Figure 11. Interrupts*

### *Timer*

**Table 12. Timer**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{DTEX}$ | CLKIN High to TIMEXP | | 15 | ns |

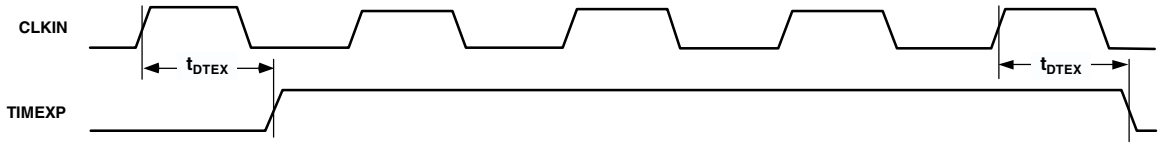



*Figure 12. Timer*

### *Flags*

**Table 13. Flags**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFI}$ | FLAG3–0 IN Setup Before CLKIN High[1] | 8 + 5DT/16 | | ns |
| $t_{HFI}$ | FLAG3–0 IN Hold After CLKIN High[1] | 0 – 5DT/16 | | ns |
| $t_{DWRFI}$ | FLAG3–0 IN Delay After $\overline{RD}/\overline{WR}$ Low[1] | | 5 + 7DT/16 | ns |
| $t_{HFIWR}$ | FLAG3–0 IN Hold After $\overline{RD}/\overline{WR}$ Deasserted[1] | 0 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFO}$ | FLAG3–0 OUT Delay After CLKIN High | | 16 | ns |
| $t_{HFO}$ | FLAG3–0 OUT Hold After CLKIN High | 4 | | ns |
| $t_{DFOE}$ | CLKIN High to FLAG3–0 OUT Enable | 3 | | ns |
| $t_{DFOD}$ | CLKIN High to FLAG3–0 OUT Disable | | 14 | ns |

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

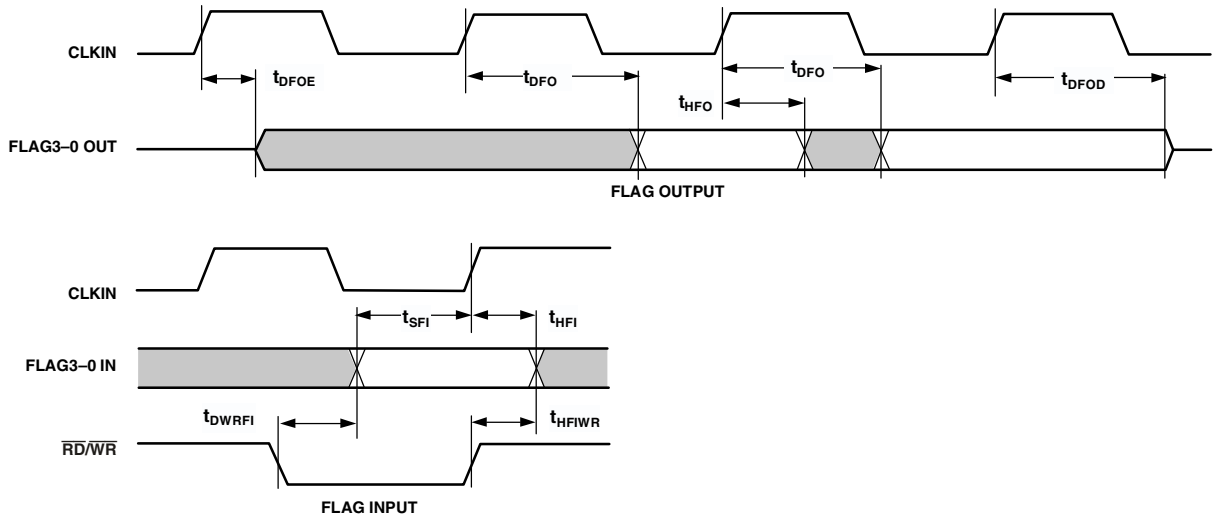



*Figure 13. Flags*

### *Memory Write—Bus Master*

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

**Table 15. Memory Write—Bus Master**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAAK}$ | ACK Delay from Address, Selects[1, 2] | | 14 + 7DT/8 + W | ns |
| $t_{DSAK}$ | ACK Delay from $\overline{WR}$ Low[1] | | 8 + DT/2 + W | ns |
| *Switching Characteristics* | | | | |
| $t_{DAWH}$ | Address Selects to $\overline{WR}$ Deasserted[2] | 17 + 15DT/16 + W | | ns |
| $t_{DAWL}$ | Address Selects to $\overline{WR}$ Low[2] | 3 + 3DT/8 | | ns |
| $t_{WW}$ | $\overline{WR}$ Pulse Width | 12 + 9DT/16 + W | | ns |
| $t_{DDWH}$ | Data Setup Before $\overline{WR}$ High | 7 + DT/2 + W | | ns |
| $t_{DWHA}$ | Address Hold After $\overline{WR}$ Deasserted | 0.5 + DT/16 + H | | ns |
| $t_{DATRWH}$ | Data Disable After $\overline{WR}$ Deasserted[3] | 1 + DT/16 + H | 6 + DT/16 + H | ns |
| $t_{WWR}$ | $\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low | 8 + 7DT/16 + H | | ns |
| $t_{DDWR}$ | Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low | 5 + 3DT/8 + I | | ns |
| $t_{WDE}$ | $\overline{WR}$ Low to Data Enabled | –1 + DT/16 | | ns |
| $t_{SADADC}$ | Address, Selects Setup Before ADRCLK High[2] | 0 + DT/4 | | ns |

W = (number of wait states specified in WAIT register) × $t_{CK}$.
H = $t_{CK}$ (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = $t_{CK}$ (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = $t_{CK}$ (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by $t_{DAAK}$ or $t_{DSAK}$ or synchronous specification $t_{SACKC}$ for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications $t_{SACKC}$ and $t_{HACK}$ must be met for wait state modes external, either, or both (both, after internal wait states have completed).

[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

### *Synchronous Read/Write—Bus Master*

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 30). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

**Table 16. Synchronous Read/Write—Bus Master**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSDATI}$ | Data Setup Before CLKIN | 3 + DT/8 | | ns |
| $t_{HSDATI}$ | Data Hold After CLKIN | 3.5 – DT/8 | | ns |
| $t_{DAAK}$ | ACK Delay After Address, Selects[1, 2] | | 14 + 7DT/8 + W | ns |
| $t_{SACKC}$ | ACK Setup Before CLKIN[2] | 6.5 + DT/4 | | ns |
| $t_{HACK}$ | ACK Hold After CLKIN | –1 – DT/4 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DADRO}$ | Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1] | | 7 – DT/8 | ns |
| $t_{HADRO}$ | Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN | –1 – DT/8 | | ns |
| $t_{DPGC}$ | PAGE Delay After CLKIN | 9 + DT/8 | 16 + DT/8 | ns |
| $t_{DRDO}$ | $\overline{RD}$ High Delay After CLKIN | –2 – DT/8 | 4 – DT/8 | ns |
| $t_{DWRO}$ | $\overline{WR}$ High Delay After CLKIN | –3 – 3DT/16 | 4 – 3DT/16 | ns |
| $t_{DRWL}$ | $\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN | 8 + DT/4 | 12.5 + DT/4 | ns |
| $t_{SDDATO}$ | Data Delay After CLKIN | | 19 + 5DT/16 | ns |
| $t_{DATTR}$ | Data Disable After CLKIN[3] | 0 – DT/8 | 7 – DT/8 | ns |
| $t_{DADCCK}$ | ADRCLK Delay After CLKIN | 4 + DT/8 | 10 + DT/8 | ns |
| $t_{ADRCK}$ | ADRCLK Period | $t_{CK}$ | | ns |
| $t_{ADRCKH}$ | ADRCLK Width High | ($t_{CK}$/2 – 2) | | ns |
| $t_{ADRCKL}$ | ADRCLK Width Low | ($t_{CK}$/2 – 2) | | ns |

[1] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[2] ACK delay/setup: user must meet $t_{DAAK}$ or $t_{DSAK}$ or synchronous specification $t_{SAKC}$ for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

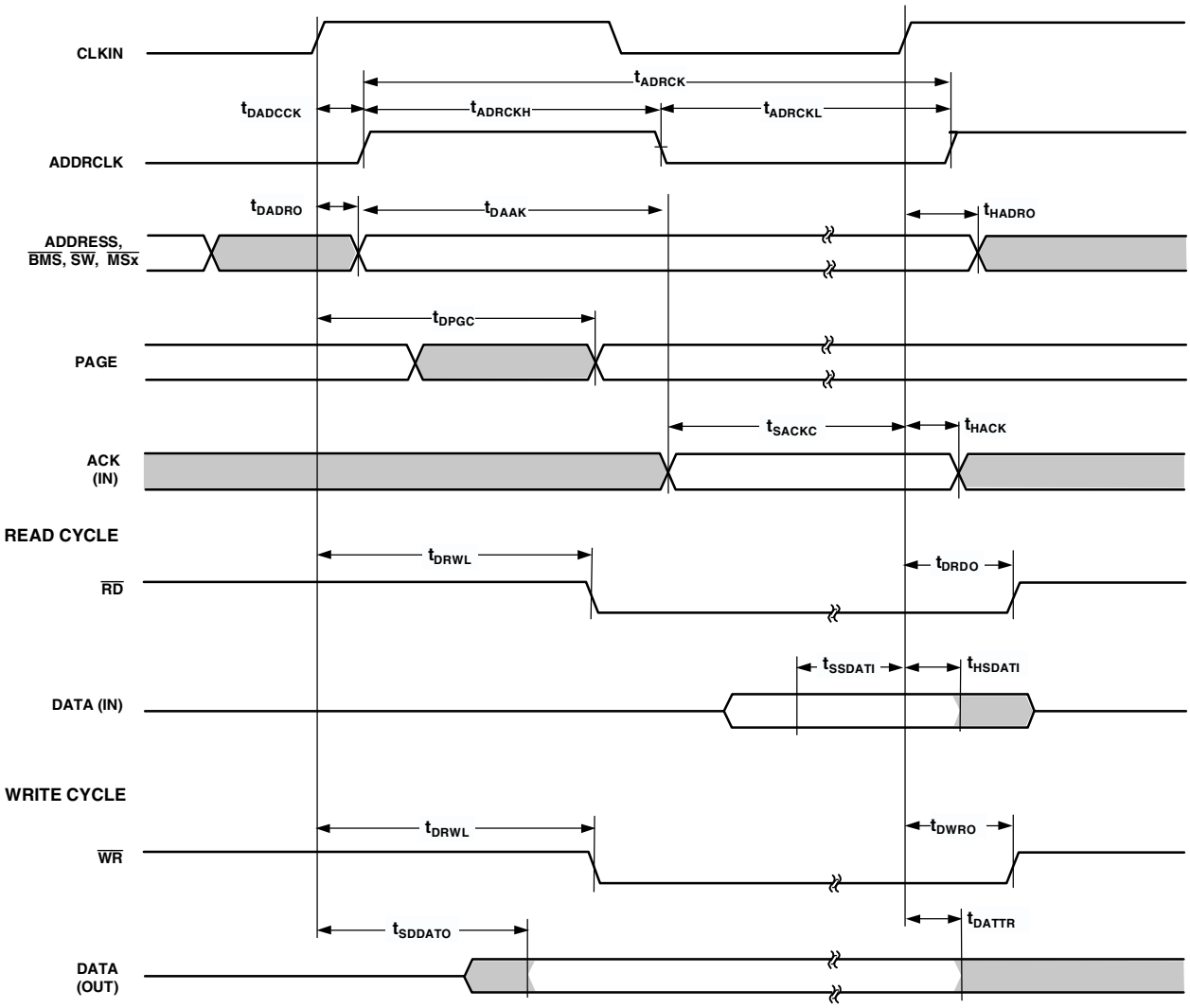



*Figure 16. Synchronous Read/Write—Bus Master*

### *Asynchronous Read/Write—Host to ADSP-2106x*

Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-2106x, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-2106x's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Not required if and address are valid $t_{HBGRCSV}$ after goes low. For first access after asserted, ADDR31–0 must be a non-MMS value 1/2 $t_{CLK}$ before or goes low or by $t_{HBGRCSV}$ after goes low. This is easily accomplished by driving an upper address signal high when is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual*, Revision 2.1.

**Table 19. Read Cycle**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SADRDL}$ | Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1] | 0 | | ns |
| $t_{HADRDH}$ | Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$ | 0 | | ns |
| $t_{WRWH}$ | $\overline{RD}$/$\overline{WR}$ High Width | 6 | | ns |
| $t_{DRDHRDY}$ | $\overline{RD}$ High Delay After REDY (O/D) Disable | 0 | | ns |
| $t_{DRDHRDY}$ | $\overline{RD}$ High Delay After REDY (A/D) Disable | 0 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SDATRDY}$ | Data Valid Before REDY Disable from Low | 2 | | ns |
| $t_{DRDYRDL}$ | REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low[2] | | 10 | ns |
| $t_{RDYPRD}$ | REDY (O/D) or (A/D) Low Pulse Width for Read | 45 + 21DT/16 | | ns |
| $t_{HDARWH}$ | Data Disable After $\overline{RD}$ High[3] | 2 | 8 | ns |

[1] Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2 $t_{CLK}$ before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual,* Revision 2.1.

[2] For ADSP-21060L, specification is 10.5 ns max; for ADSP-21060LC, specification is 12.5 ns max.

[3] For ADSP-21060L/ADSP-21060LC, specification is 2 ns min, 8.5 ns max.

**Table 20. Write Cycle**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SCSWRL}$ | $\overline{CS}$ Low Setup Before $\overline{WR}$ Low | 0 | | ns |
| $t_{HCSWRH}$ | $\overline{CS}$ Low Hold After $\overline{WR}$ High | 0 | | ns |
| $t_{SADWRH}$ | Address Setup Before $\overline{WR}$ High | 5 | | ns |
| $t_{HADWRH}$ | Address Hold After $\overline{WR}$ High | 2 | | ns |
| $t_{WWRL}$ | $\overline{WR}$ Low Width | 7 | | ns |
| $t_{WRWH}$ | $\overline{RD}$/$\overline{WR}$ High Width | 6 | | ns |
| $t_{DWRHRDY}$ | $\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable | 0 | | ns |
| $t_{SDATWH}$ | Data Setup Before $\overline{WR}$ High | 5 | | ns |
| $t_{HDATWH}$ | Data Hold After $\overline{WR}$ High | 1 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DRDYWRL}$ | REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low | | 10 | ns |
| $t_{RDYPWR}$ | REDY (O/D) or (A/D) Low Pulse Width for Write | 15 + 7DT/16 | | ns |
| $t_{SRDYCK}$ | REDY (O/D) or (A/D) Disable to CLKIN | 1 + 7DT/16 | 8 + 7DT/16 | ns |

### *DMA Handshake*

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, PAGE, DATA63–0, and ACK also apply.

**Table 22. DMA Handshake**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SDRLC}$ | $\overline{\text{DMARx}}$ Low Setup Before CLKIN[1] | 5 | | ns |
| $t_{SDRHC}$ | $\overline{\text{DMARx}}$ High Setup Before CLKIN[1] | 5 | | ns |
| $t_{WDR}$ | $\overline{\text{DMARx}}$ Width Low (Nonsynchronous) | 6 | | ns |
| $t_{SDATDGL}$ | Data Setup After $\overline{\text{DMAGx}}$ Low[2] | | 10 + 5DT/8 | ns |
| $t_{HDATIDG}$ | Data Hold After $\overline{\text{DMAGx}}$ High | 2 | | ns |
| $t_{DATDRH}$ | Data Valid After $\overline{\text{DMARx}}$ High[2] | | 16 + 7DT/8 | ns |
| $t_{DMARLL}$ | $\overline{\text{DMARx}}$ Low Edge to Low Edge | 23 + 7DT/8 | | ns |
| $t_{DMARH}$ | $\overline{\text{DMARx}}$ Width High[2] | 6 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DDGL}$ | $\overline{\text{DMAGx}}$ Low Delay After CLKIN | 9 + DT/4 | 15 + DT/4 | ns |
| $t_{WDGH}$ | $\overline{\text{DMAGx}}$ High Width | 6 + 3DT/8 | | ns |
| $t_{WDGL}$ | $\overline{\text{DMAGx}}$ Low Width | 12 + 5DT/8 | | ns |
| $t_{HDGC}$ | $\overline{\text{DMAGx}}$ High Delay After CLKIN | –2 – DT/8 | 6 – DT/8 | ns |
| $t_{VDATDGH}$ | Data Valid Before $\overline{\text{DMAGx}}$ High[3] | 8 + 9DT/16 | | ns |
| $t_{DATRDGH}$ | Data Disable After $\overline{\text{DMAGx}}$ High[4] | 0 | 7 | ns |
| $t_{DGWRL}$ | $\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low[5] | 0 | 2 | ns |
| $t_{DGWRH}$ | $\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High | 10 + 5DT/8 + W | | ns |
| $t_{DGWRR}$ | $\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High | 1 + DT/16 | 3 + DT/16 | ns |
| $t_{DGRDL}$ | $\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low | 0 | 2 | ns |
| $t_{DRDGH}$ | $\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High | 11 + 9DT/16 + W | | ns |
| $t_{DGRDR}$ | $\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High | 0 | 3 | ns |
| $t_{DGWR}$ | $\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low | 5 + 3DT/8 + HI | | ns |
| $t_{DADGH}$ | Address/Select Valid to $\overline{\text{DMAGx}}$ High | 17 + DT | | ns |
| $t_{DDGHA}$ | Address/Select Hold After $\overline{\text{DMAGx}}$ High[6] | –0.5 | | ns |

W = (number of wait states specified in WAIT register) × $t_{CK}$.
HI = $t_{CK}$ (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven $t_{DATDRH}$ after $\overline{\text{DMARx}}$ is brought high.
[3] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - 0.25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] For ADSP-21062/ADSP-21062L specification is –2.5 ns min, 2 ns max.
[6] For ADSP-21060L/ADSP-21062L specification is –1 ns min.

**Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLCK}$ | LACK/LCLK Setup Before CLKIN Low[1] | 10 | | 10 | | ns |
| $t_{HLCK}$ | LACK/LCLK Hold After CLKIN Low[1] | 2 | | 2 | | ns |

[1] Only required for interrupt recognition in the current cycle.

### *Link Ports —2 × CLK Speed Operation*

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$Setup\ Skew = t_{LCLKTWH}\ \text{min} - t_{DLDCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$Hold\ Skew = t_{LCLKTWL}\ \text{min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

Note that link port transfers at 2× CLK speed at 40 MHz ($t_{CK}$ = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz ($t_{CK}$ = 30 ns) work as specified.

**Table 26. Link Ports—Receive**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLDCL}$ | Data Setup Before LCLK Low | 2.5 | | 2.25 | | ns |
| $t_{HLDCL}$ | Data Hold After LCLK Low | 2.25 | | 2.25 | | ns |
| $t_{LCLKIW}$ | LCLK Period (2× Operation) | $t_{CK}/2$ | | $t_{CK}/2$ | | ns |
| $t_{LCLKRWL}$ | LCLK Width Low[1] | 4.5 | | 5.25 | | ns |
| $t_{LCLKRWH}$ | LCLK Width High[2] | 4.25 | | 4 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DLAHC}$ | LACK High Delay After CLKIN High[3] | 18 + DT/2 | 28.5 + DT/2 | 18 + DT/2 | 29.5 + DT/2 | ns |
| $t_{DLALC}$ | LACK Low Delay After LCLK High[4] | 6 | 16 | 6 | 16 | ns |

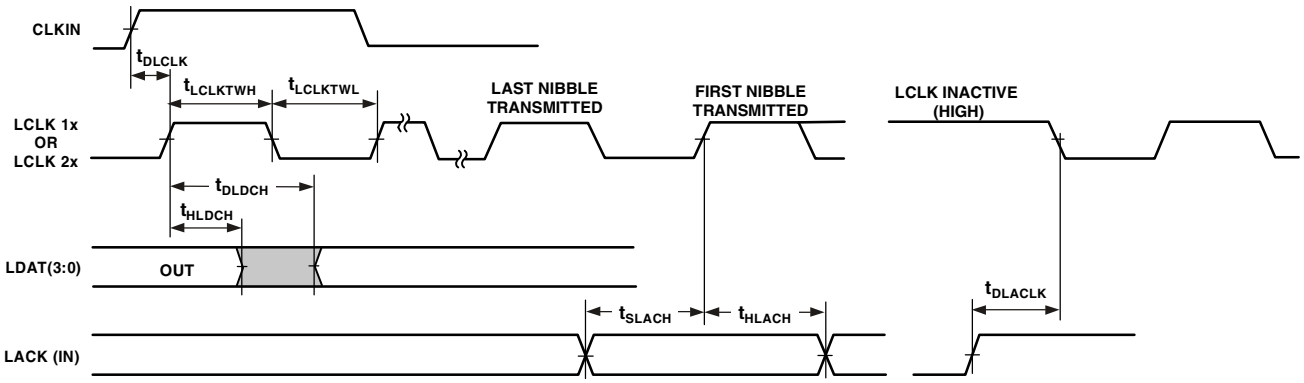
[1] For ADSP-21060L, specification is 5 ns min.
[2] For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.
[3] LACK goes low with $t_{DLALC}$ relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[4] For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

**Table 27. Link Ports—Transmit**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLACH}$ | LACK Setup Before LCLK High | 19 | | 19 | | ns |
| $t_{HLACH}$ | LACK Hold After LCLK High | –6.75 | | –6.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DLCLK}$ | Data Delay After CLKIN | | 8 | | 8 | ns |
| $t_{DLDCH}$ | Data Delay After LCLK High[1] | | 2.25 | | 2.25 | ns |
| $t_{HLDCH}$ | Data Hold After LCLK High[2] | –2.0 | | –2 | | ns |
| $t_{LCLKTWL}$ | LCLK Width Low[3] | $(t_{CK}/4) - 1$ | $(t_{CK}/4) + 1.25$ | $(t_{CK}/4) - 0.75$ | $(t_{CK}/4) + 1.5$ | ns |
| $t_{LCLKTWH}$ | LCLK Width High[4] | $(t_{CK}/4) - 1.25$ | $(t_{CK}/4) + 1$ | $(t_{CK}/4) - 1.5$ | $(t_{CK}/4) + 1$ | ns |
| $t_{DLACLK}$ | LCLK Low Delay After LACK High | $(t_{CK}/4) + 9$ | $(3 \times t_{CK}/4) + 16.5$ | $(t_{CK}/4) + 9$ | $(3 \times t_{CK}/4) + 16.5$ | ns |

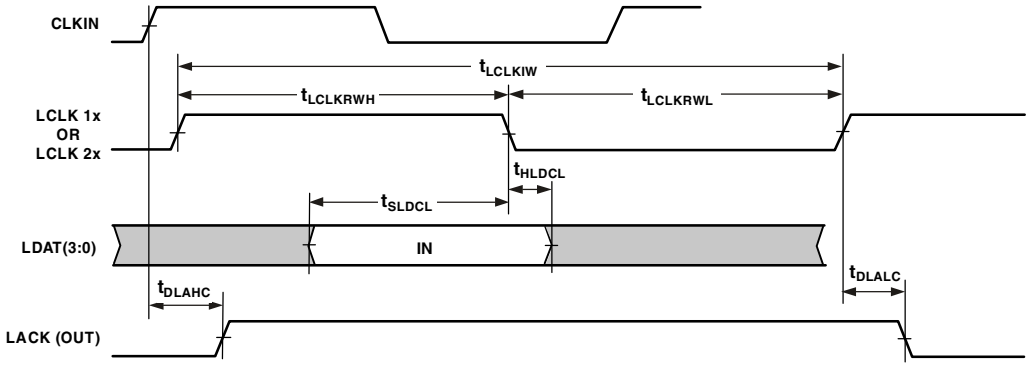
[1] For ADSP-21060/ADSP-21060C, specification is 2.5 ns max.
[2] For ADSP-21062L, specification is –2.25 ns min.
[3] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C/ADSP-21062L, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1.5$ ns max.
[4] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C, specification is $(t_{CK}/4) - 1.5$ ns min, $(t_{CK}/4) + 1$ ns max.

**TRANSMIT**

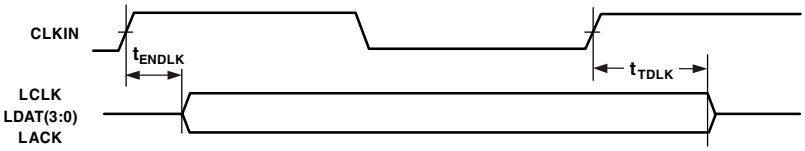



THE $t_{SLACH}$ REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

**RECEIVE**




**LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION**




LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

**LINK PORT INTERRUPT SETUP TIME**

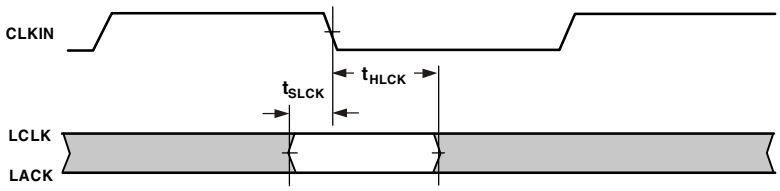



*Figure 24. Link Ports—Receive*

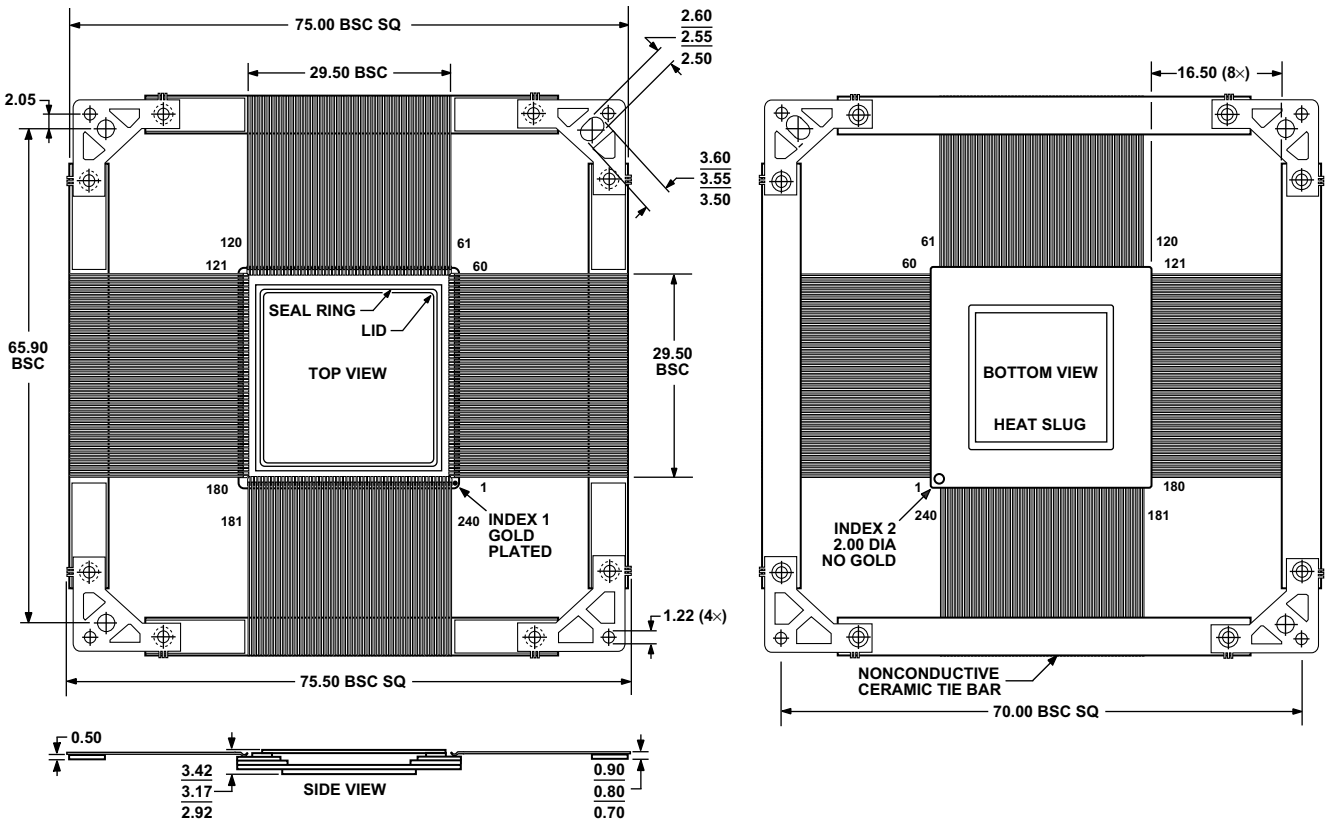



*Figure 45. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Up [CQFP]*
*(QS-240-1B)*
*Dimensions shown in millimeters*

## SURFACE-MOUNT DESIGN

Table 43 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

**Table 43. BGA Data for Use with Surface-Mount Design**

| Package | Ball Attach Type | Solder Mask Opening | Ball Pad Size |
|---|---|---|---|
| 225-Ball Grid Array (PBGA) | Solder Mask Defined | 0.63 mm diameter | 0.76 mm diameter |

## ORDERING GUIDE

| Model | Notes | Temperature Range | Instruction Rate | On-Chip SRAM | Operating Voltage | Package Description | Package Option |
|---|---|---|---|---|---|---|---|
| ASDP-21060CZ-133 | 1, 2 | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CZ-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CW-133 | 1, 2 | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ASDP-21060CW-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21060KS-133 | | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-133 | 2 | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060KBZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LKSZ-133 | 2 | 0°C to 85°C | 33 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKSZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LAB-160 | | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LABZ-160 | 2 | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCB-133 | | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCBZ-133 | 2 | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ASDP-21060LCW-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21062KS-133 | | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-133 | 2 | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062KBZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062CS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062CSZ-160 | 2 | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-133 | 2 | 0°C to 85°C | 33 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LKBZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LAB-160 | | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LABZ-160 | 2 | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LCS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LCSZ-160 | 2 | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |

[1] Model refers to package with formed leads. For model numbers of unformed lead versions (QS-240-1B, QS-240-2B), contact Analog Devices or an Analog Devices sales representative.
[2] RoHS compliant part.