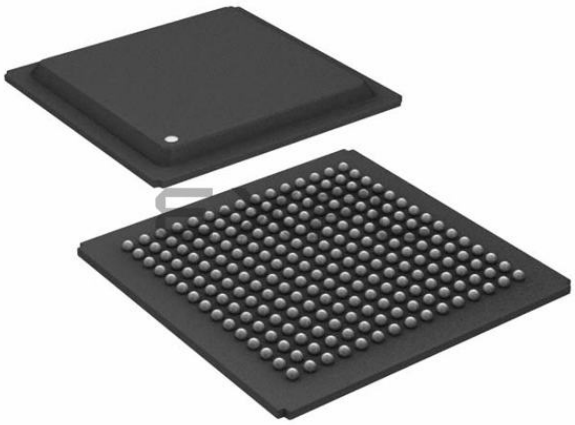

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	33MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	225-BBGA
Supplier Device Package	225-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21060lcb-133

Table 3. Pin Descriptions (Continued)

Pin	Type	Function
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-2106x deasserts ACK as an output to add waitstates to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-2106x deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-2106x attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-2106x deadlock, or used with a DRAM controller.
$\overline{\text{IRQ2–0}}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
FLAG3–0	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** This pin must be asserted by a host processor to request control of the ADSP-2106x's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-2106x places the address, data, select and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-2106x bus requests $\overline{\text{BR6–1}}$ in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges a bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-2106x until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-2106x bus master and is monitored by all others.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-2106x.
REDY	O (O/D)	**Host Bus Acknowledge.** The ADSP-2106x deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR2–1}}$	I/A	**DMA Request 1** (DMA Channel 7) and **DMA Request 2** (DMA Channel 8).
$\overline{\text{DMAG2–1}}$	O/T	**DMA Grant 1** (DMA Channel 7) and **DMA Grant 2** (DMA Channel 8).
$\overline{\text{BR6–1}}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-2106xs to arbitrate for bus master-ship. An ADSP-2106x only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-2106xs, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
$\overline{\text{ID2–0}}$	O (O/D)	**Multiprocessing ID.** Determines which multiprocessing bus request ($\overline{\text{BR1}}$– $\overline{\text{BR6}}$) is used by ADSP-2106x. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, etc. ID = 000 in single-processor systems. These lines are a system configuration selection that should be hardwired or changed at reset only.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x.
$\overline{\text{CPA}}$	I/O (O/D)	**Core Priority Access.** Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open drain output that is connected to all ADSP-2106xs in the system. The $\overline{\text{CPA}}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTx	O	**Data Transmit (Serial Ports 0, 1).** Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	**Data Receive (Serial Ports 0, 1).** Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50 kΩ internal pull-up resistor.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

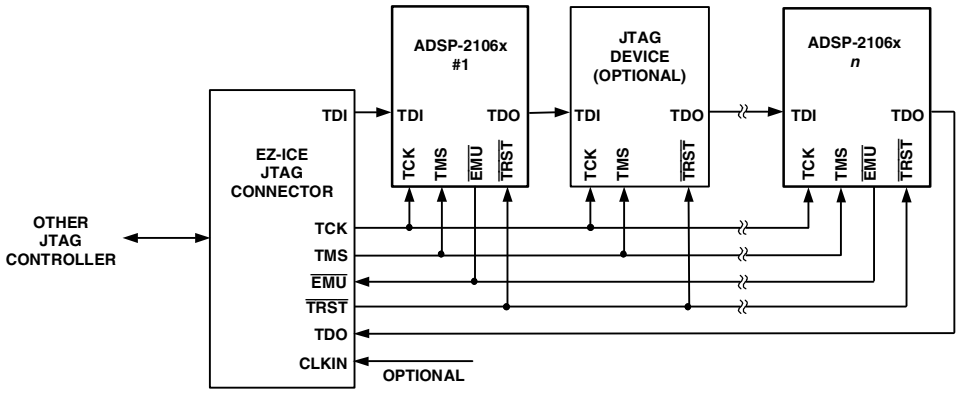


Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

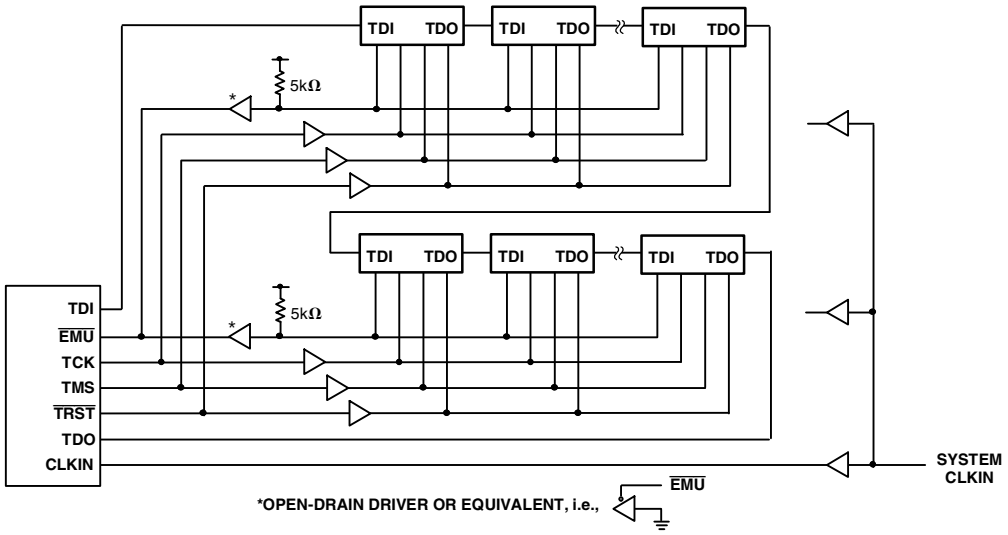


Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where% is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	745	mA
	t_{CK} = 25 ns, V_{DD} = Max	850	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	575	mA
	t_{CK} = 25 ns, V_{DD} = Max	670	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	340	mA
	t_{CK} = 25 ns, V_{DD} = Max	390	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	200	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106x state during execution of IDLE instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 6. External Power Calculations (3.3 V Devices)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W
						P_{EXT} = 0.074 W

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed Table 7 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	ADSP-21060/ADSP-21060C ADSP-21062 5 V	ADSP-21060L/ADSP-21060LC ADSP-21062L 3.3 V
Supply Voltage (V_{DD})	–0.3 V to +7.0 V	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF	200 pF
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C
Lead Temperature (5 seconds)	280°C	280°C
Junction Temperature Under Bias	130°C	130°C

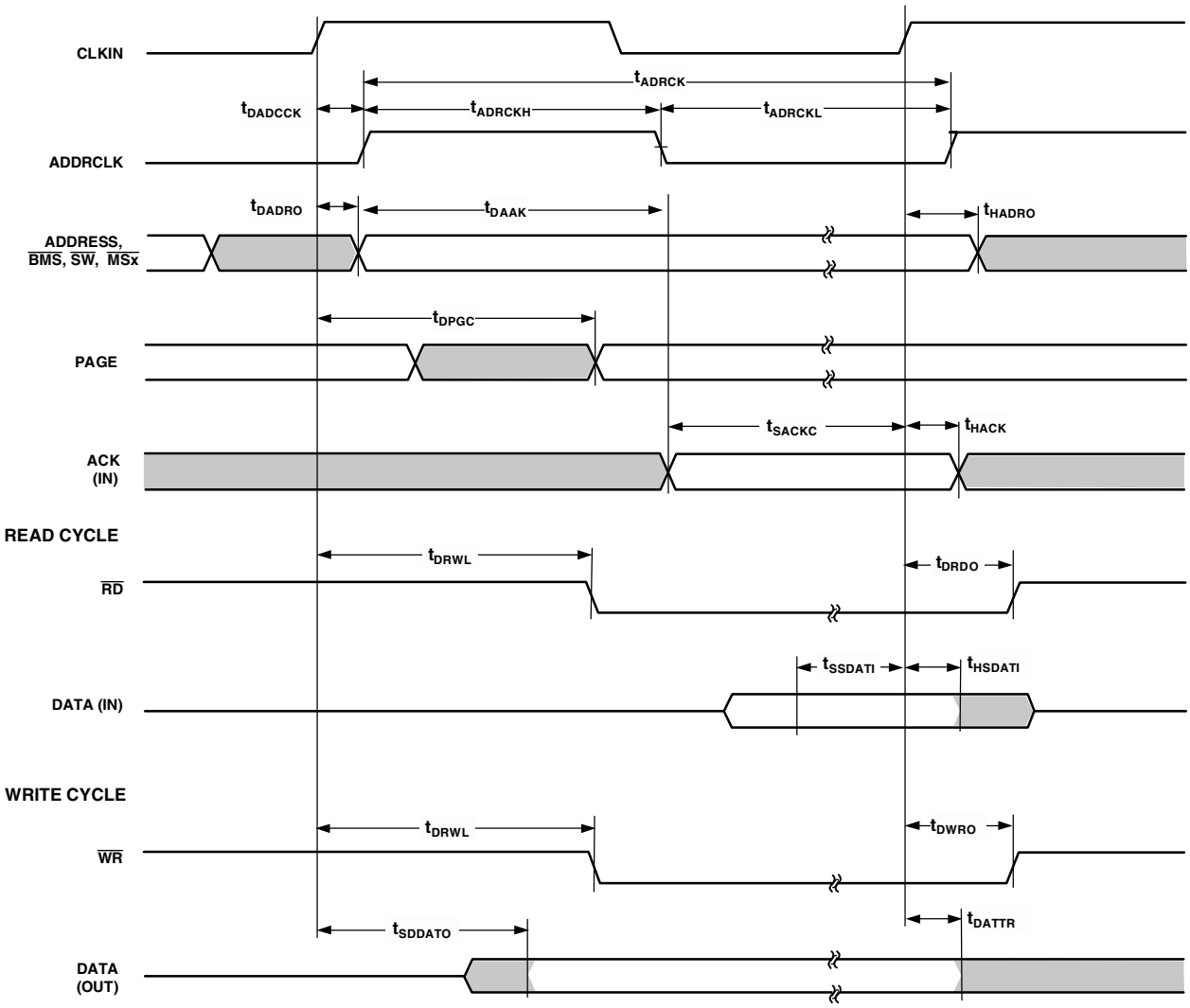


Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet the bus slave timing requirements.

Table 17. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	15 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}$/$\overline{WR}$ Low Setup Before CLKIN[1]	9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}$/$\overline{WR}$ Low Hold After CLKIN[2]	–4 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}$/$\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN[3]		18 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[5]		9	ns
t_{ACKTR}	ACK Disable After CLKIN[5]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.
[2] For ADSP-21060C specification is –3.5 – 5DT/16 ns min, 8 + 7DT/16 ns max; for ADSP-21060LC specification is –3.75 – 5DT/16 ns min, 8 + 7DT/16 ns max.
[3] For ADSP-21062/ADSP-21062L/ADSP-21060C specification is 19 + 5DT/16 ns max; for ADSP-21060LC specification is 19.25 + 5DT/16 ns max.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

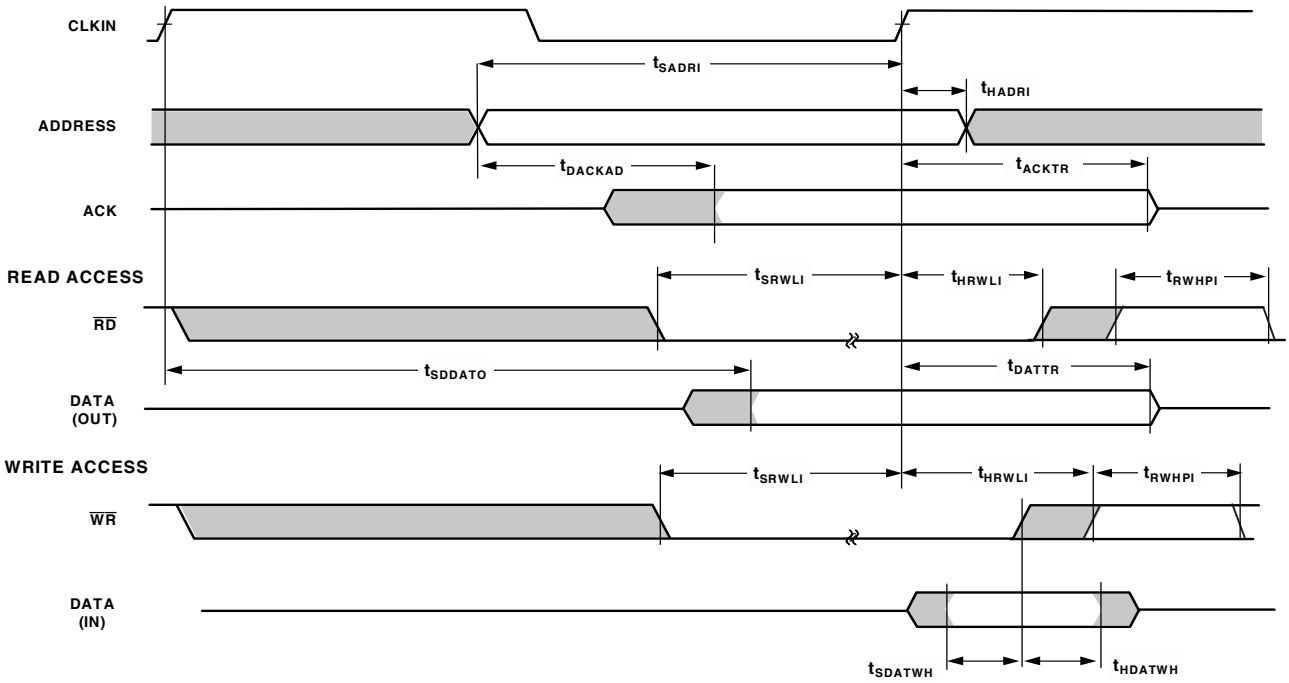


Figure 17. Synchronous Read/Write—Bus Slave

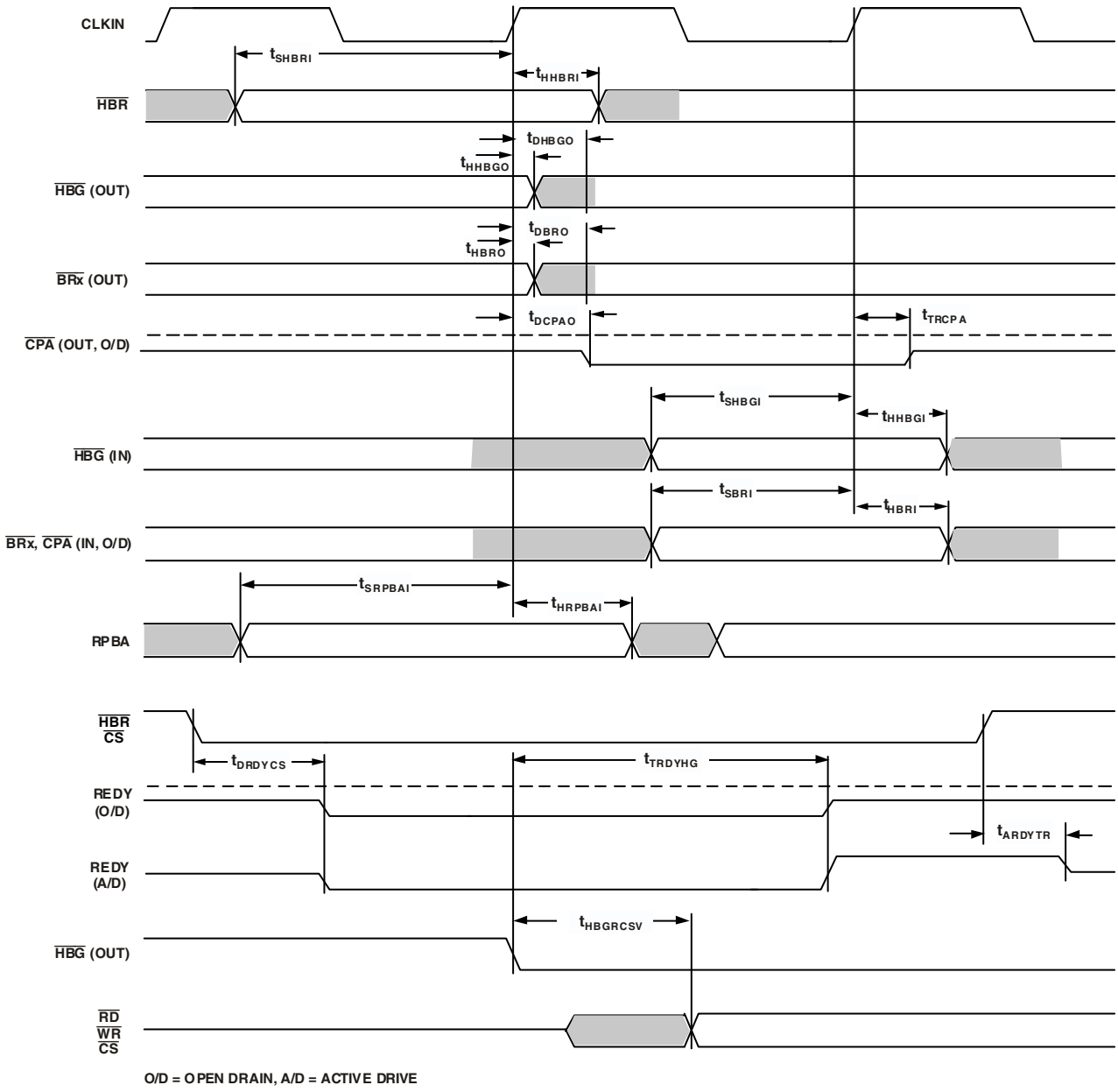


Figure 18. Multiprocessor Bus Request and Host Bus Request

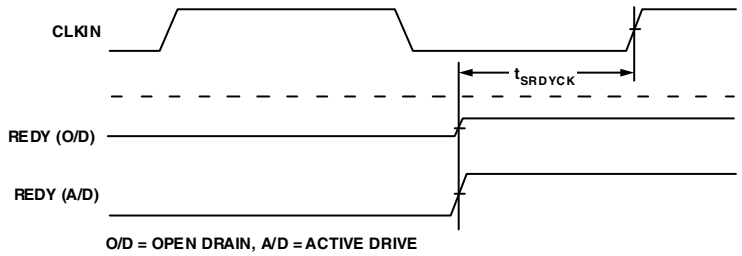


Figure 19. Synchronous REDY Timing

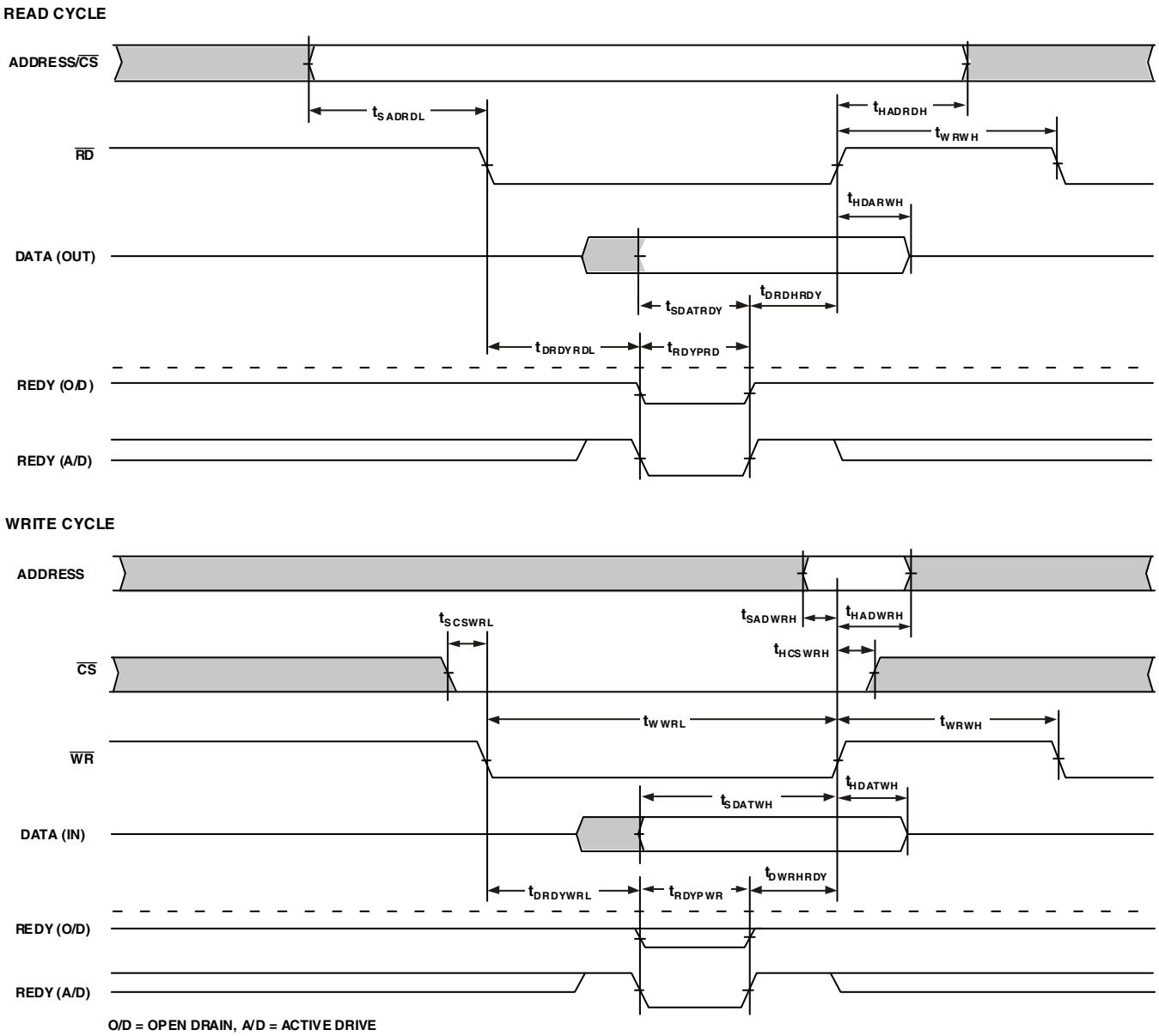


Figure 20. Asynchronous Read/Write—Host to ADSP-2106x

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, PAGE, DATA63–0, and ACK also apply.

Table 22. DMA Handshake

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SDRLC}	$\overline{\text{DMARx}}$ Low Setup Before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMARx}}$ High Setup Before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High[2]	6		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[3]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[4]	0	7	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low[5]	0	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High	0	3	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low	5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	17 + DT		ns
t_{DDGHA}	Address/Select Hold After $\overline{\text{DMAGx}}$ High[6]	–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[3] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - 0.25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] For ADSP-21062/ADSP-21062L specification is –2.5 ns min, 2 ns max.
[6] For ADSP-21060L/ADSP-21062L specification is –1 ns min.

Link Ports —1 × CLK Speed Operation

Table 23. Link Ports—Receive

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLDCL}	Data Setup Before LCLK Low[1]	3.5		3		ns
t_{HLDCL}	Data Hold After LCLK Low	3		3		ns
t_{LCLKIW}	LCLK Period (1× Operation)	t_{CK}		t_{CK}		ns
$t_{LCLKRWL}$	LCLK Width Low	6		6		ns
$t_{LCLKRWH}$	LCLK Width High	5		5		ns
Switching Characteristics						
t_{DLAHC}	LACK High Delay After CLKIN High[2, 3]	18 + DT/2	28.5 + DT/2	18 + DT/2	28.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High	–3	+13	–3	+13	ns
t_{ENDLK}	LACK Enable From CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable From CLKIN		20 + DT/2		20 + DT/2	ns

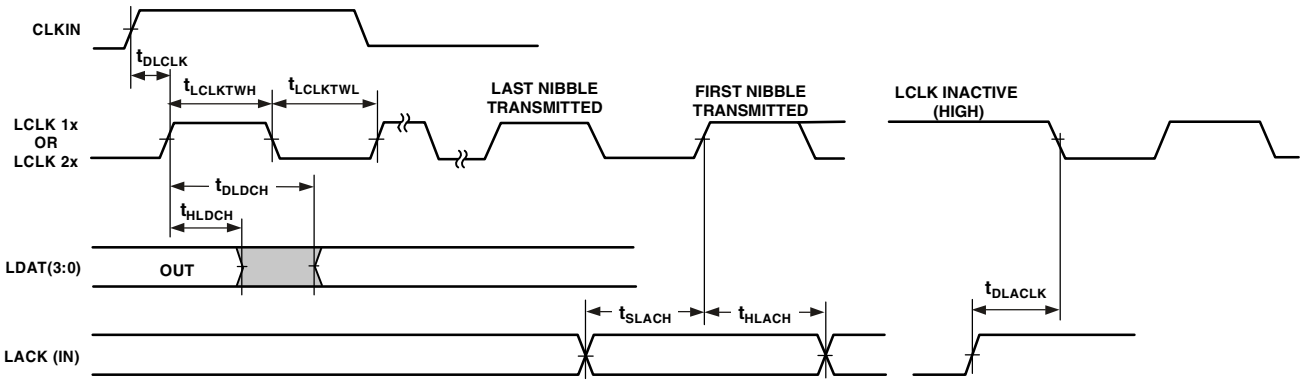
[1] For ADSP-21062, specification is 3 ns min.
[2] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[3] For ADSP-21060C, specification is 18 + DT/2 ns min, 29 + DT/2 ns max.

Table 24. Link Ports—Transmit

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLACH}	LACK Setup Before LCLK High[1]	18		18		ns
t_{HLACH}	LACK Hold After LCLK High	–7		–7		ns
Switching Characteristics						
t_{DLCLK}	Data Delay After CLKIN (1× Operation)[2]		15.5		15.5	ns
t_{DLDCH}	Data Delay After LCLK High[3]		3		2.5	ns
t_{HLDCH}	Data Hold After LCLK High	–3		–3		ns
$t_{LCLKTWL}$	LCLK Width Low[4]	(t_{CK}/2) – 2	(t_{CK}/2) + 2	(t_{CK}/2) – 1	(t_{CK}/2) + 1.25	ns
$t_{LCLKTWH}$	LCLK Width High[5]	(t_{CK}/2) – 2	(t_{CK}/2) + 2	(t_{CK}/2) – 1.25	(t_{CK}/2) + 1	ns
t_{DLACLK}	LCLK Low Delay After LACK High[6]	(t_{CK}/2) + 8.5	(3 × t_{CK}/2) + 17	(t_{CK}/2) + 8	(3 × t_{CK}/2) + 17.5	ns
t_{ENDLK}	LACK Enable From CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable From CLKIN		20 + DT/2		20 + DT/2	ns

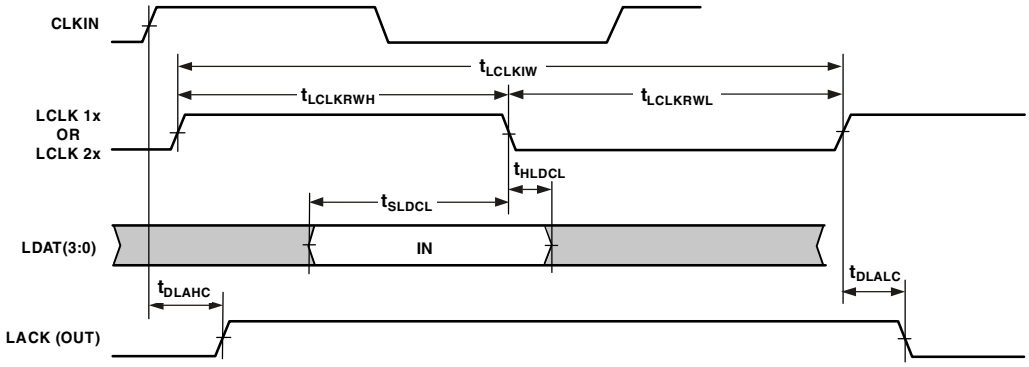
[1] For ADSP-21060L/ADSP-21060LC, specification is 20 ns min.
[2] For ADSP-21060L, specification is 16.5 ns max; for ADSP-21060LC, specification is 16.75 ns max.
[3] For ADSP-21062, specification is 2.5 ns max.
[4] For ADSP-21062, specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 1.25 ns max; for ADSP-21062L, specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 1.5 ns max; for ADSP-21060LC specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 2.25 ns max.
[5] For ADSP-21062, specification is (t_{CK}/2) – 1.25 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21062L, specification is (t_{CK}/2) – 1.5 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21060C specification is (t_{CK}/2) – 2.25 ns min, (t_{CK}/2) + 1 ns max.
[6] For ADSP-21062, specification is (t_{CK}/2) + 8.75 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21062L, specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21060LC specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 18.5 ns max.

TRANSMIT

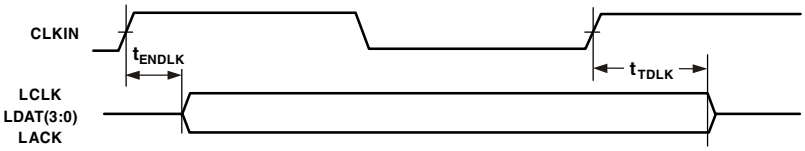


THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME

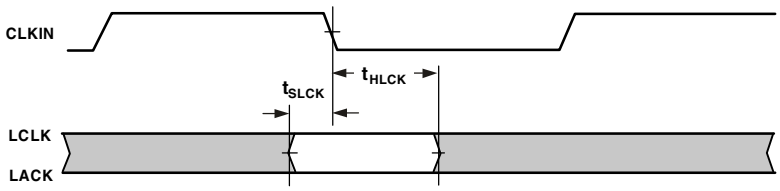


Figure 24. Link Ports—Receive

Serial Ports

For serial ports, see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 35, Figure 26, and Figure 25. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 28. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	6.5		ns
t_{SCLKW}	TCLK/RCLK Width[3]	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.
[3] For ADSP-21060/ADSP-21060C/ADSP-21060LC, specification is 9.5 ns min.

Table 29. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 30. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HDTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

Table 32. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –2.5	$0.5t_{SCLK}$+2.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 0.5_{TSCLK} – 2 ns min, $0.5t_{SCLK}$ + 2 ns max.

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1, 3]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1, 4]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3 DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 3.5 ns min; for ADSP-21062 specification is 4.5 ns min.
[3] For ADSP-21062L, specification is 16 ns max.
[4] For ADSP-21062L, specification is 7.5 ns max.

Table 34. Serial Ports—GATED SCLK with External TFS (Mesh Multiprocessing)[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{STFSCK}	TFS Setup Before CLKIN	4		ns
t_{HTFSCK}	TFS Hold After CLKIN		$t_{CK}/2$	ns

[1] Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1, 2]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1, 3]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.
[2] For ADSP-21062/ADSP-21062L, specification is 12.75 ns max; for ADSP-21060L/ADSP-21060LC, specification is 12.8 ns max.
[3] For ADSP-21060/ADSP-21060C, specification is 3 ns min.

TEST CONDITIONS

For the ac signal specifications (timing parameters), see Timing Specifications on Page 21. These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 28.

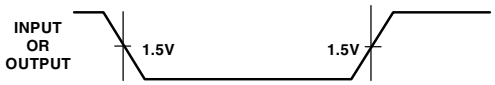


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

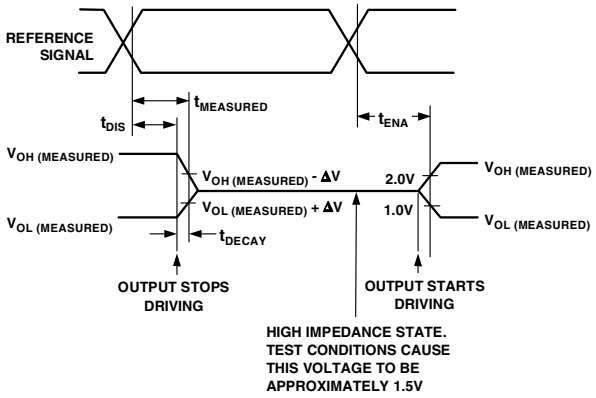


Figure 29. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 29). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 30). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 32, Figure 33, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 34 and Figure 36 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 32, Figure 33, Figure 37, and Figure 38 may not be linear outside the ranges shown.

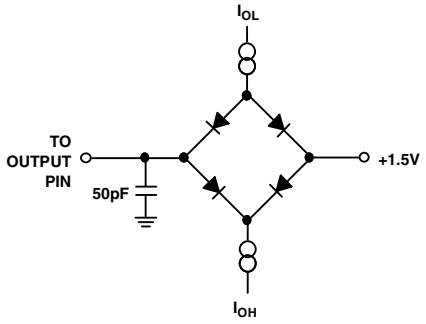


Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Output Drive Characteristics

Figure 31 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

Output Characteristics (5 V)

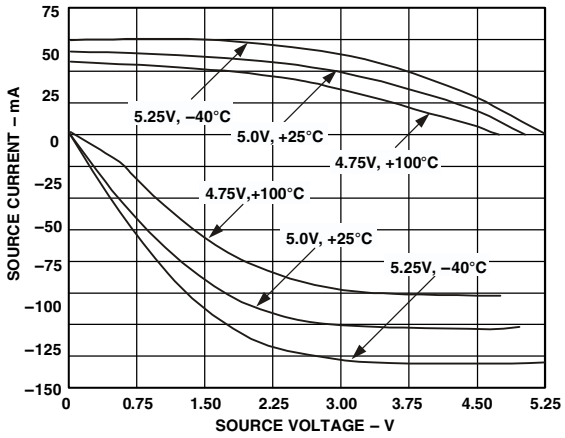


Figure 31. ADSP-21062 Typical Output Drive Currents (V_{DD} = 5 V)

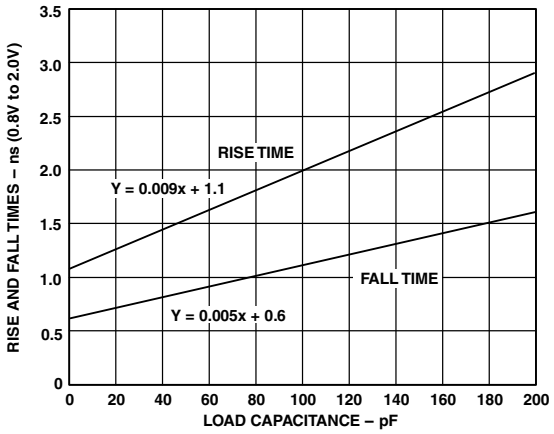


Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

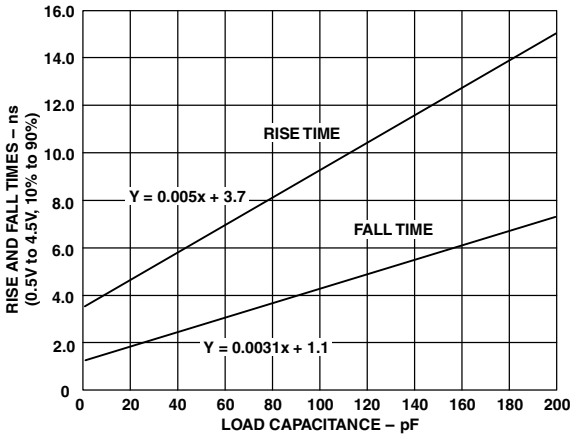


Figure 32. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

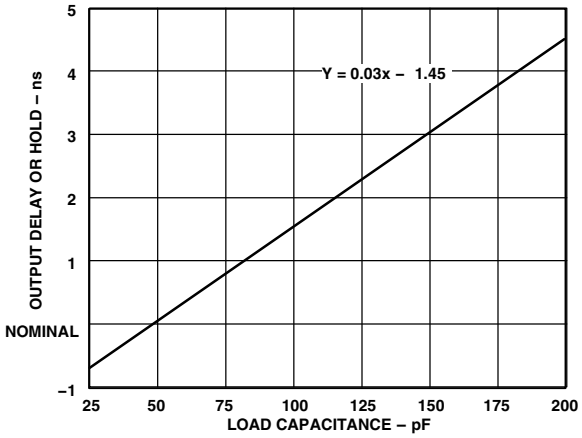


Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

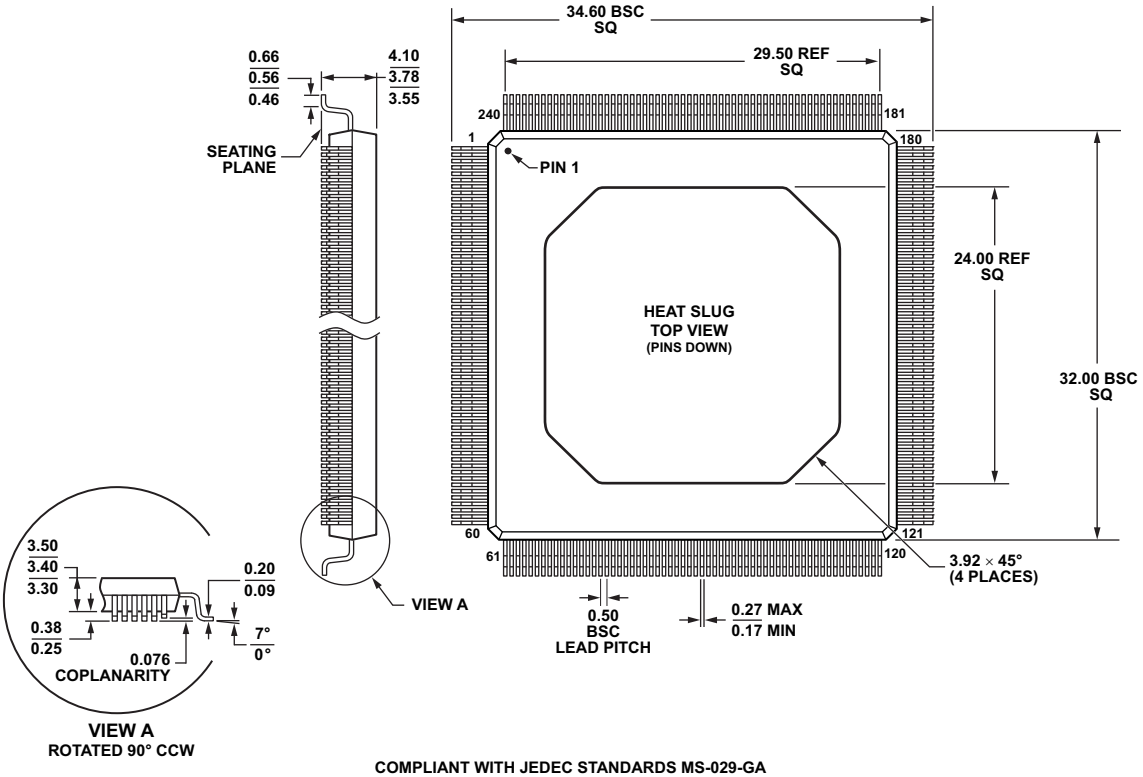


Figure 41. 240-Lead Metric Quad Flat Package, Thermally Enhanced "PowerQuad" [MQFP_PQ4]
(SP-240-2)
Dimensions shown in millimeters

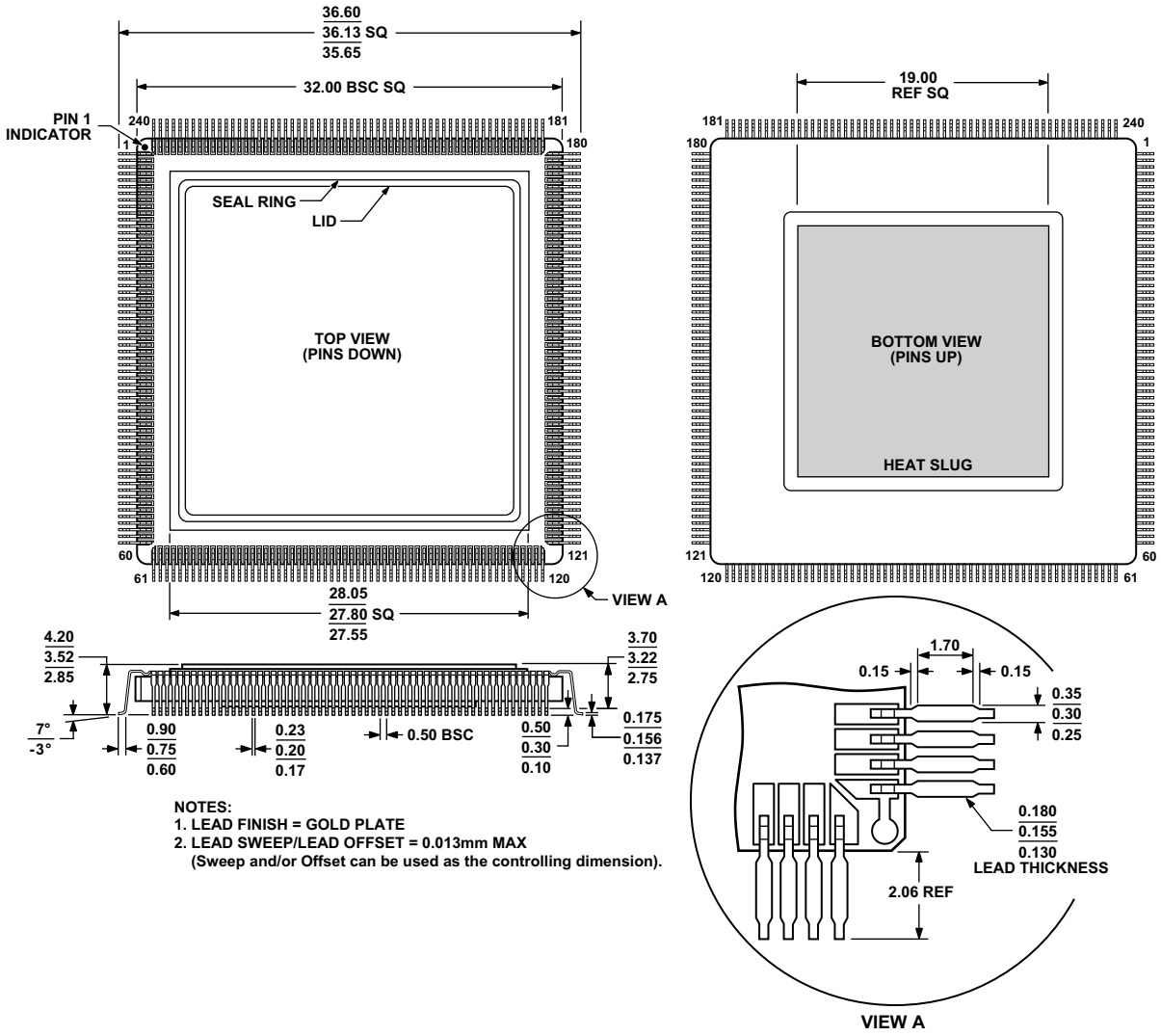


Figure 44. 240-Lead Ceramic Quad Flat Package, Heat Slug Down [CQFP]
(QS-240-1A)
Dimensions shown in millimeters

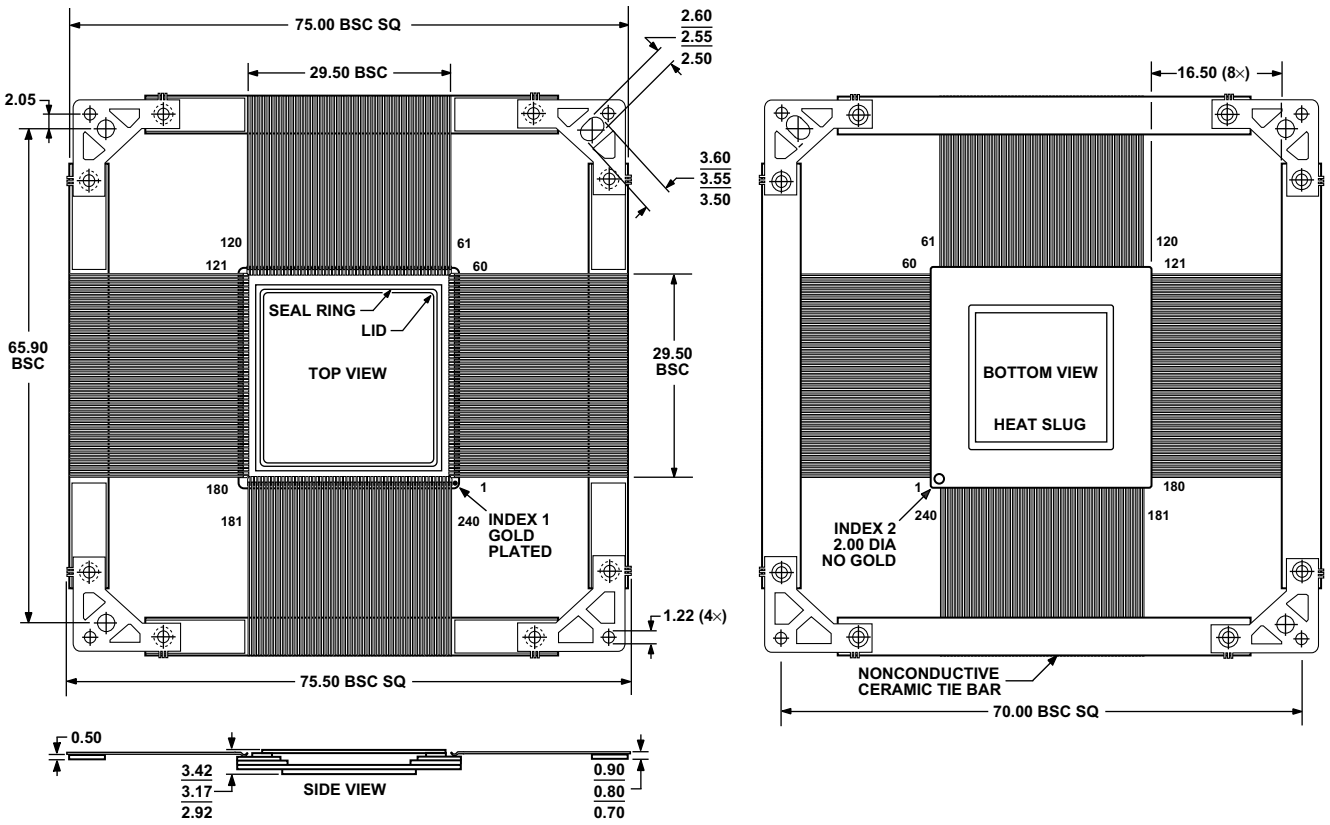


Figure 45. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Up [CQFP]
(QS-240-1B)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 43 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 43. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball Grid Array (PBGA)	Solder Mask Defined	0.63 mm diameter	0.76 mm diameter