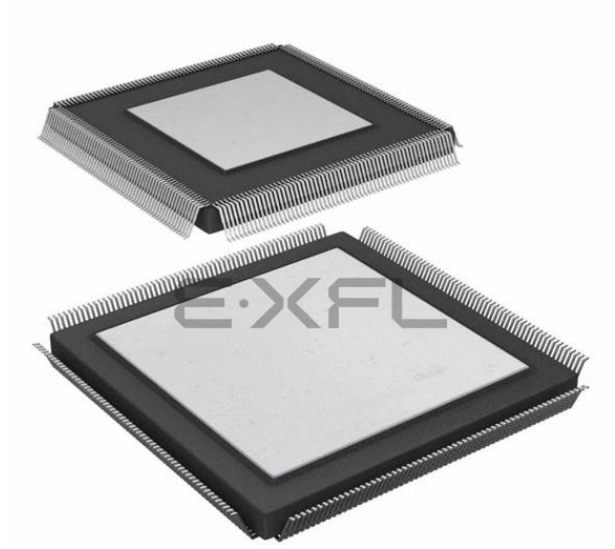

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFCQFP Exposed Pad
Supplier Device Package	240-CQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21060lcw-160

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2106x architecture and functionality. For detailed information on the ADSP-21000 family core architecture and instruction set, refer to the *ADSP-2106x SHARC User's Manual*, Revision 2.1.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The ADSP-2106x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31–0, DATA47–0, FLAG3–0, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, LxDAT3–0, LxCLK, LxACK, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 3. Pin Descriptions

Pin	Type	Function
ADDR31–0	I/O/T	**External Bus Address.** The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
DATA47–0	I/O/T	**External Bus Data.** The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47–8 of the bus. 16-bit short word data is transferred over bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23–16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS3–0}}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The $\overline{\text{MS3–0}}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{\text{MS3–0}}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{\text{MS0}}$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{\text{MS3–0}}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert $\overline{\text{RD}}$ to read from the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE® Emulator uses the IEEE 1149.1JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TRST, TDI, TDO, EMU, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

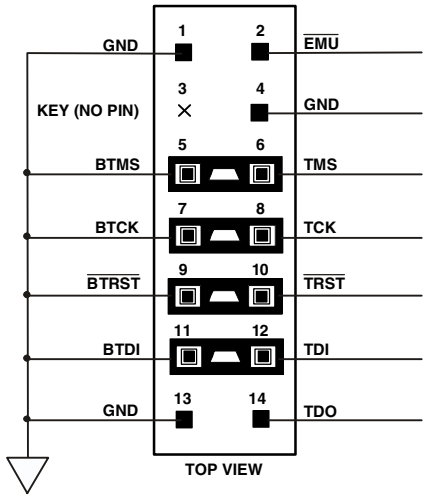


Figure 5. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, BTRST, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers on the Bxxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie BTRST to GND and tie or pull up BTCK to V_{DD}. The TRST pin must be asserted (pulsed low) after power-up (through BTRST on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 4.

Table 4. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
TRST[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled-Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
EMU	Active Low 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] TRST is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and EMU should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-2106xs (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x User's Manual*, Revision 2.1.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, EMU and TRST are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference*.

EXTERNAL POWER DISSIPATION (5 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 5. External Power Calculations (5 V Devices)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 25 V	= 0.084 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 25 V	= 0.022 W
Data	32	50	× 14.7 pF	× 10 MHz	× 25 V	= 0.059 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 25 V	= 0.002 W
						P_{EXT} = 0.167 W

Interrupts

Table 11. Interrupts

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulse Width[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

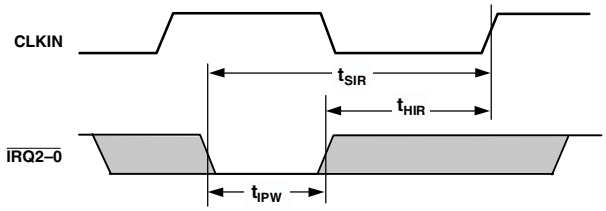


Figure 11. Interrupts

Timer

Table 12. Timer

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

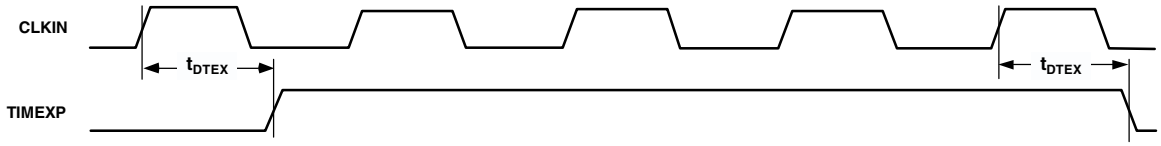


Figure 12. Timer

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 14. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 48 for the calculation of hold times given capacitive and dc loads.
[4] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

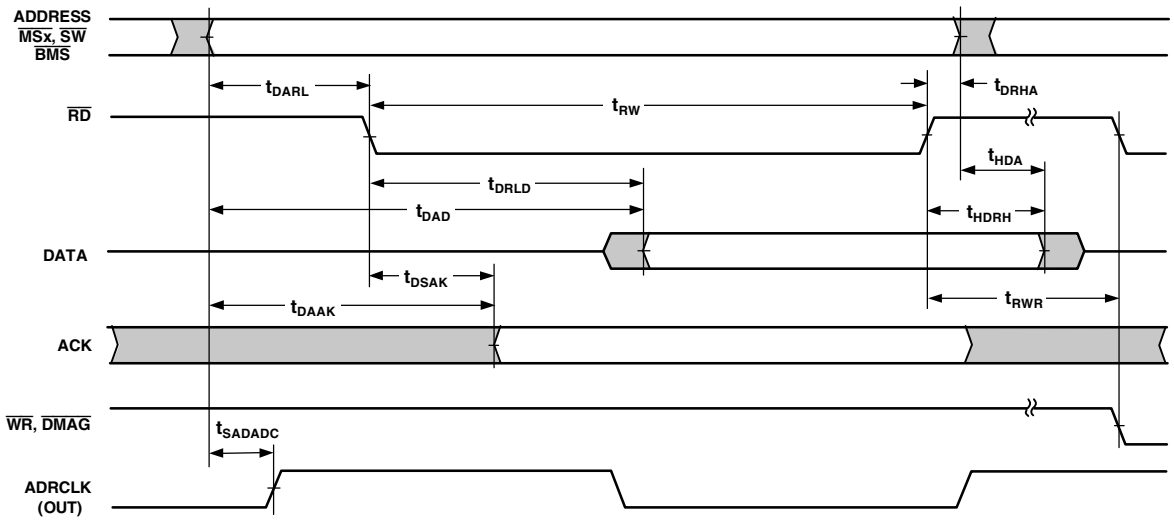


Figure 14. Memory Read—Bus Master

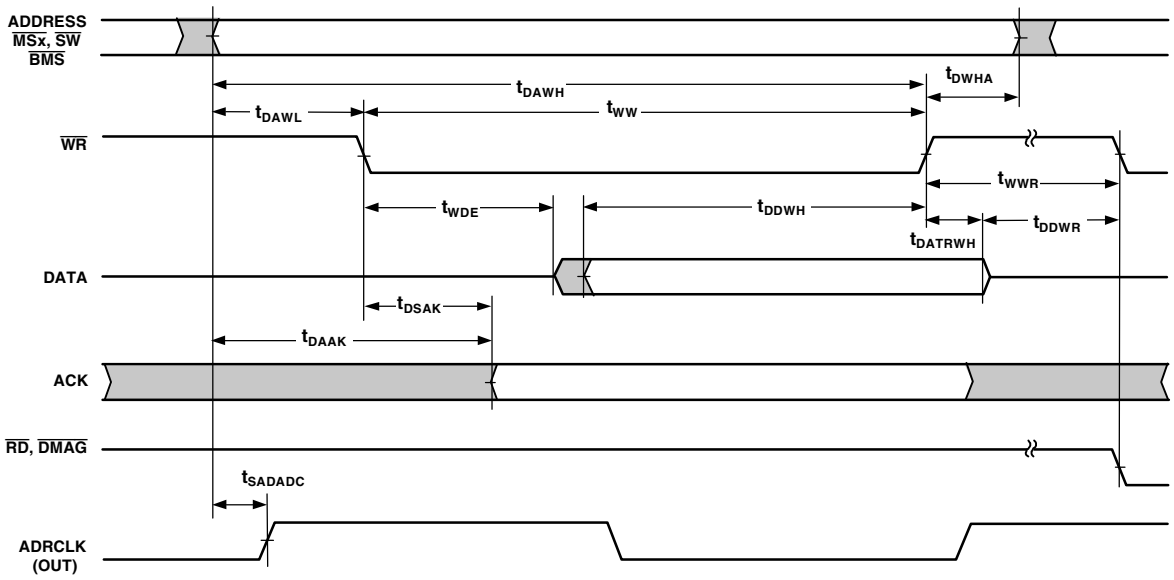


Figure 15. Memory Write—Bus Master

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 18. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BRx}$, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{BRx}$, $\overline{CPA}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	21 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		7 – DT/8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN[4]		8 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		8.5	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[6, 7]	44 + 23DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[6]		10	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual, Revision* 2.1.

[2] Only required for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For ADSP-21060LC, specification is 8.5 – DT/8 ns max.

[5] For ADSP-21060L, specification is 9.5 ns max, For ADSP-21060LC, specification is 11.0 ns max, For ADSP-21062L, specification is 8.75 ns max.

[6] (O/D) = open drain, (A/D) = active drive.

[7] For ADSP-21060C/ADSP-21060LC, specification is 40 + 23DT/16 ns min.

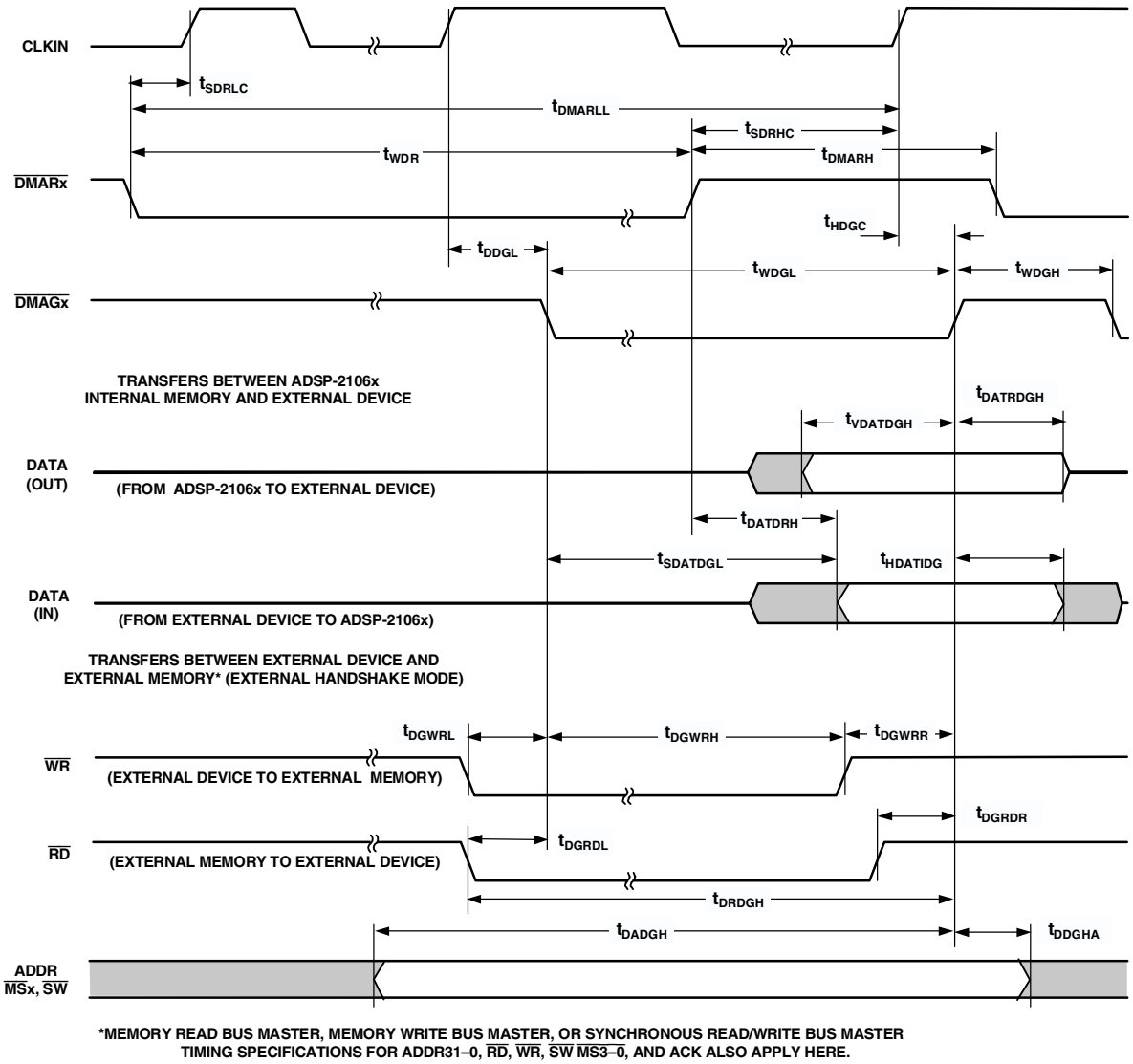


Figure 23. DMA Handshake

Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLCK}	LACK/LCLK Setup Before CLKIN Low[1]	10		10		ns
t_{HLCK}	LACK/LCLK Hold After CLKIN Low[1]	2		2		ns

[1] Only required for interrupt recognition in the current cycle.

Link Ports —2 × CLK Speed Operation

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$Setup\ Skew = t_{LCLKTWH}\ \text{min} - t_{DLDCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$Hold\ Skew = t_{LCLKTWL}\ \text{min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

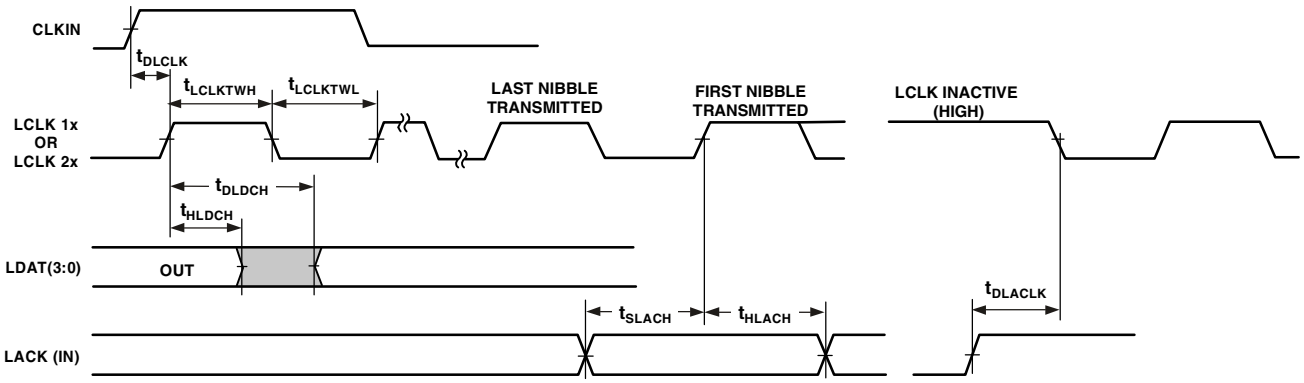
Note that link port transfers at 2× CLK speed at 40 MHz (t_{CK} = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz (t_{CK} = 30 ns) work as specified.

Table 26. Link Ports—Receive

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLDCL}	Data Setup Before LCLK Low	2.5		2.25		ns
t_{HLDCL}	Data Hold After LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2× Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low[1]	4.5		5.25		ns
$t_{LCLKRWH}$	LCLK Width High[2]	4.25		4		ns
Switching Characteristics						
t_{DLAHC}	LACK High Delay After CLKIN High[3]	18 + DT/2	28.5 + DT/2	18 + DT/2	29.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High[4]	6	16	6	16	ns

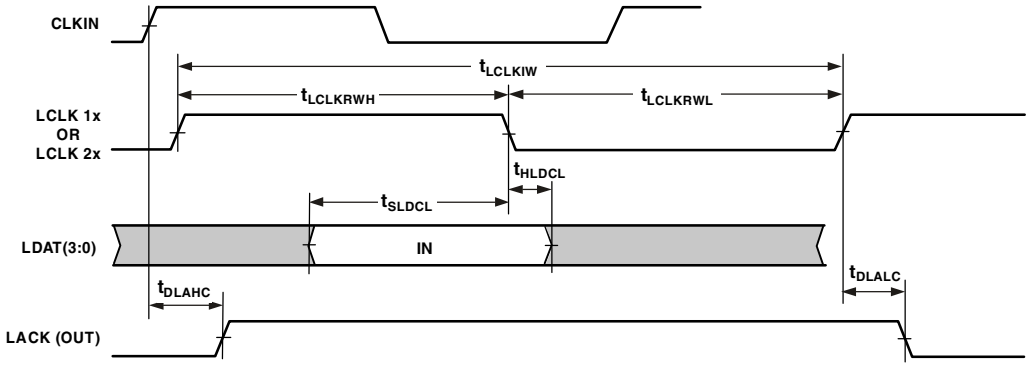
[1] For ADSP-21060L, specification is 5 ns min.
[2] For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.
[3] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[4] For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

TRANSMIT

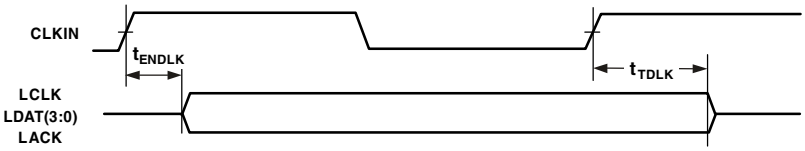


THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME

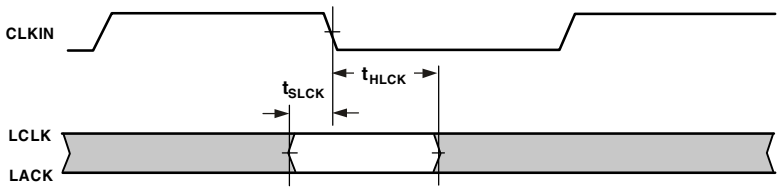


Figure 24. Link Ports—Receive

Serial Ports

For serial ports, see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 35, Figure 26, and Figure 25. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 28. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	6.5		ns
t_{SCLKW}	TCLK/RCLK Width[3]	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.
[3] For ADSP-21060/ADSP-21060C/ADSP-21060LC, specification is 9.5 ns min.

Table 29. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 30. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HDTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

TEST CONDITIONS

For the ac signal specifications (timing parameters), see Timing Specifications on Page 21. These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 28.

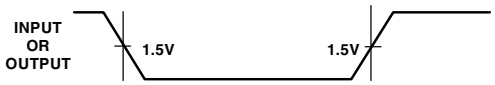


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

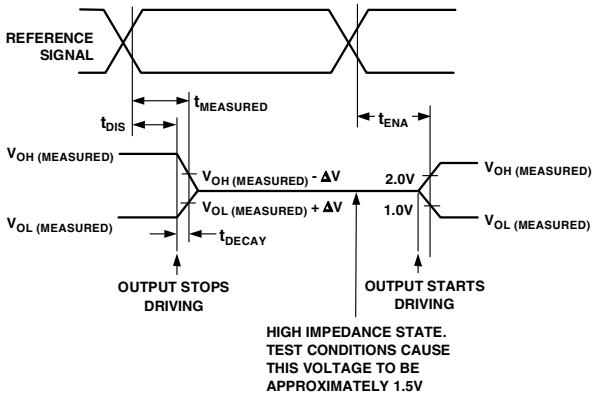


Figure 29. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 29). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 30). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 32, Figure 33, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 34 and Figure 36 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 32, Figure 33, Figure 37, and Figure 38 may not be linear outside the ranges shown.

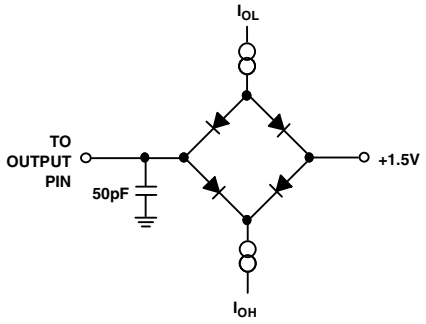


Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Output Drive Characteristics

Figure 31 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

ENVIRONMENTAL CONDITIONS

The ADSP-2106x processors are rated for performance under T_{CASE} environmental conditions specified in the Operating Conditions (5 V) on Page 15 and Operating Conditions (3.3 V) on Page 18.

Thermal Characteristics for MQFP_PQ4 and PBGA Packages

The ADSP-21060/ADSP-21060L and ADSP-21062/ADSP-21062L are available in 240-lead thermally enhanced MQFP_PQ4 and 225-ball plastic ball grid array packages. The top surface of the thermally enhanced MQFP_PQ4 contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

Both packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heatsink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)
T_{AMB} = Ambient temperature °C
PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Values from Table 37 and Table 38 below.

Table 37. Thermal Characteristics for Thermally Enhanced 240-Lead MQFP_PQ4[1]

Parameter	Airflow (LFM[2])	Typical	Unit
θ_{CA}	0	10	°C/W
θ_{CA}	100	9	°C/W
θ_{CA}	200	8	°C/W
θ_{CA}	400	7	°C/W
θ_{CA}	600	6	°C/W

[1] This represents thermal resistance at total power of 5 W. With airflow, no variance is seen in θ_{CA} at 5 W.
θ_{CA} at 0 LFM varies with power:
at 2 W, θ_{CA} = 14°C/W
at 3 W, θ_{CA} = 11°C/W
[2] LFM = Linear feet per minute of airflow.

Table 38. Thermal Characteristics for BGA

Parameter	Airflow (LFM[1])	Typical	Unit
θ_{CA}	0	20.70	°C/W
θ_{CA}	200	15.30	°C/W
θ_{CA}	400	12.90	°C/W

[1] LFM = Linear feet per minute of airflow.

Thermal Characteristics for CQFP Package

The ADSP-21060C/ADSP-21060LC are available in 240-lead thermally enhanced ceramic QFP (CQFP). There are two package versions, one with a copper/tungsten heat slug on top of the package (CZ) for air cooling, and one with the heat slug on the bottom (CW) for cooling through the board. The ADSP-2106x is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. A heatsink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)
T_{AMB} = Ambient temperature °C
PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from Table 39 below.

Table 39. Thermal Characteristics for Thermally Enhanced 240-Lead CQFP[1]

Parameter	Airflow (LFM[2])	Typical	Unit
ADSP-21060CW/ADSP-21060LCW			
θ_{CA}	0	19.5	°C/W
θ_{CA}	100	16	°C/W
θ_{CA}	200	14	°C/W
θ_{CA}	400	12	°C/W
θ_{CA}	600	10	°C/W
ADSP-21060CZ/ADSP-21060LCZ			
θ_{CA}	0	20	°C/W
θ_{CA}	100	16	°C/W
θ_{CA}	200	14	°C/W
θ_{CA}	400	11.5	°C/W
θ_{CA}	600	9.5	°C/W

[1] This represents thermal resistance at total power of 5 W. With airflow, no variance is seen in θ_{CA} at 5W.
θ_{CA} at 0 LFM varies with power.
ADSP-21060CW/ADSP-21060LCW:
at 2 W, θ_{CA} = 23°C/W
at 3 W, θ_{CA} = 21.5°C/W
ADSP-21060CZ/ADSP-21060LCZ:
at 2 W, θ_{CA} = 24°C/W
at 3 W, θ_{CA} = 21.5°C/W
θ_{JC} = 0.24°C/W for all CQFP models.
[2] LFM = Linear feet per minute of airflow.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DATA42	DATA44	DATA47	$\overline{BR3}$	PAGE	CLKIN	$\overline{CS}$	ADRCLK	RCLK0	TCLK0	RCLK1	DT1	$\overline{DMAR2}$	ADDR30	$\overline{BMS}$	A
DATA39	DATA43	DATA45	$\overline{BR2}$	$\overline{BR6}$	ACK	$\overline{RD}$	REDY	DR0	DT0	DR1	$\overline{HBR}$	ADDR31	$\overline{SW}$	$\overline{MS0}$	B
DATA36	DATA38	DATA41	DATA46	$\overline{BR4}$	$\overline{DMAG1}$	$\overline{WR}$	RFS0	TFS0	RFS1	TCLK1	$\overline{SBTS}$	ADDR28	$\overline{MS1}$	$\overline{MS3}$	C
DATA34	DATA35	DATA37	DATA40	$\overline{BR1}$	$\overline{BR5}$	$\overline{DMAG2}$	$\overline{HBG}$	$\overline{CPA}$	TFS1	$\overline{DMAR1}$	ADDR29	$\overline{MS2}$	ADDR26	ADDR25	D
DATA31	DATA32	DATA30	DATA33	NC	GND	GND	GND	GND	GND	GND	ADDR27	ADDR24	ADDR22	ADDR21	E
DATA27	DATA28	DATA26	DATA29	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	GND	ADDR23	ADDR20	ADDR18	ADDR17	F
DATA23	DATA24	DATA25	DATA22	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR19	ADDR16	ADDR15	ADDR14	G
DATA20	DATA21	DATA19	DATA18	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR10	ADDR13	ADDR11	ADDR12	H
DATA17	DATA16	DATA15	DATA12	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR4	ADDR7	ADDR8	ADDR9	J
DATA14	DATA13	DATA11	DATA8	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	ICSA	ADDR0	ADDR3	ADDR5	ADDR6	K
DATA10	DATA9	DATA7	DATA4	NC	GND	GND	GND	GND	GND	RPBA	FLAG3	FLAG0	ADDR1	ADDR2	L
DATA6	DATA5	DATA2	L0DAT0	L1DAT1	L2DAT3	L3DAT0	L4DAT2	L5DAT2	L5ACK	LBOOT	TDI	TIMEXP	FLAG2	FLAG1	M
DATA3	DATA1	L0DAT3	L1DAT3	L1ACK	L2DAT0	L3DAT3	L3CLK	L4CLK	L5DAT1	ID2	$\overline{IRQ1}$	$\overline{IRQ0}$	TDO	$\overline{EMU}$	N
DATA0	L0DAT1	L0ACK	L1DAT0	L2DAT2	L2CLK	L3DAT2	L4DAT3	L4DAT0	L5DAT3	L5CLK	ID0	EBOOT	TMS	$\overline{TRST}$	P
L0DAT2	L0CLK	L1DAT2	L1CLK	L2DAT1	L2ACK	L3DAT1	L3ACK	L4DAT1	L4ACK	L5DAT0	ID1	$\overline{RESET}$	$\overline{IRQ2}$	TCK	R

Figure 39. ADSP-21060/ADSP-21062 PBGA Ball Assignments (Top View, Summary)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

Table 42. ADSP-21060CW/21060LCW CQFP Pin Assignments (QS-240-1A, QS-240-1B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	DATA29	41	$\overline{\text{DMAG2}}$	81	ADDR28	121	ADDR5	161	GND	201
DATA0	2	GND	42	ACK	82	$\overline{\text{BMS}}$	122	GND	162	V_{DD}	202
DATA1	3	DATA30	43	CLKIN	83	$\overline{\text{SW}}$	123	ADDR4	163	L4ACK	203
DATA2	4	DATA31	44	GND	84	$\overline{\text{MS0}}$	124	ADDR3	164	L4CLK	204
V_{DD}	5	DATA32	45	V_{DD}	85	$\overline{\text{MS1}}$	125	ADDR2	165	L4DAT0	205
DATA3	6	GND	46	GND	86	$\overline{\text{MS2}}$	126	V_{DD}	166	L4DAT1	206
DATA4	7	V_{DD}	47	$\overline{\text{WR}}$	87	$\overline{\text{MS3}}$	127	ADDR1	167	L4DAT2	207
DATA5	8	V_{DD}	48	$\overline{\text{RD}}$	88	GND	128	ADDR0	168	L4DAT3	208
GND	9	DATA33	49	$\overline{\text{CS}}$	89	ADDR27	129	GND	169	GND	209
DATA6	10	DATA34	50	$\overline{\text{HBG}}$	90	ADDR26	130	FLAG0	170	L3ACK	210
DATA7	11	DATA35	51	REDY	91	ADDR25	131	FLAG1	171	L3CLK	211
DATA8	12	NC	52	ADRCLK	92	V_{DD}	132	FLAG2	172	L3DAT0	212
V_{DD}	13	GND	53	GND	93	GND	133	FLAG3	173	L3DAT1	213
DATA9	14	DATA36	54	V_{DD}	94	V_{DD}	134	ICSA	174	L3DAT2	214
DATA10	15	DATA37	55	V_{DD}	95	ADDR24	135	$\overline{\text{EMU}}$	175	L3DAT3	215
DATA11	16	DATA38	56	RFS0	96	ADDR23	136	TIMEXP	176	V_{DD}	216
GND	17	V_{DD}	57	RCLK0	97	ADDR22	137	TDO	177	NC	217
DATA12	18	DATA39	58	DR0	98	GND	138	V_{DD}	178	L2ACK	218
DATA13	19	DATA40	59	TFS0	99	ADDR21	139	$\overline{\text{TRST}}$	179	L2CLK	219
DATA14	20	DATA41	60	TCLK0	100	ADDR20	140	TDI	180	L2DAT0	220
V_{DD}	21	GND	61	DT0	101	ADDR19	141	TMS	181	L2DAT1	221
DATA15	22	DATA42	62	$\overline{\text{CPA}}$	102	V_{DD}	142	TCK	182	L2DAT2	222
DATA16	23	DATA43	63	GND	103	V_{DD}	143	$\overline{\text{IRQ0}}$	183	L2DAT3	223
DATA17	24	DATA44	64	RFS1	104	ADDR18	144	$\overline{\text{IRQ1}}$	184	V_{DD}	224
GND	25	V_{DD}	65	RCLK1	105	ADDR17	145	$\overline{\text{IRQ2}}$	185	GND	225
DATA18	26	DATA45	66	DR1	106	ADDR16	146	EBOOT	186	GND	226
DATA19	27	DATA46	67	TFS1	107	GND	147	$\overline{\text{RESET}}$	187	L1ACK	227
DATA20	28	DATA47	68	TCLK1	108	ADDR15	148	RPBA	188	L1CLK	228
V_{DD}	29	GND	69	DT1	109	ADDR14	149	LBOOT	189	L1DAT0	229
DATA21	30	V_{DD}	70	$\overline{\text{HBR}}$	110	V_{DD}	150	ID0	190	L1DAT1	230
DATA22	31	GND	71	$\overline{\text{DMAR1}}$	111	ADDR13	151	ID1	191	L1DAT2	231
DATA23	32	$\overline{\text{BR1}}$	72	$\overline{\text{DMAR2}}$	112	ADDR12	152	ID2	192	L1DAT3	232
GND	33	$\overline{\text{BR2}}$	73	$\overline{\text{SBTS}}$	113	ADDR11	153	GND	193	V_{DD}	233
DATA24	34	$\overline{\text{BR3}}$	74	GND	114	GND	154	L5ACK	194	L0ACK	234
DATA25	35	$\overline{\text{BR4}}$	75	ADDR31	115	ADDR10	155	L5CLK	195	L0CLK	235
DATA26	36	$\overline{\text{BR5}}$	76	ADDR30	116	ADDR9	156	L5DAT0	196	L0DAT0	236
V_{DD}	37	$\overline{\text{BR6}}$	77	ADDR29	117	ADDR8	157	L5DAT1	197	L0DAT1	237
V_{DD}	38	V_{DD}	78	V_{DD}	118	V_{DD}	158	L5DAT2	198	L0DAT2	238
DATA27	39	PAGE	79	V_{DD}	119	ADDR7	159	L5DAT3	199	L0DAT3	239
DATA28	40	$\overline{\text{DMAG1}}$	80	GND	120	ADDR6	160	V_{DD}	200	GND	240

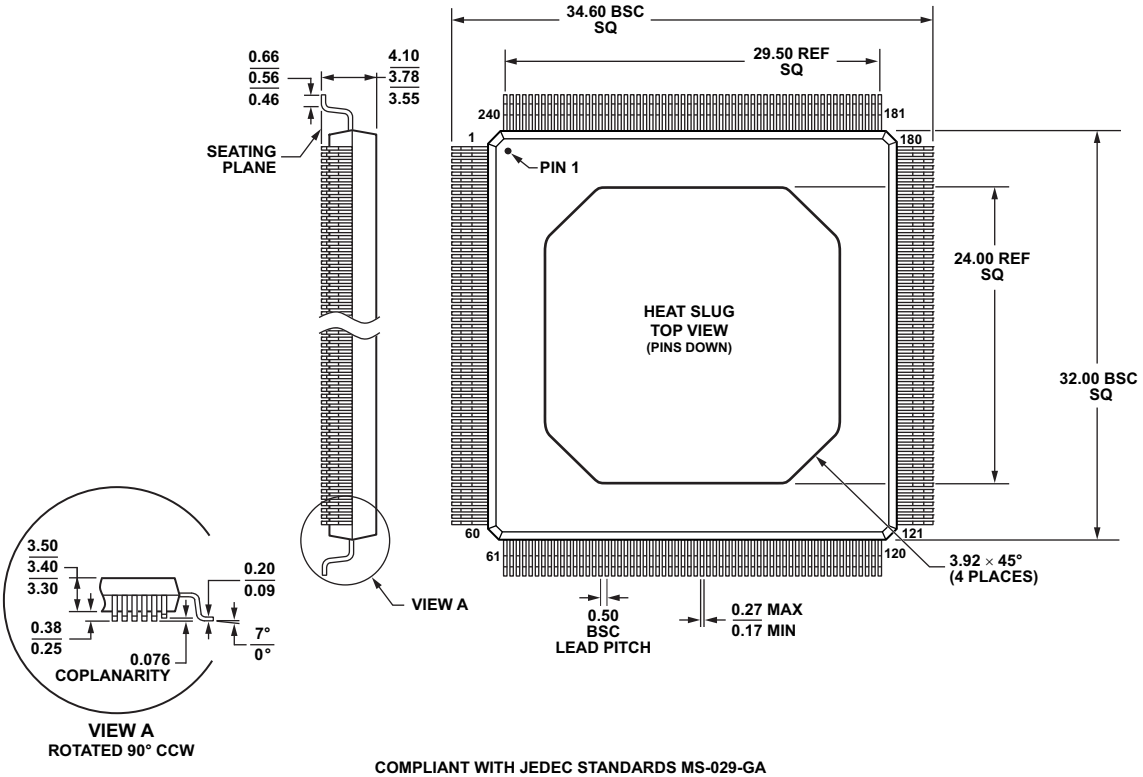


Figure 41. 240-Lead Metric Quad Flat Package, Thermally Enhanced "PowerQuad" [MQFP_PQ4]
(SP-240-2)
Dimensions shown in millimeters

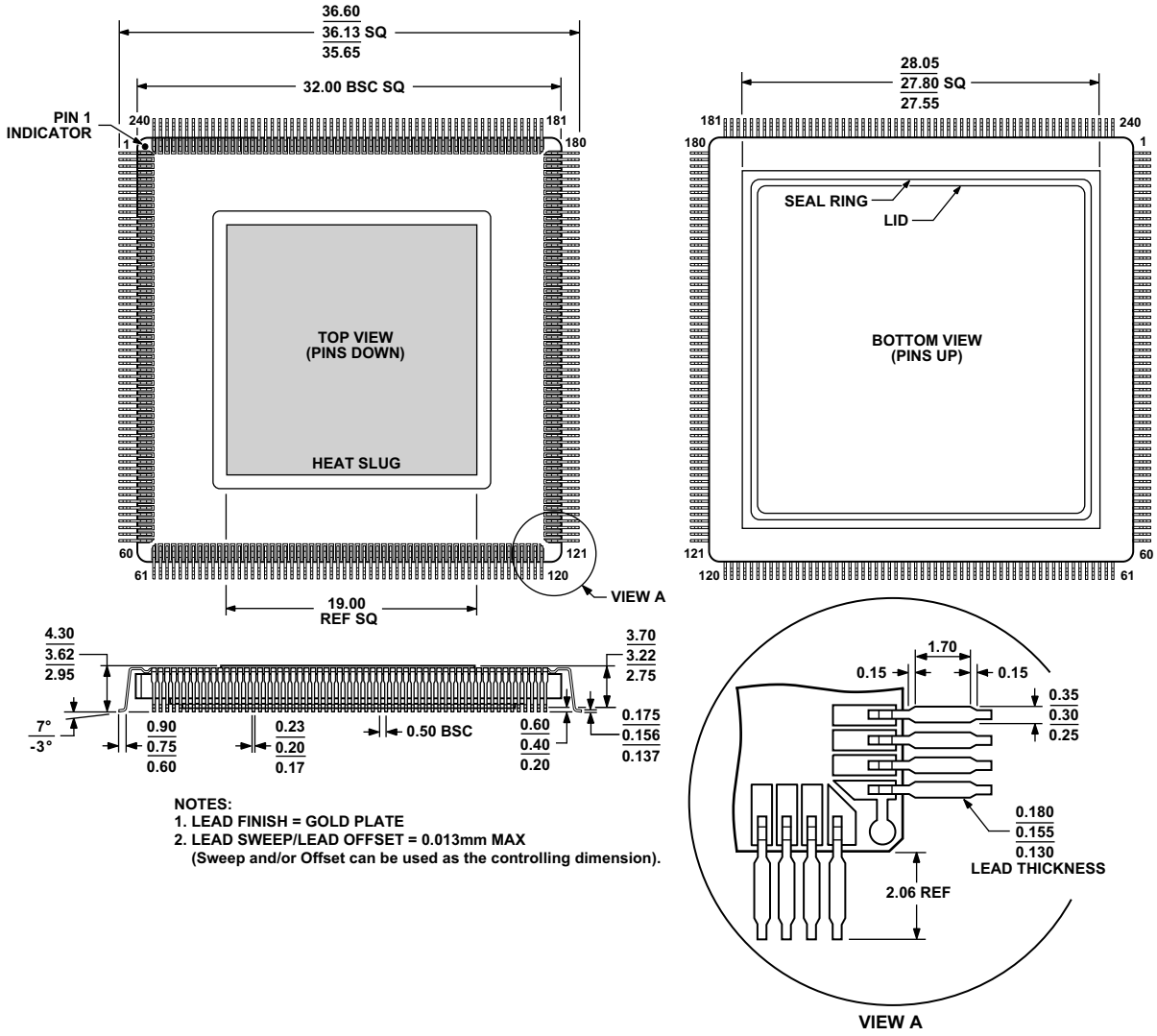


Figure 42. 240-Lead Ceramic Quad Flat Package, Heat Slug Up [CQFP]
(QS-240-2A)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ASDP-21060CZ-133	1, 2	–40°C to +100°C	33 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Up]	QS-240-2A
ASDP-21060CZ-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Up]	QS-240-2A
ASDP-21060CW-133	1, 2	–40°C to +100°C	33 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ASDP-21060CW-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	5 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ADSP-21060KS-133		0°C to 85°C	33 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KSZ-133	2	0°C to 85°C	33 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KS-160		0°C to 85°C	40 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KSZ-160	2	0°C to 85°C	40 MHz	4M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060KB-160		0°C to 85°C	40 MHz	4M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21060KBZ-160	2	0°C to 85°C	40 MHz	4M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21060LKSZ-133	2	0°C to 85°C	33 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKS-160		0°C to 85°C	40 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKSZ-160	2	0°C to 85°C	40 MHz	4M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21060LKB-160		0°C to 85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LAB-160		–40°C to +85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LABZ-160	2	–40°C to +85°C	40 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LCB-133		–40°C to +100°C	33 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21060LCBZ-133	2	–40°C to +100°C	33 MHz	4M Bit	3.3 V	225-Ball PBGA	B-225-2
ASDP-21060LCW-160	1, 2	–40°C to +100°C	40 MHz	4M Bit	3.3 V	240-Lead CQFP [Heat Slug Down]	QS-240-1A
ADSP-21062KS-133		0°C to 85°C	33 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KSZ-133	2	0°C to 85°C	33 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KS-160		0°C to 85°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KSZ-160	2	0°C to 85°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062KB-160		0°C to 85°C	40 MHz	2M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21062KBZ-160	2	0°C to 85°C	40 MHz	2M Bit	5 V	225-Ball PBGA	B-225-2
ADSP-21062CS-160		–40°C to +100°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062CSZ-160	2	–40°C to +100°C	40 MHz	2M Bit	5 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKSZ-133	2	0°C to 85°C	33 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKS-160		0°C to 85°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKSZ-160	2	0°C to 85°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LKB-160		0°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LKBZ-160	2	0°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LAB-160		–40°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LABZ-160	2	–40°C to 85°C	40 MHz	2M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21062LCS-160		–40°C to +100°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2
ADSP-21062LCSZ-160	2	–40°C to +100°C	40 MHz	2M Bit	3.3 V	240-Lead MQFP_PQ4	SP-240-2

[1] Model refers to package with formed leads. For model numbers of unformed lead versions (QS-240-1B, QS-240-2B), contact Analog Devices or an Analog Devices sales representative.
[2] RoHS compliant part.