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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21060lks-160

PARALLEL COMPUTATIONS

Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch

Multiply with add and subtract for accelerated FFT butterfly computation

UP TO 4M BIT ON-CHIP SRAM

Dual-ported for independent access by core processor and DMA

OFF-CHIP MEMORY INTERFACING

4 gigawords addressable

Programmable wait state generation, page-mode DRAM support

DMA CONTROLLER

10 DMA channels for transfers between ADSP-2106x internal memory and external memory, external peripherals, host processor, serial ports, or link ports

Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

HOST PROCESSOR INTERFACE TO 16- AND 32-BIT MICROPROCESSORS

Host can directly read/write ADSP-2106x internal memory and IOP registers

MULTIPROCESSING

Glueless connection for scalable DSP multiprocessing architecture

Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-2106xs plus host

Six link ports for point-to-point connectivity and array multiprocessing

240 MBps transfer rate over parallel bus

240 MBps transfer rate over link ports

SERIAL PORTS

Two 40 Mbps synchronous serial ports with companding hardware

Independent transmit and receive functions

Table 1. ADSP-2106x SHARC Processor Family Features

Feature	ADSP-21060	ADSP-21062	ADSP-21060L	ADSP-21062L	ADSP-21060C	ADSP-21060LC
SRAM	4M bits	2M bits	4M bits	2M bits	4M bits	4M bits
Operating Voltage	5 V	5 V	3.3 V	3.3 V	5 V	3.3 V
Instruction Rate	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz
Package	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	CQFP	CQFP

CONTENTS

REVISION HISTORY

3/13—Rev. G to Rev. H

Updated Development Tools 8

Corrected the power dissipation equation from $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$ to $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$
External Power Dissipation (3.3 V) 20

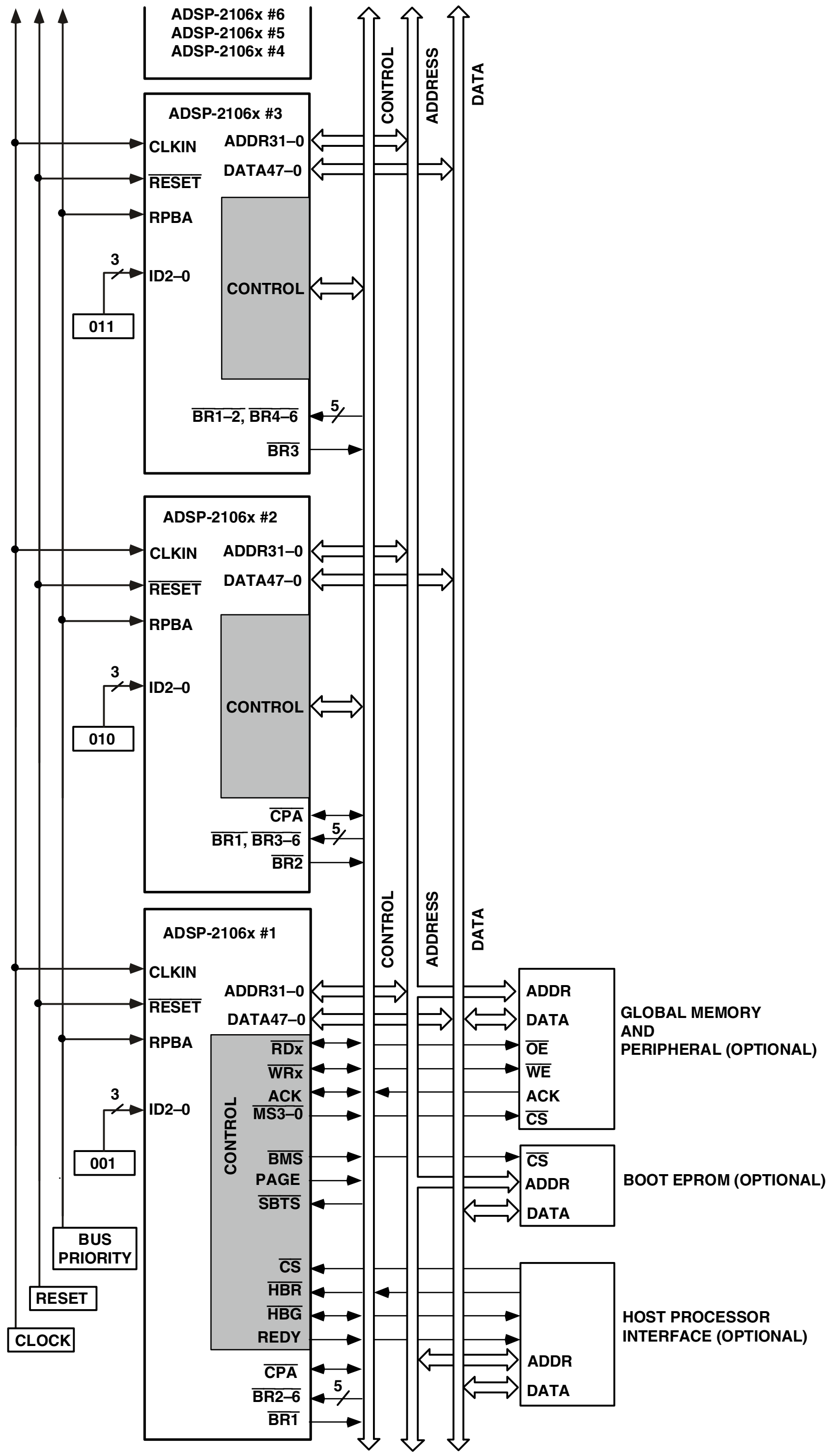

Figure 3. Shared Memory Multiprocessing System

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE® Emulator uses the IEEE 1149.1JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TRST, TDI, TDO, EMU, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

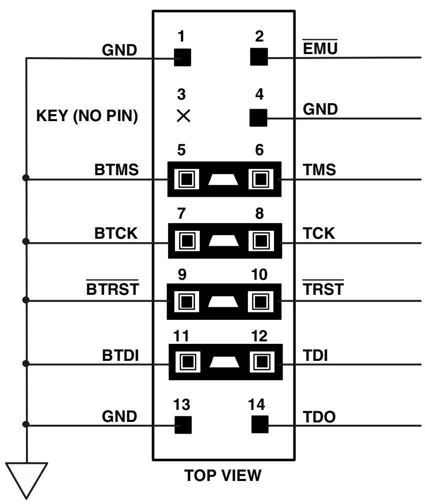

Figure 5. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, BTRST, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers on the Bxxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie BTRST to GND and tie or pull up BTCK to V_{DD}. The TRST pin must be asserted (pulsed low) after power-up (through BTRST on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 4.

Table 4. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
TRST[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled-Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
EMU	Active Low 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] TRST is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and EMU should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-2106xs (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x User's Manual*, Revision 2.1.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, EMU and TRST are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference*.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	540	mA
	t_{CK} = 25 ns, V_{DD} = Max	600	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	425	mA
	t_{CK} = 25 ns, V_{DD} = Max	475	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	250	mA
	t_{CK} = 25 ns, V_{DD} = Max	275	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	180	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106xL state during execution of IDLE instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 6. External Power Calculations (3.3 V Devices)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed Table 7 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	ADSP-21060/ADSP-21060C ADSP-21062 5 V	ADSP-21060L/ADSP-21060LC ADSP-21062L 3.3 V
Supply Voltage (V_{DD})	–0.3 V to +7.0 V	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} + 0.5 V	–0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF	200 pF
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C
Lead Temperature (5 seconds)	280°C	280°C
Junction Temperature Under Bias	130°C	130°C

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 30). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 16. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	3 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[1, 2]		14 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[2]	6.5+DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{\text{MSx}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$ Delay After CLKIN[1]		7 – DT/8	ns
t_{HADRO}	Address, $\overline{\text{MSx}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{\text{RD}}$ High Delay After CLKIN	–2 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{\text{WR}}$ High Delay After CLKIN	–3 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Low Delay After CLKIN	8 + DT/4	12.5 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] The falling edge of $\overline{\text{MSx}}$, $\overline{\text{SW}}$, $\overline{\text{BMS}}$ is referenced.

[2] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet the bus slave timing requirements.

Table 17. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	15 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}$/$\overline{WR}$ Low Setup Before CLKIN[1]	9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}$/$\overline{WR}$ Low Hold After CLKIN[2]	–4 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}$/$\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN[3]		18 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[5]		9	ns
t_{ACKTR}	ACK Disable After CLKIN[5]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.
[2] For ADSP-21060C specification is –3.5 – 5DT/16 ns min, 8 + 7DT/16 ns max; for ADSP-21060LC specification is –3.75 – 5DT/16 ns min, 8 + 7DT/16 ns max.
[3] For ADSP-21062/ADSP-21062L/ADSP-21060C specification is 19 + 5DT/16 ns max; for ADSP-21060LC specification is 19.25 + 5DT/16 ns max.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

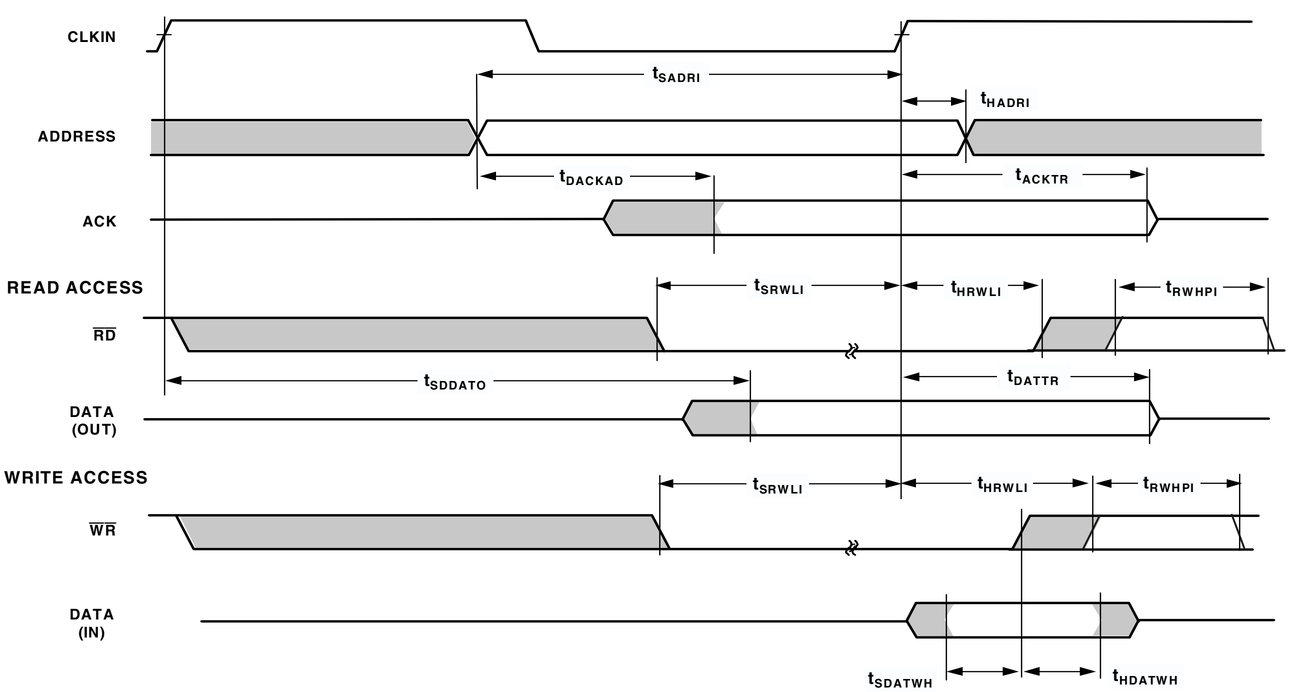

Figure 17. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 18. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}/\overline{WR}/\overline{CS}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BRx}$, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{BRx}$, $\overline{CPA}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	21 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		7 – DT/8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN[4]		8 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		8.5	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[6, 7]	44 + 23DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[6]		10	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual, Revision* 2.1.

[2] Only required for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For ADSP-21060LC, specification is 8.5 – DT/8 ns max.

[5] For ADSP-21060L, specification is 9.5 ns max, For ADSP-21060LC, specification is 11.0 ns max, For ADSP-21062L, specification is 8.75 ns max.

[6] (O/D) = open drain, (A/D) = active drive.

[7] For ADSP-21060C/ADSP-21060LC, specification is 40 + 23DT/16 ns min.

Asynchronous Read/Write—Host to ADSP-2106x

Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-2106x, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-2106x's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Not required if and address are valid $t_{HBGRCSV}$ after goes low. For first access after asserted, ADDR31–0 must be a non-MMS value 1/2 t_{CLK} before or goes low or by $t_{HBGRCSV}$ after goes low. This is easily accomplished by driving an upper address signal high when is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual*, Revision 2.1.

Table 19. Read Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$	0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low[2]		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulse Width for Read	45 + 21DT/16		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High[3]	2	8	ns

[1] Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual,* Revision 2.1.

[2] For ADSP-21060L, specification is 10.5 ns max; for ADSP-21060LC, specification is 12.5 ns max.

[3] For ADSP-21060L/ADSP-21060LC, specification is 2 ns min, 8.5 ns max.

Table 20. Write Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	7		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		10	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulse Width for Write	15 + 7DT/16		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

Three-State Timing—Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Table 21. Three-State Timing—Bus Master, Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	12 + DT/2		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold Before CLKIN		6 + DT/2	ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN[1]	–1.5 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[2]	–1.5 – DT/8		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable After CLKIN[3]		0 – DT/4	ns
t_{MITRS}	Strobes Disable After CLKIN[2]		1.5 – DT/4	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN		2.0 – DT/4	ns
t_{DATEN}	Data Enable After CLKIN[4]	9 + 5DT/16		ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable After CLKIN[4]	7.5 + DT/4		ns
t_{ACKTR}	ACK Disable After CLKIN[4]	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable After CLKIN	–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable After CLKIN		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{\text{HBG}}$ Low[5]	0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[5]	19 + DT		ns

[1] For ADSP-21060L/ADSP-21060LC/ADSP-21062L, specification is –1.25 – DT/8 ns min, for ADSP-21062, specification is –1 – DT/8 ns min.
[2] Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, $\overline{\text{DMAG}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$.
[3] For ADSP-21060LC, specification is 0.25 – DT/4 ns max.
[4] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[5] Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MSx}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode).

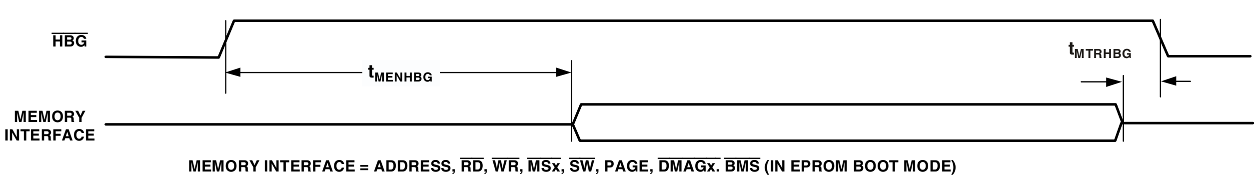

Figure 21. Three-State Timing (Bus Transition Cycle, $\overline{\text{SBTS}}$ Assertion)

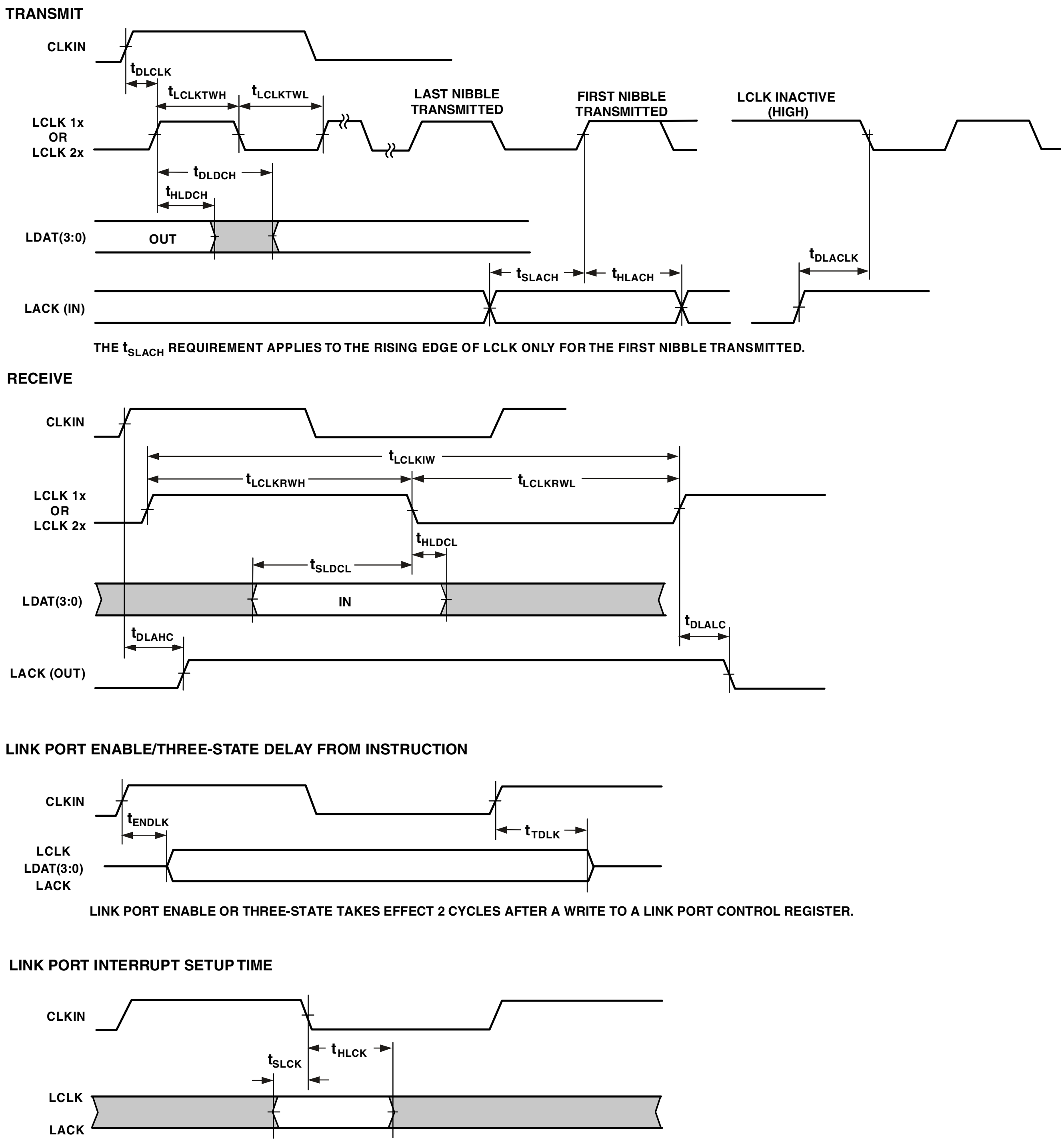

Figure 24. Link Ports—Receive

Serial Ports

For serial ports, see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 35, Figure 26, and Figure 25. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 28. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	6.5		ns
t_{SCLKW}	TCLK/RCLK Width[3]	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.
[3] For ADSP-21060/ADSP-21060C/ADSP-21060LC, specification is 9.5 ns min.

Table 29. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 30. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HDTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

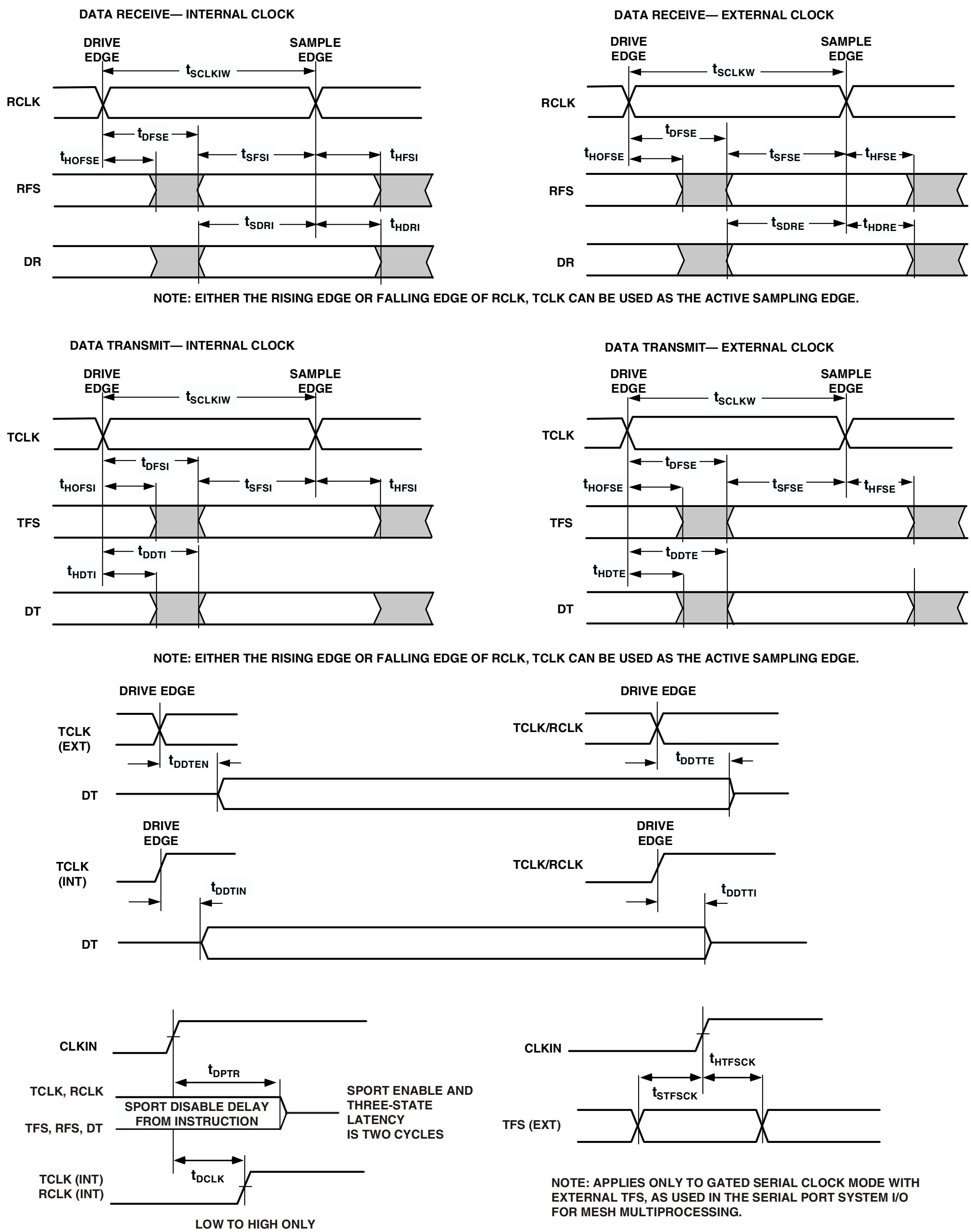

Figure 25. Serial Ports

Output Characteristics (3.3 V)

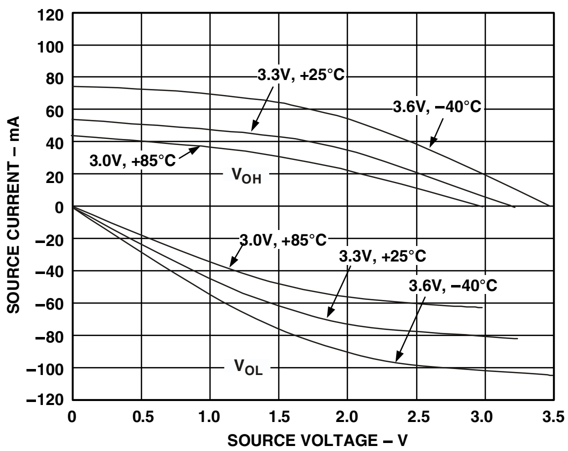

Figure 35. ADSP-21062 Typical Output Drive Currents (V_{DD} = 3.3 V)

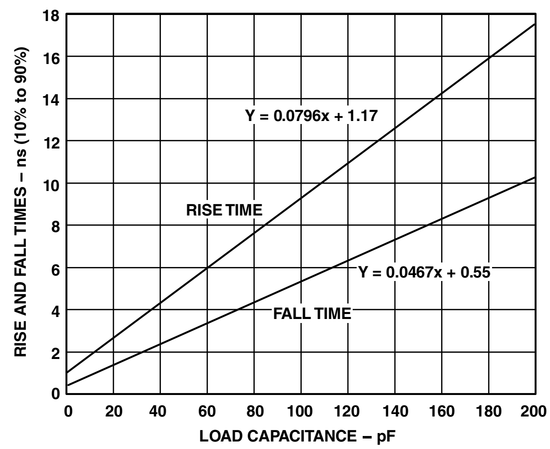

Figure 37. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

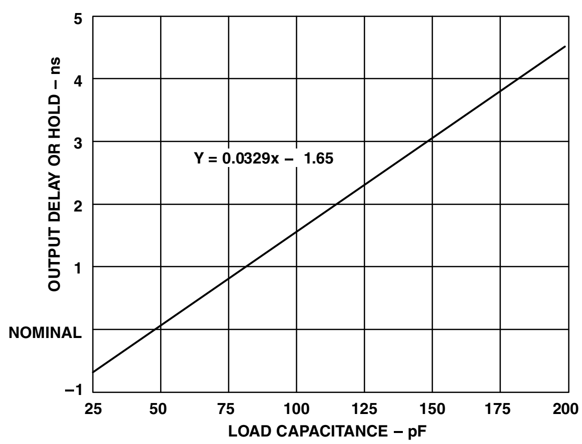

Figure 36. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

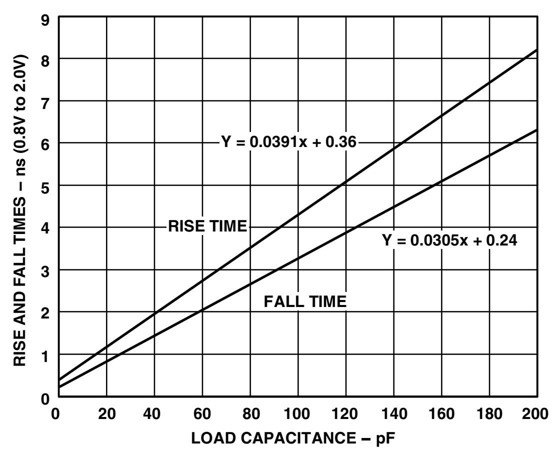

Figure 38. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

225-BALL PBGA BALL CONFIGURATION

Table 40. ADSP-2106x 225-Ball Metric PBGA Ball Assignments (B-225-2)

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
$\overline{\text{BMS}}$	A01	ADDR25	D01	ADDR14	G01	ADDR6	K01	$\overline{\text{EMU}}$	N01
ADDR30	A02	ADDR26	D02	ADDR15	G02	ADDR5	K02	TDO	N02
$\overline{\text{DMAR2}}$	A03	$\overline{\text{MS2}}$	D03	ADDR16	G03	ADDR3	K03	$\overline{\text{IRQ0}}$	N03
DT1	A04	ADDR29	D04	ADDR19	G04	ADDR0	K04	$\overline{\text{IRQ1}}$	N04
RCLK1	A05	$\overline{\text{DMAR1}}$	D05	GND	G05	ICSA	K05	ID2	N05
TCLK0	A06	TFS1	D06	V_{DD}	G06	GND	K06	L5DAT1	N06
RCLK0	A07	$\overline{\text{CPA}}$	D07	V_{DD}	G07	V_{DD}	K07	L4CLK	N07
ADRCLK	A08	$\overline{\text{HBG}}$	D08	V_{DD}	G08	V_{DD}	K08	L3CLK	N08
$\overline{\text{CS}}$	A09	$\overline{\text{DMAG2}}$	D09	V_{DD}	G09	V_{DD}	K09	L3DAT3	N09
CLKIN	A10	$\overline{\text{BR5}}$	D10	V_{DD}	G10	GND	K10	L2DAT0	N10
PAGE	A11	$\overline{\text{BR1}}$	D11	GND	G11	GND	K11	L1ACK	N11
$\overline{\text{BR3}}$	A12	DATA40	D12	DATA22	G12	DATA8	K12	L1DAT3	N12
DATA47	A13	DATA37	D13	DATA25	G13	DATA11	K13	L0DAT3	N13
DATA44	A14	DATA35	D14	DATA24	G14	DATA13	K14	DATA1	N14
DATA42	A15	DATA34	D15	DATA23	G15	DATA14	K15	DATA3	N15
$\overline{\text{MS0}}$	B01	ADDR21	E01	ADDR12	H01	ADDR2	L01	$\overline{\text{TRST}}$	P01
$\overline{\text{SW}}$	B02	ADDR22	E02	ADDR11	H02	ADDR1	L02	TMS	P02
ADDR31	B03	ADDR24	E03	ADDR13	H03	FLAG0	L03	EBOOT	P03
$\overline{\text{HBR}}$	B04	ADDR27	E04	ADDR10	H04	FLAG3	L04	ID0	P04
DR1	B05	GND	E05	GND	H05	RPBA	L05	L5CLK	P05
DT0	B06	GND	E06	V_{DD}	H06	GND	L06	L5DAT3	P06
DR0	B07	GND	E07	V_{DD}	H07	GND	L07	L4DAT0	P07
REDY	B08	GND	E08	V_{DD}	H08	GND	L08	L4DAT3	P08
$\overline{\text{RD}}$	B09	GND	E09	V_{DD}	H09	GND	L09	L3DAT2	P09
ACK	B10	GND	E10	V_{DD}	H10	GND	L10	L2CLK	P10
$\overline{\text{BR6}}$	B11	NC	E11	GND	H11	NC	L11	L2DAT2	P11
$\overline{\text{BR2}}$	B12	DATA33	E12	DATA18	H12	DATA4	L12	L1DAT0	P12
DATA45	B13	DATA30	E13	DATA19	H13	DATA7	L13	L0ACK	P13
DATA43	B14	DATA32	E14	DATA21	H14	DATA9	L14	L0DAT1	P14
DATA39	B15	DATA31	E15	DATA20	H15	DATA10	L15	DATA0	P15
$\overline{\text{MS3}}$	C01	ADDR17	F01	ADDR9	J01	FLAG1	M01	TCK	R01
$\overline{\text{MS1}}$	C02	ADDR18	F02	ADDR8	J02	FLAG2	M02	$\overline{\text{IRQ2}}$	R02
ADDR28	C03	ADDR20	F03	ADDR7	J03	TIMEXP	M03	$\overline{\text{RESET}}$	R03
$\overline{\text{SBTS}}$	C04	ADDR23	F04	ADDR4	J04	TDI	M04	ID1	R04
TCLK1	C05	GND	F05	GND	J05	LBOOT	M05	L5DAT0	R05
RFS1	C06	GND	F06	V_{DD}	J06	L5ACK	M06	L4ACK	R06
TFS0	C07	V_{DD}	F07	V_{DD}	J07	L5DAT2	M07	L4DAT1	R07
RFS0	C08	V_{DD}	F08	V_{DD}	J08	L4DAT2	M08	L3ACK	R08
$\overline{\text{WR}}$	C09	V_{DD}	F09	V_{DD}	J09	L3DAT0	M09	L3DAT1	R09
$\overline{\text{DMAG1}}$	C10	GND	F10	V_{DD}	J10	L2DAT3	M10	L2ACK	R10
$\overline{\text{BR4}}$	C11	GND	F11	GND	J11	L1DAT1	M11	L2DAT1	R11
DATA46	C12	DATA29	F12	DATA12	J12	L0DAT0	M12	L1CLK	R12
DATA41	C13	DATA26	F13	DATA15	J13	DATA2	M13	L1DAT2	R13
DATA38	C14	DATA28	F14	DATA16	J14	DATA5	M14	L0CLK	R14
DATA36	C15	DATA27	F15	DATA17	J15	DATA6	M15	L0DAT2	R15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DATA42	DATA44	DATA47	$\overline{BR3}$	PAGE	CLKIN	$\overline{CS}$	ADRCLK	RCLK0	TCLK0	RCLK1	DT1	$\overline{DMAR2}$	ADDR30	$\overline{BMS}$	A
DATA39	DATA43	DATA45	$\overline{BR2}$	$\overline{BR6}$	ACK	$\overline{RD}$	REDY	DR0	DT0	DR1	$\overline{HBR}$	ADDR31	$\overline{SW}$	$\overline{MS0}$	B
DATA36	DATA38	DATA41	DATA46	$\overline{BR4}$	$\overline{DMAG1}$	$\overline{WR}$	RFS0	TFS0	RFS1	TCLK1	$\overline{SBTS}$	ADDR28	$\overline{MS1}$	$\overline{MS3}$	C
DATA34	DATA35	DATA37	DATA40	$\overline{BR1}$	$\overline{BR5}$	$\overline{DMAG2}$	$\overline{HBG}$	$\overline{CPA}$	TFS1	$\overline{DMAR1}$	ADDR29	$\overline{MS2}$	ADDR26	ADDR25	D
DATA31	DATA32	DATA30	DATA33	NC	GND	GND	GND	GND	GND	GND	ADDR27	ADDR24	ADDR22	ADDR21	E
DATA27	DATA28	DATA26	DATA29	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	GND	ADDR23	ADDR20	ADDR18	ADDR17	F
DATA23	DATA24	DATA25	DATA22	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR19	ADDR16	ADDR15	ADDR14	G
DATA20	DATA21	DATA19	DATA18	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR10	ADDR13	ADDR11	ADDR12	H
DATA17	DATA16	DATA15	DATA12	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR4	ADDR7	ADDR8	ADDR9	J
DATA14	DATA13	DATA11	DATA8	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	ICSA	ADDR0	ADDR3	ADDR5	ADDR6	K
DATA10	DATA9	DATA7	DATA4	NC	GND	GND	GND	GND	GND	RPBA	FLAG3	FLAG0	ADDR1	ADDR2	L
DATA6	DATA5	DATA2	L0DAT0	L1DAT1	L2DAT3	L3DAT0	L4DAT2	L5DAT2	L5ACK	LBOOT	TDI	TIMEXP	FLAG2	FLAG1	M
DATA3	DATA1	L0DAT3	L1DAT3	L1ACK	L2DAT0	L3DAT3	L3CLK	L4CLK	L5DAT1	ID2	$\overline{IRQ1}$	$\overline{IRQ0}$	TDO	$\overline{EMU}$	N
DATA0	L0DAT1	L0ACK	L1DAT0	L2DAT2	L2CLK	L3DAT2	L4DAT3	L4DAT0	L5DAT3	L5CLK	ID0	EBOOT	TMS	$\overline{TRST}$	P
L0DAT2	L0CLK	L1DAT2	L1CLK	L2DAT1	L2ACK	L3DAT1	L3ACK	L4DAT1	L4ACK	L5DAT0	ID1	$\overline{RESET}$	$\overline{IRQ2}$	TCK	R

Figure 39. ADSP-21060/ADSP-21062 PBGA Ball Assignments (Top View, Summary)

Table 42. ADSP-21060CW/21060LCW CQFP Pin Assignments (QS-240-1A, QS-240-1B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	DATA29	41	$\overline{\text{DMAG2}}$	81	ADDR28	121	ADDR5	161	GND	201
DATA0	2	GND	42	ACK	82	$\overline{\text{BMS}}$	122	GND	162	V_{DD}	202
DATA1	3	DATA30	43	CLKIN	83	$\overline{\text{SW}}$	123	ADDR4	163	L4ACK	203
DATA2	4	DATA31	44	GND	84	$\overline{\text{MS0}}$	124	ADDR3	164	L4CLK	204
V_{DD}	5	DATA32	45	V_{DD}	85	$\overline{\text{MS1}}$	125	ADDR2	165	L4DAT0	205
DATA3	6	GND	46	GND	86	$\overline{\text{MS2}}$	126	V_{DD}	166	L4DAT1	206
DATA4	7	V_{DD}	47	$\overline{\text{WR}}$	87	$\overline{\text{MS3}}$	127	ADDR1	167	L4DAT2	207
DATA5	8	V_{DD}	48	$\overline{\text{RD}}$	88	GND	128	ADDR0	168	L4DAT3	208
GND	9	DATA33	49	$\overline{\text{CS}}$	89	ADDR27	129	GND	169	GND	209
DATA6	10	DATA34	50	$\overline{\text{HBG}}$	90	ADDR26	130	FLAG0	170	L3ACK	210
DATA7	11	DATA35	51	REDY	91	ADDR25	131	FLAG1	171	L3CLK	211
DATA8	12	NC	52	ADRCLK	92	V_{DD}	132	FLAG2	172	L3DAT0	212
V_{DD}	13	GND	53	GND	93	GND	133	FLAG3	173	L3DAT1	213
DATA9	14	DATA36	54	V_{DD}	94	V_{DD}	134	ICSA	174	L3DAT2	214
DATA10	15	DATA37	55	V_{DD}	95	ADDR24	135	$\overline{\text{EMU}}$	175	L3DAT3	215
DATA11	16	DATA38	56	RFS0	96	ADDR23	136	TIMEXP	176	V_{DD}	216
GND	17	V_{DD}	57	RCLK0	97	ADDR22	137	TDO	177	NC	217
DATA12	18	DATA39	58	DR0	98	GND	138	V_{DD}	178	L2ACK	218
DATA13	19	DATA40	59	TFS0	99	ADDR21	139	$\overline{\text{TRST}}$	179	L2CLK	219
DATA14	20	DATA41	60	TCLK0	100	ADDR20	140	TDI	180	L2DAT0	220
V_{DD}	21	GND	61	DT0	101	ADDR19	141	TMS	181	L2DAT1	221
DATA15	22	DATA42	62	$\overline{\text{CPA}}$	102	V_{DD}	142	TCK	182	L2DAT2	222
DATA16	23	DATA43	63	GND	103	V_{DD}	143	$\overline{\text{IRQ0}}$	183	L2DAT3	223
DATA17	24	DATA44	64	RFS1	104	ADDR18	144	$\overline{\text{IRQ1}}$	184	V_{DD}	224
GND	25	V_{DD}	65	RCLK1	105	ADDR17	145	$\overline{\text{IRQ2}}$	185	GND	225
DATA18	26	DATA45	66	DR1	106	ADDR16	146	EBOOT	186	GND	226
DATA19	27	DATA46	67	TFS1	107	GND	147	$\overline{\text{RESET}}$	187	L1ACK	227
DATA20	28	DATA47	68	TCLK1	108	ADDR15	148	RPBA	188	L1CLK	228
V_{DD}	29	GND	69	DT1	109	ADDR14	149	LBOOT	189	L1DAT0	229
DATA21	30	V_{DD}	70	$\overline{\text{HBR}}$	110	V_{DD}	150	ID0	190	L1DAT1	230
DATA22	31	GND	71	$\overline{\text{DMAR1}}$	111	ADDR13	151	ID1	191	L1DAT2	231
DATA23	32	$\overline{\text{BR1}}$	72	$\overline{\text{DMAR2}}$	112	ADDR12	152	ID2	192	L1DAT3	232
GND	33	$\overline{\text{BR2}}$	73	$\overline{\text{SBTS}}$	113	ADDR11	153	GND	193	V_{DD}	233
DATA24	34	$\overline{\text{BR3}}$	74	GND	114	GND	154	L5ACK	194	L0ACK	234
DATA25	35	$\overline{\text{BR4}}$	75	ADDR31	115	ADDR10	155	L5CLK	195	L0CLK	235
DATA26	36	$\overline{\text{BR5}}$	76	ADDR30	116	ADDR9	156	L5DAT0	196	L0DAT0	236
V_{DD}	37	$\overline{\text{BR6}}$	77	ADDR29	117	ADDR8	157	L5DAT1	197	L0DAT1	237
V_{DD}	38	V_{DD}	78	V_{DD}	118	V_{DD}	158	L5DAT2	198	L0DAT2	238
DATA27	39	PAGE	79	V_{DD}	119	ADDR7	159	L5DAT3	199	L0DAT3	239
DATA28	40	$\overline{\text{DMAG1}}$	80	GND	120	ADDR6	160	V_{DD}	200	GND	240

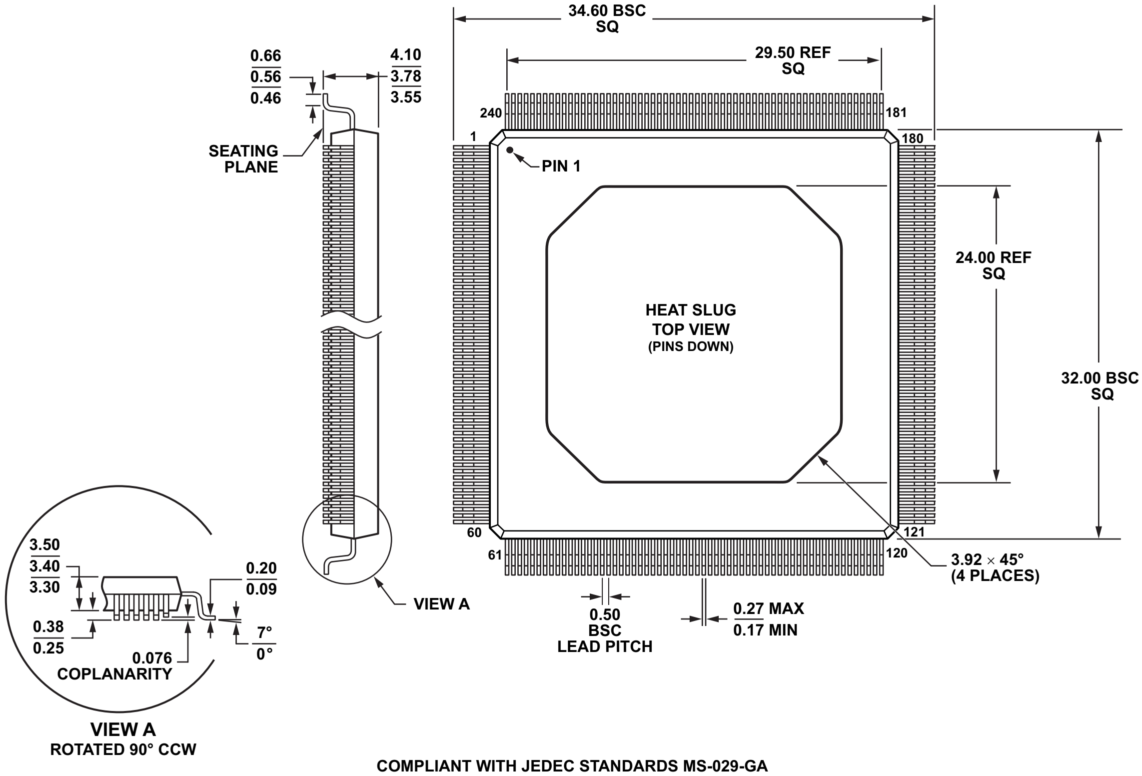

Figure 41. 240-Lead Metric Quad Flat Package, Thermally Enhanced "PowerQuad" [MQFP_PQ4]
(SP-240-2)
Dimensions shown in millimeters

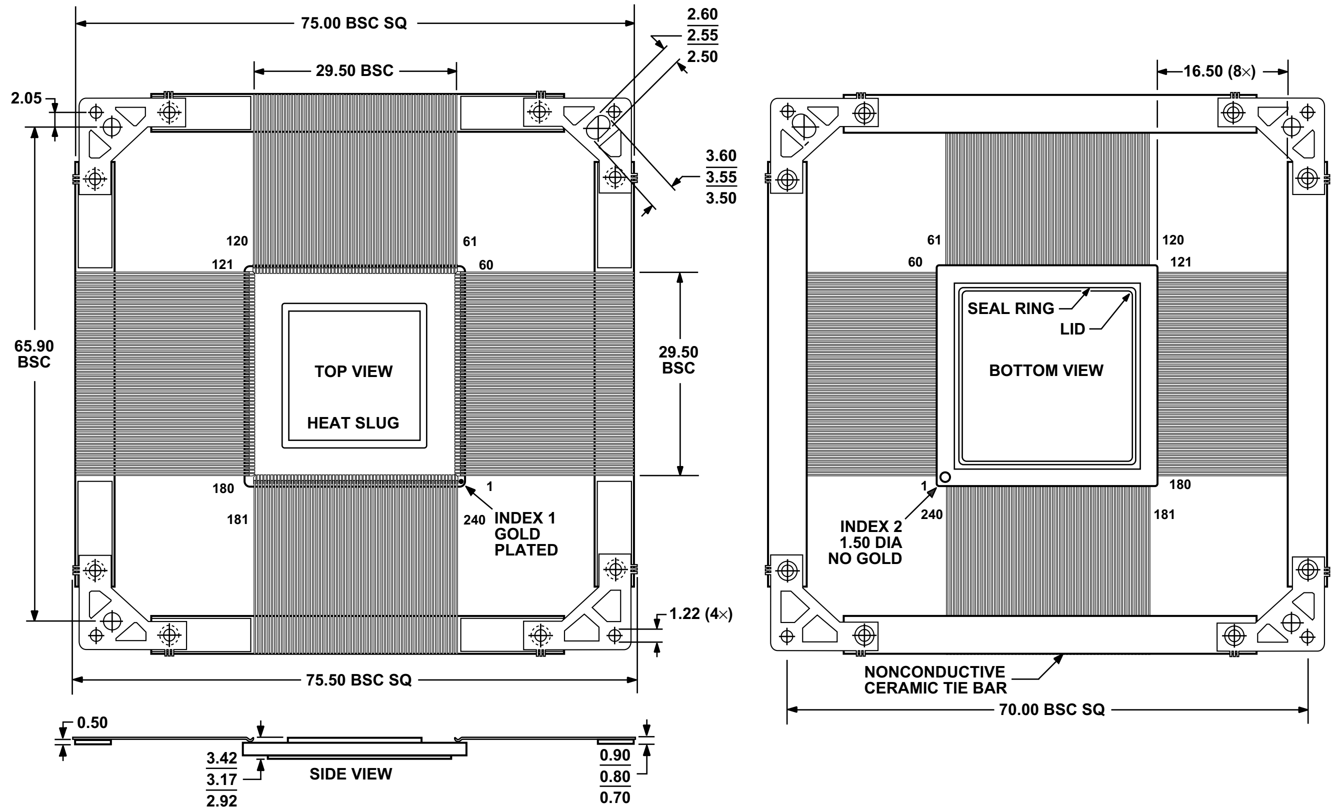

Figure 43. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Down [CQFP]
(QS-240-2B)
Dimensions shown in millimeters