Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	33MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21060lksz-133

CONTENTS

REVISION HISTORY

3/13—Rev. G to Rev. H

Updated Development Tools 8

Corrected the power dissipation equation from $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$ to $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$
External Power Dissipation (3.3 V) 20

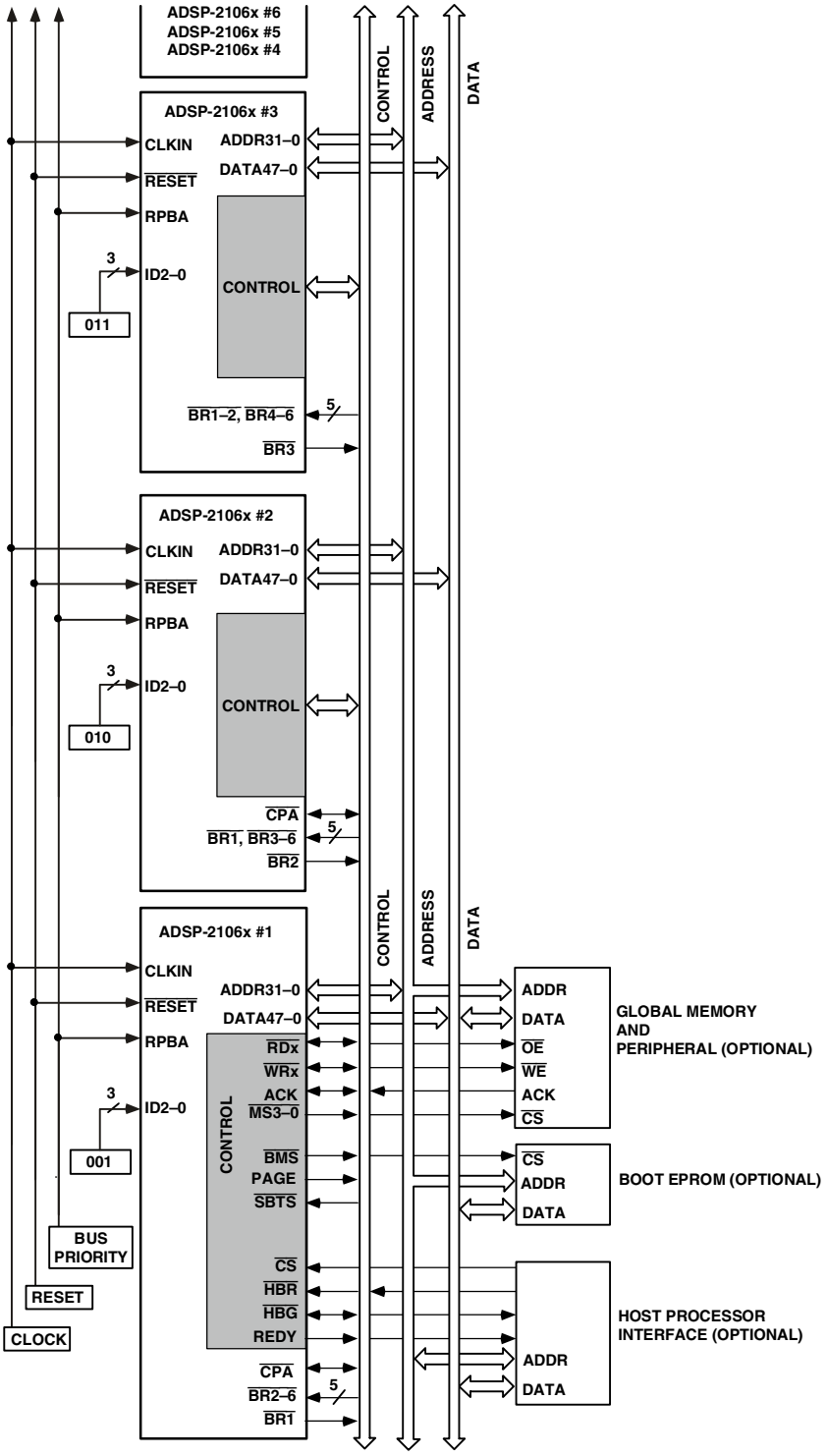

Figure 3. Shared Memory Multiprocessing System

DMA Controller

The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-2106x's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Multiprocessing

The ADSP-2106x offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240M bytes/s over the link ports or external port. Broadcast writes allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

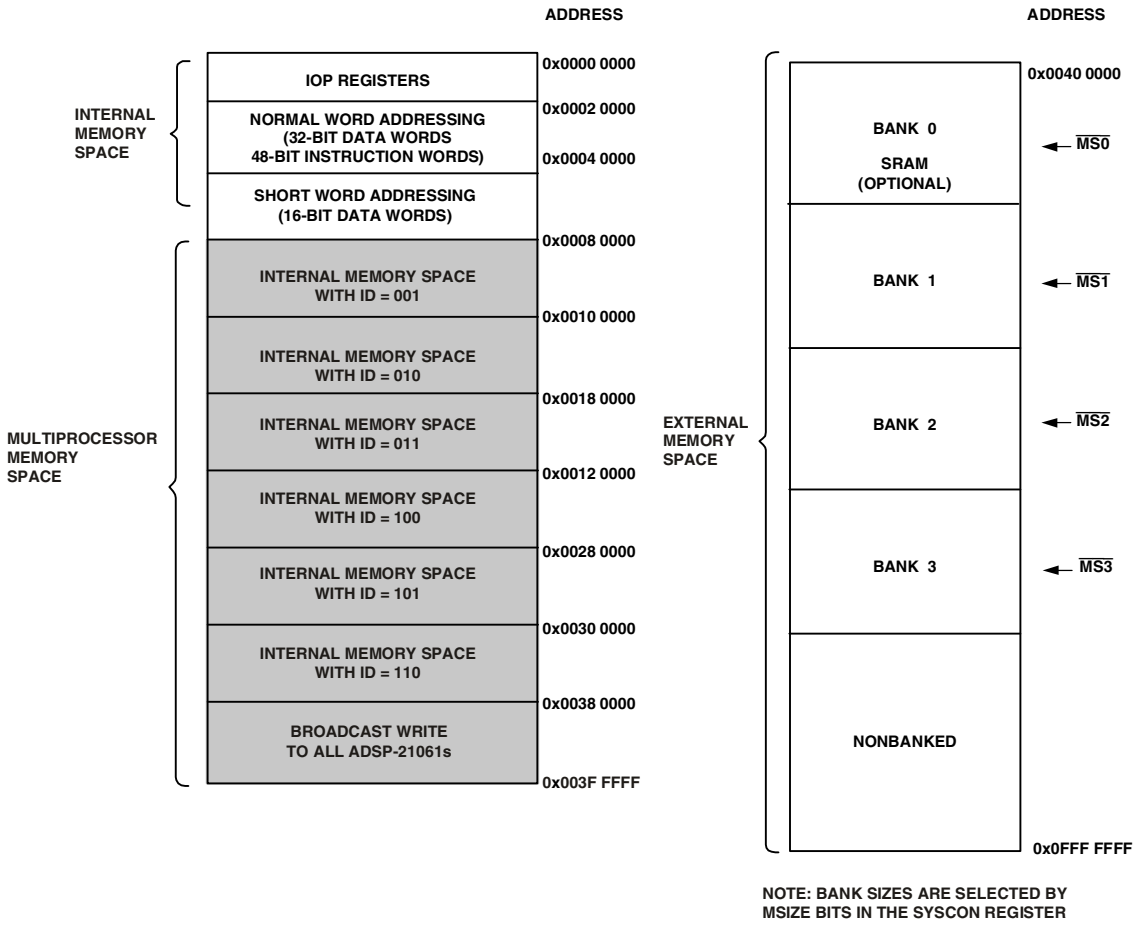

Figure 4. Memory Map

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2106x architecture and functionality. For detailed information on the ADSP-21000 family core architecture and instruction set, refer to the *ADSP-2106x SHARC User's Manual*, Revision 2.1.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where% is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	745	mA
	t_{CK} = 25 ns, V_{DD} = Max	850	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	575	mA
	t_{CK} = 25 ns, V_{DD} = Max	670	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	340	mA
	t_{CK} = 25 ns, V_{DD} = Max	390	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	200	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106x state during execution of IDLE instruction.

ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade Min	A Grade Max	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	3.15	3.45	3.15	3.45	3.15	3.45	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

Clock Input

Table 9. Clock Input

Parameter		ADSP-21060 ADSP-21062 40 MHz, 5 V Min	ADSP-21060 ADSP-21062 40 MHz, 5 V Max	ADSP-21060 ADSP-21062 33 MHz, 5 V Min	ADSP-21060 ADSP-21062 33 MHz, 5 V Max	ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Min	ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Max	ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Min	ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	25	100	30	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		8.75		8.75[1]		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

[1] For the ADSP-21060LC, this specification is 9.5 ns min.

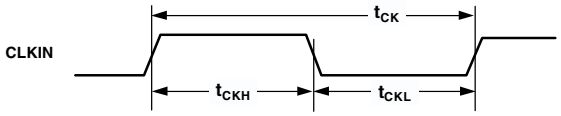

Figure 9. Clock Input

Reset

Table 10. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

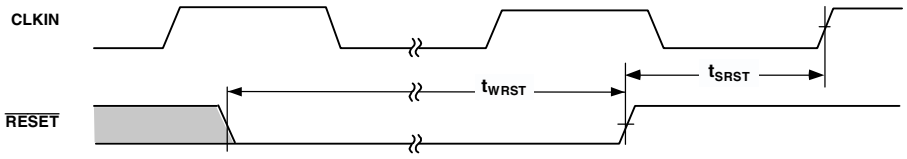

Figure 10. Reset

Interrupts

Table 11. Interrupts

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulse Width[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

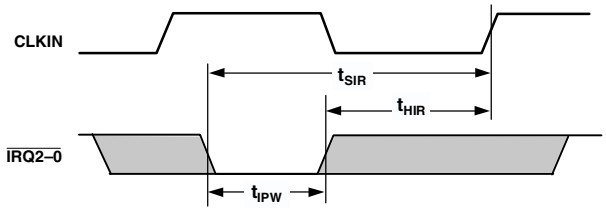

Figure 11. Interrupts

Timer

Table 12. Timer

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

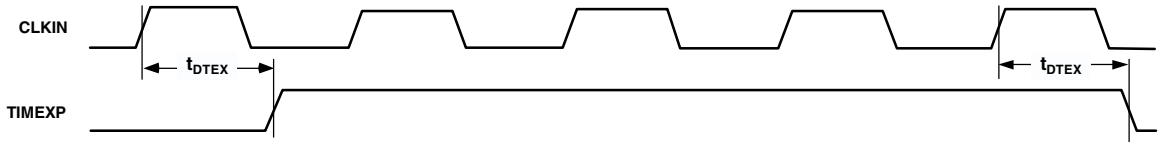

Figure 12. Timer

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 14. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 48 for the calculation of hold times given capacitive and dc loads.
[4] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

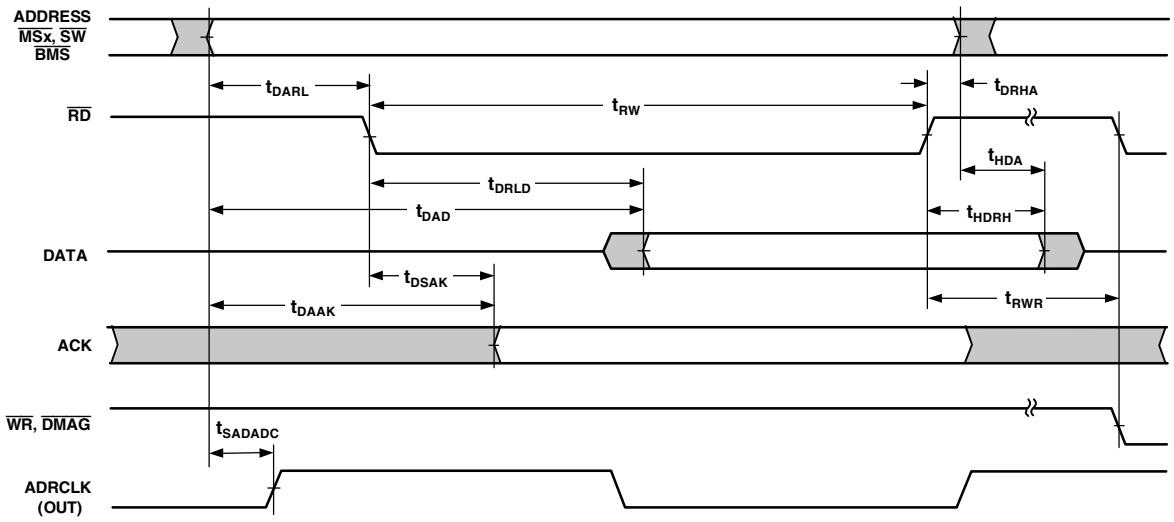

Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 15. Memory Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DAWH}	Address Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		ns
t_{DAWL}	Address Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	12 + 9DT/16 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	7 + DT/2 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.5 + DT/16 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

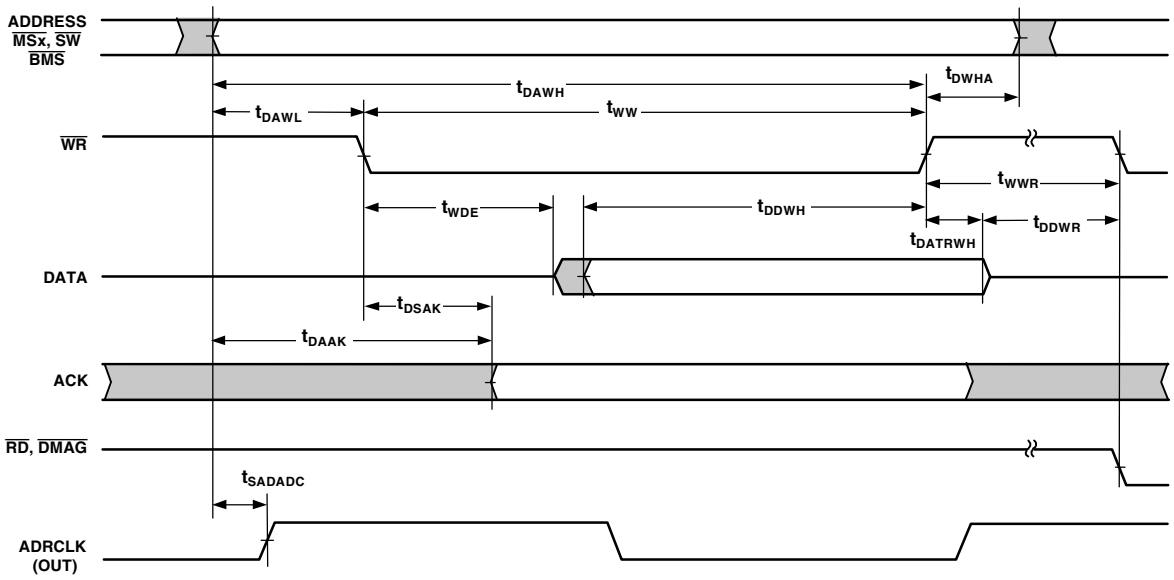

Figure 15. Memory Write—Bus Master

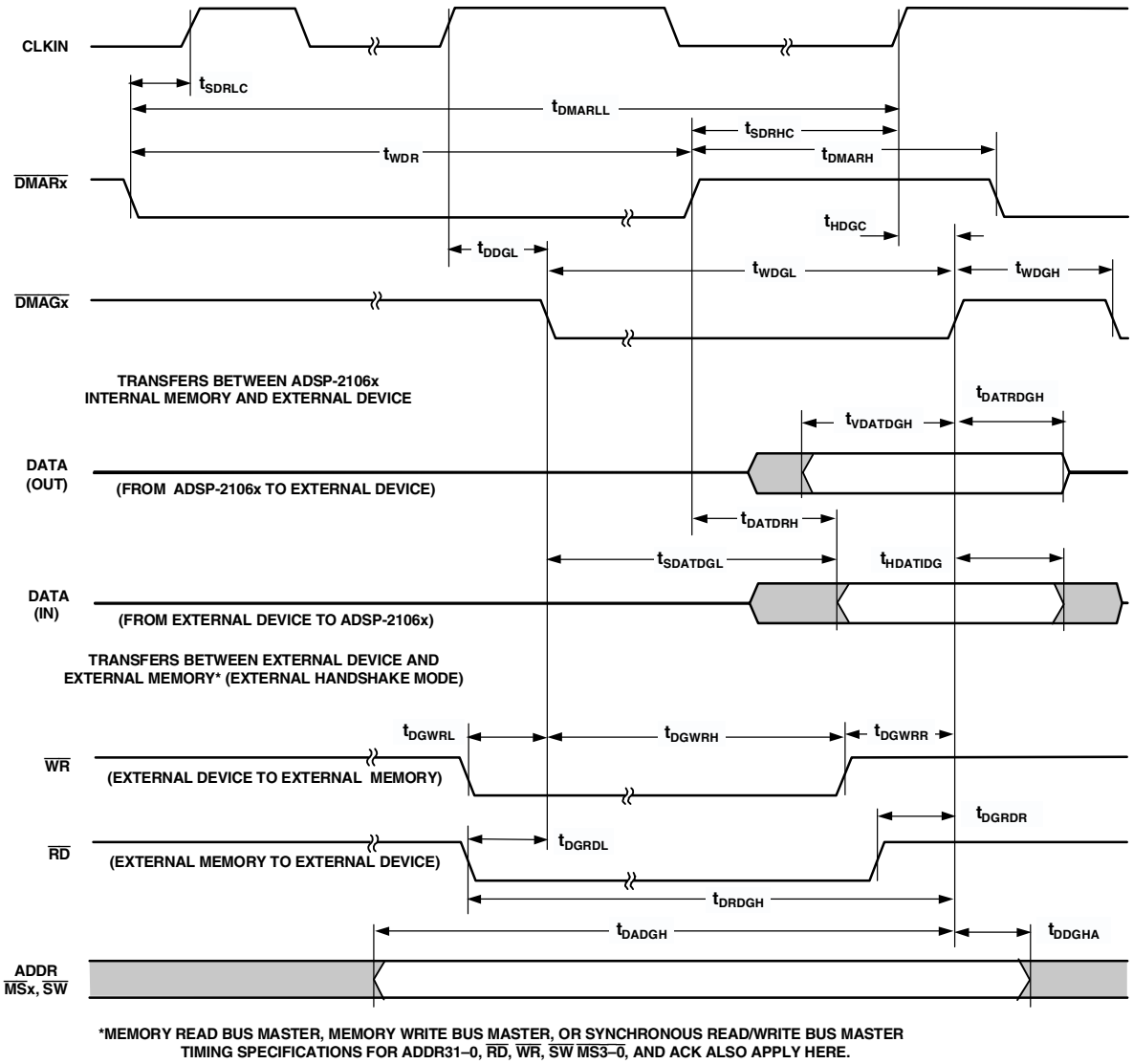

Figure 23. DMA Handshake

Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLCK}	LACK/LCLK Setup Before CLKIN Low[1]	10		10		ns
t_{HLCK}	LACK/LCLK Hold After CLKIN Low[1]	2		2		ns

[1] Only required for interrupt recognition in the current cycle.

Link Ports —2 × CLK Speed Operation

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$Setup\ Skew = t_{LCLKTWH}\ \text{min} - t_{DLDCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$Hold\ Skew = t_{LCLKTWL}\ \text{min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

Note that link port transfers at 2× CLK speed at 40 MHz (t_{CK} = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz (t_{CK} = 30 ns) work as specified.

Table 26. Link Ports—Receive

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLDCL}	Data Setup Before LCLK Low	2.5		2.25		ns
t_{HLDCL}	Data Hold After LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2× Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low[1]	4.5		5.25		ns
$t_{LCLKRWH}$	LCLK Width High[2]	4.25		4		ns
Switching Characteristics						
t_{DLAHC}	LACK High Delay After CLKIN High[3]	18 + DT/2	28.5 + DT/2	18 + DT/2	29.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High[4]	6	16	6	16	ns

[1] For ADSP-21060L, specification is 5 ns min.
[2] For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.
[3] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[4] For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

Table 27. Link Ports—Transmit

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLACH}	LACK Setup Before LCLK High	19		19		ns
t_{HLACH}	LACK Hold After LCLK High	–6.75		–6.5		ns
Switching Characteristics						
t_{DLCLK}	Data Delay After CLKIN		8		8	ns
t_{DLDCH}	Data Delay After LCLK High[1]		2.25		2.25	ns
t_{HLDCH}	Data Hold After LCLK High[2]	–2.0		–2		ns
$t_{LCLKTWL}$	LCLK Width Low[3]	$(t_{CK}/4) - 1$	$(t_{CK}/4) + 1.25$	$(t_{CK}/4) - 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High[4]	$(t_{CK}/4) - 1.25$	$(t_{CK}/4) + 1$	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$(t_{CK}/4) + 9$	$(3 \times t_{CK}/4) + 16.5$	$(t_{CK}/4) + 9$	$(3 \times t_{CK}/4) + 16.5$	ns

[1] For ADSP-21060/ADSP-21060C, specification is 2.5 ns max.
[2] For ADSP-21062L, specification is –2.25 ns min.
[3] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C/ADSP-21062L, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1.5$ ns max.
[4] For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C, specification is $(t_{CK}/4) - 1.5$ ns min, $(t_{CK}/4) + 1$ ns max.

Table 32. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –2.5	$0.5t_{SCLK}$+2.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 0.5_{TSCLK} – 2 ns min, $0.5t_{SCLK}$ + 2 ns max.

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1, 3]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1, 4]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3 DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 3.5 ns min; for ADSP-21062 specification is 4.5 ns min.
[3] For ADSP-21062L, specification is 16 ns max.
[4] For ADSP-21062L, specification is 7.5 ns max.

Table 34. Serial Ports—GATED SCLK with External TFS (Mesh Multiprocessing)[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{STFSCK}	TFS Setup Before CLKIN	4		ns
t_{HTFSCK}	TFS Hold After CLKIN		$t_{CK}/2$	ns

[1] Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1, 2]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1, 3]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.
[2] For ADSP-21062/ADSP-21062L, specification is 12.75 ns max; for ADSP-21060L/ADSP-21060LC, specification is 12.8 ns max.
[3] For ADSP-21060/ADSP-21060C, specification is 3 ns min.

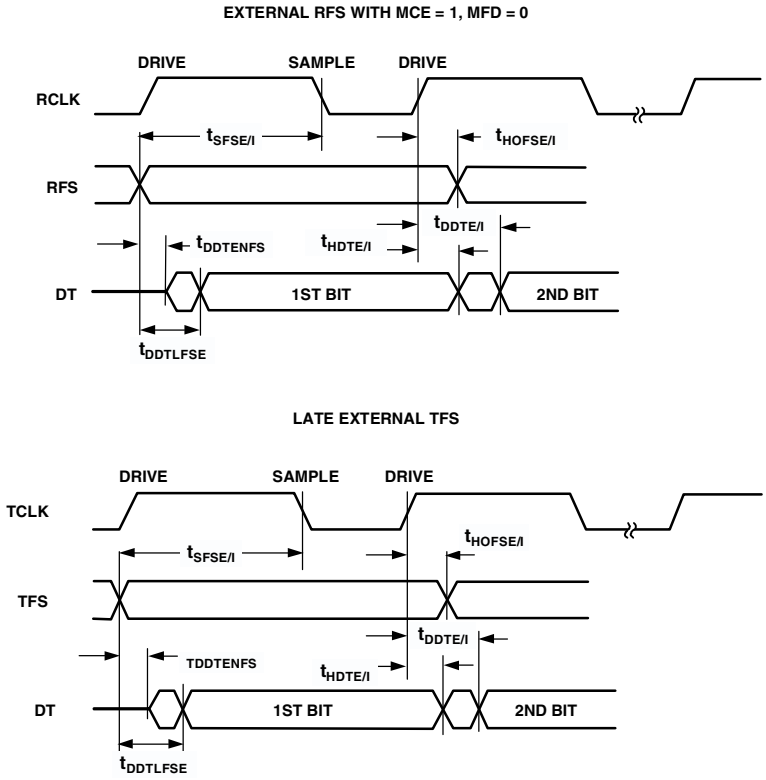

Figure 26. Serial Ports—External Late Frame Sync

TEST CONDITIONS

For the ac signal specifications (timing parameters), see Timing Specifications on Page 21. These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 28.

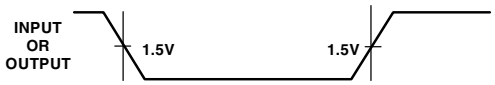

Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

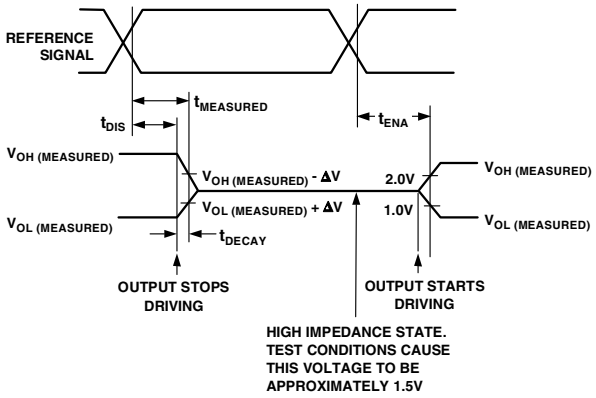

Figure 29. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 29). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 30). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 32, Figure 33, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 34 and Figure 36 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 32, Figure 33, Figure 37, and Figure 38 may not be linear outside the ranges shown.

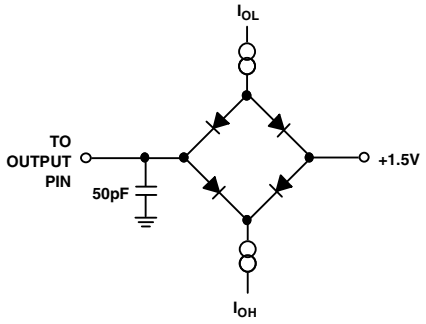

Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Output Drive Characteristics

Figure 31 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

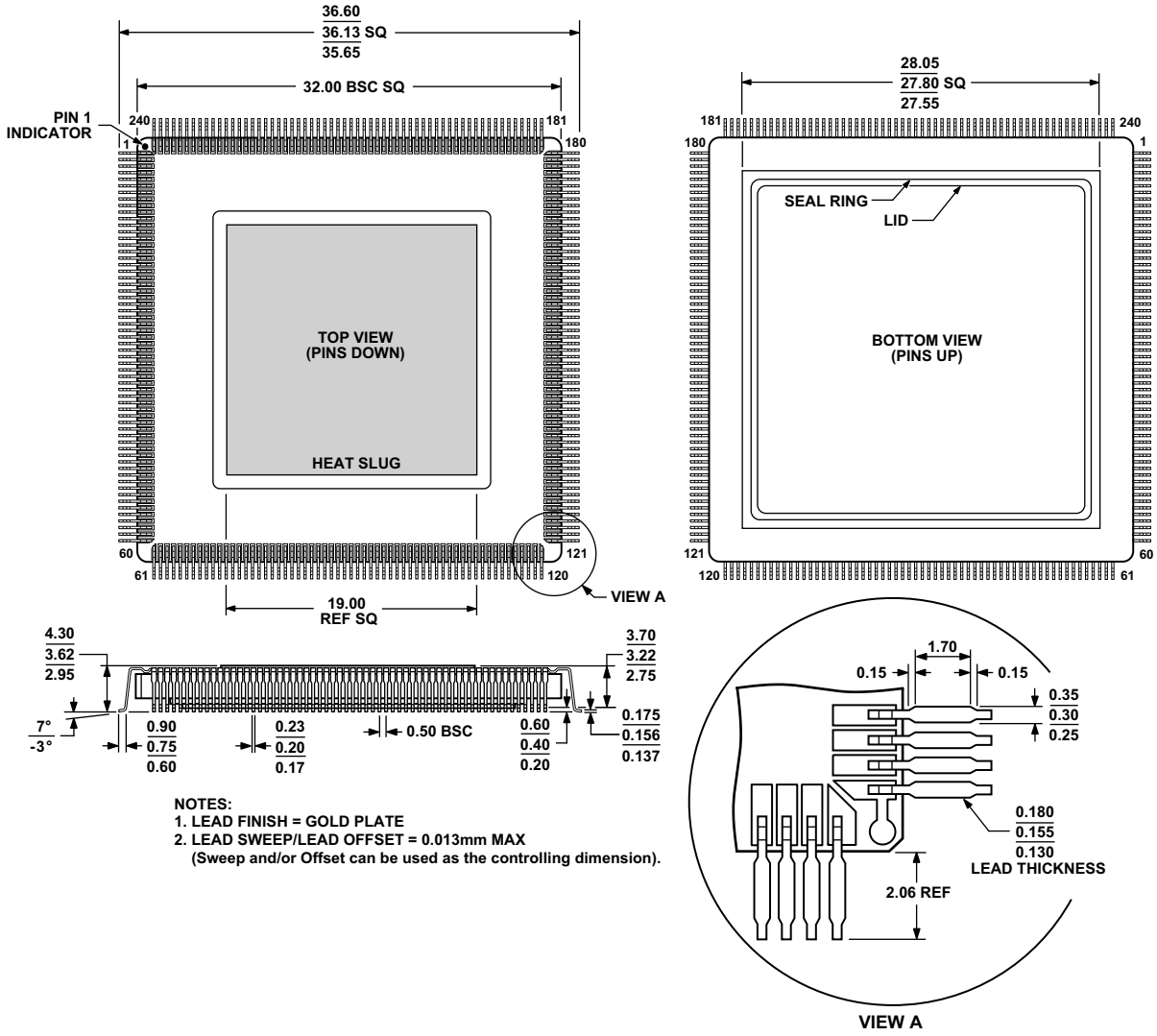

Figure 42. 240-Lead Ceramic Quad Flat Package, Heat Slug Up [CQFP]
(QS-240-2A)
Dimensions shown in millimeters

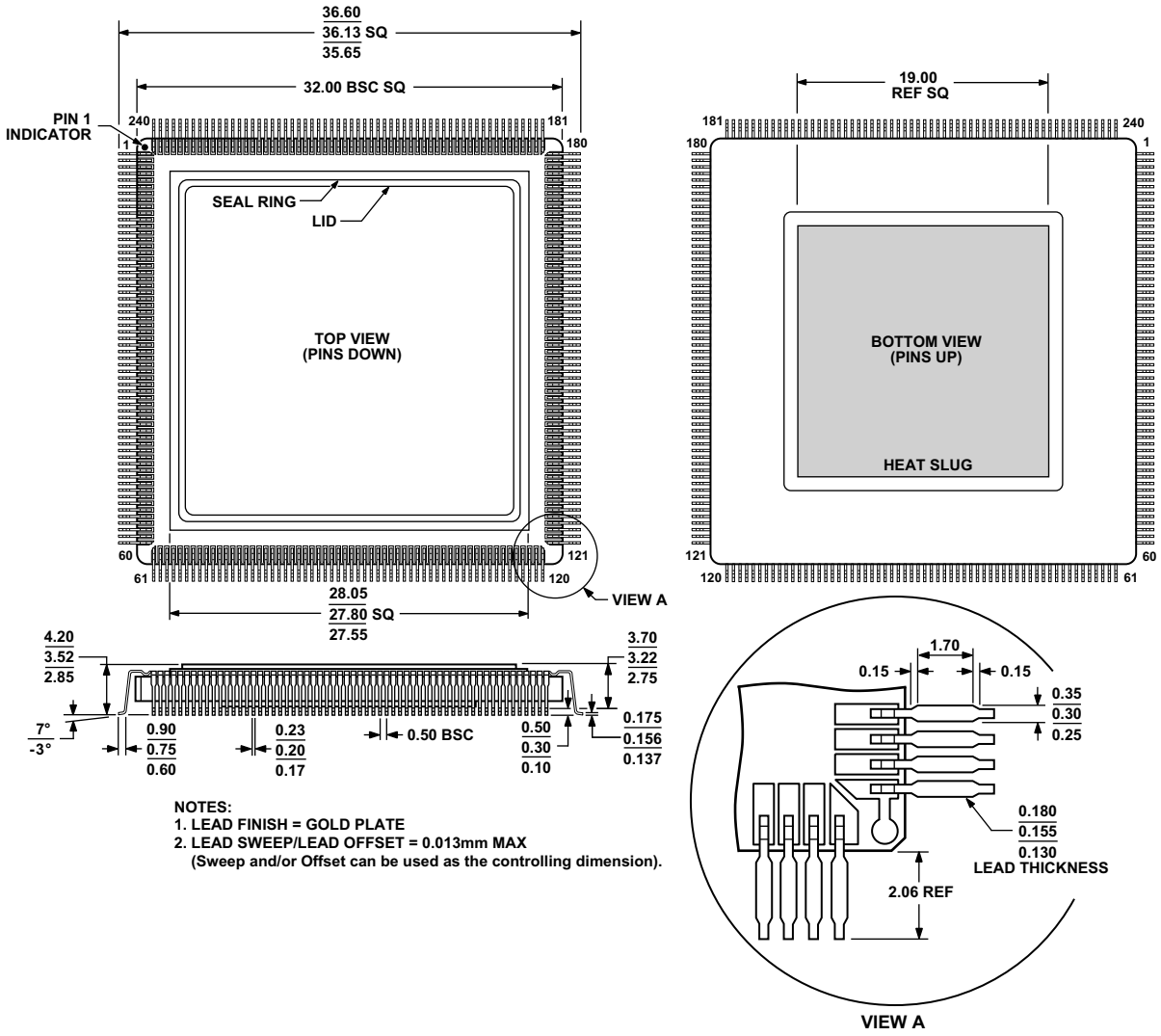

Figure 44. 240-Lead Ceramic Quad Flat Package, Heat Slug Down [CQFP]
(QS-240-1A)
Dimensions shown in millimeters