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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Floating Point |
| Interface | Host Interface, Link Port, Serial Port |
| Clock Rate | 40MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 256kB |
| Voltage - I/O | 5.00V |
| Voltage - Core | 5.00V |
| Operating Temperature | -40°C ~ 100°C (TC) |
| Mounting Type | Surface Mount |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-MQFP-EP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-21062cs-160 |

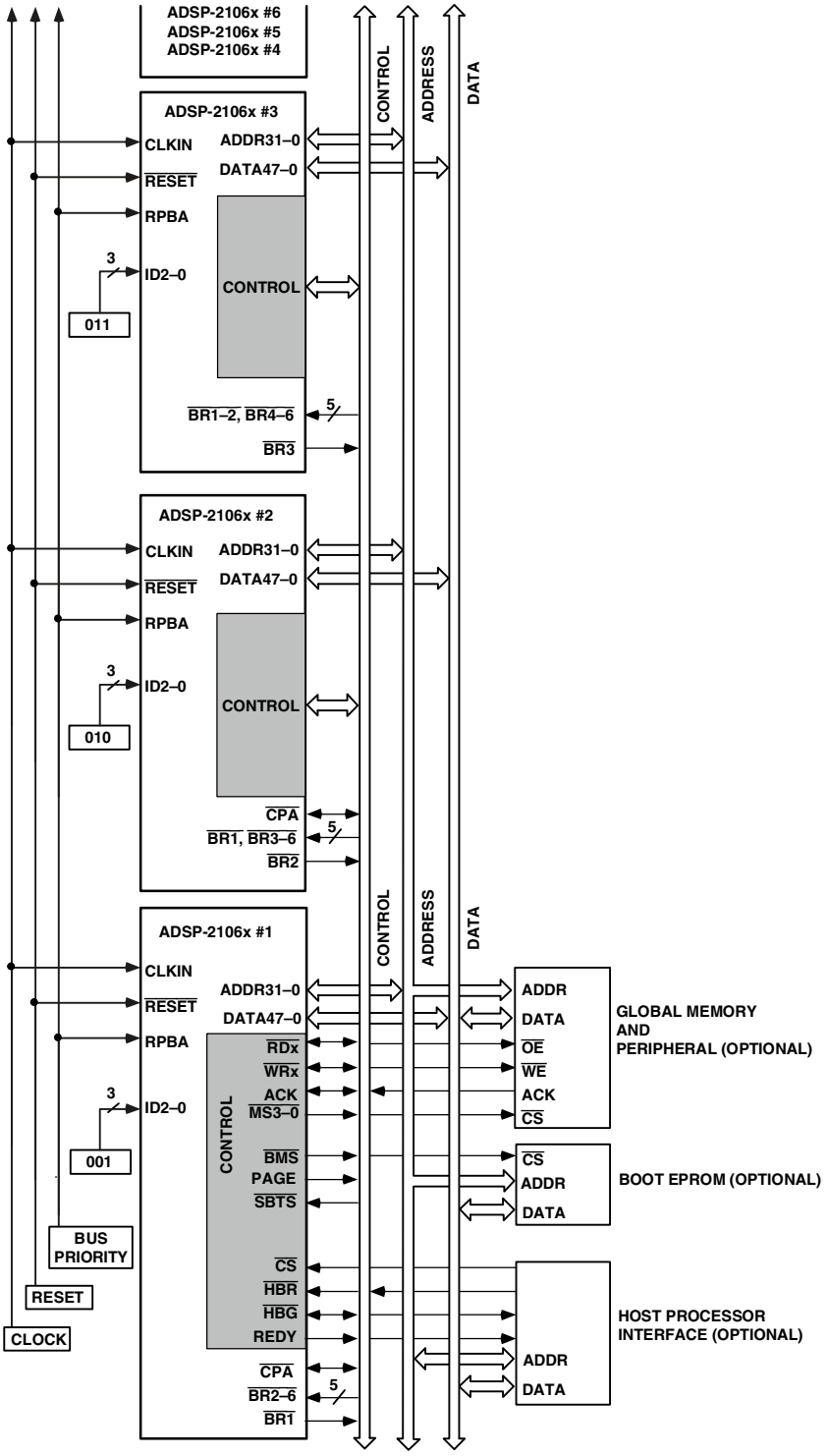



*Figure 3. Shared Memory Multiprocessing System*

### DMA Controller

The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-2106x's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR1–2}}$, $\overline{\text{DMAG1–2}}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

### Multiprocessing

The ADSP-2106x offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240M bytes/s over the link ports or external port. Broadcast writes allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

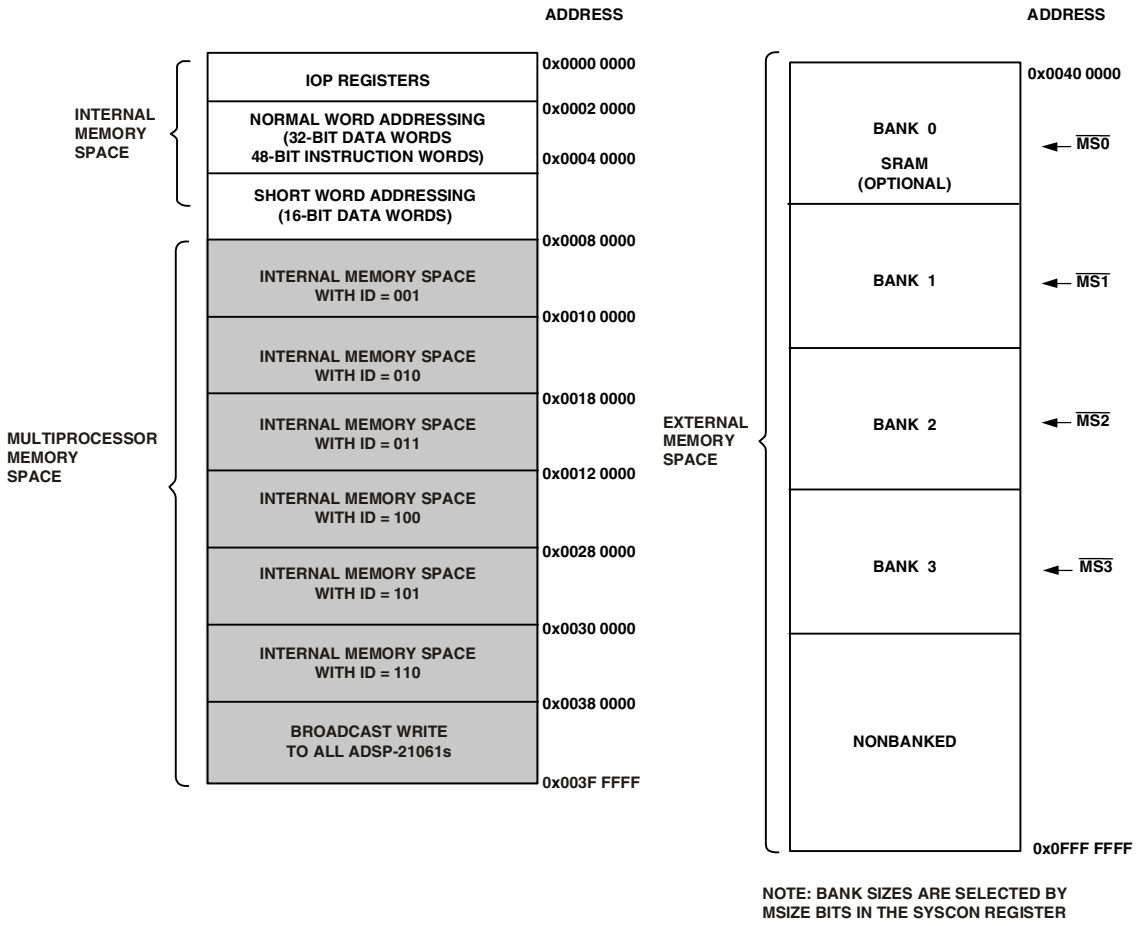



*Figure 4. Memory Map*

# PIN FUNCTION DESCRIPTIONS

The ADSP-2106x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31–0, DATA47–0, FLAG3–0, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, LxDAT3–0, LxCLK, LxACK, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

**Table 3. Pin Descriptions**

| Pin | Type | Function |
|---|---|---|
| ADDR31–0 | I/O/T | **External Bus Address.** The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers. |
| DATA47–0 | I/O/T | **External Bus Data.** The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47–8 of the bus. 16-bit short word data is transferred over bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23–16. Pull-up resistors on unused DATA pins are not necessary. |
| $\overline{\text{MS3–0}}$ | O/T | **Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The $\overline{\text{MS3–0}}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{\text{MS3–0}}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{\text{MS0}}$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{\text{MS3–0}}$ lines are output by the bus master. |
| $\overline{\text{RD}}$ | I/O/T | **Memory Read Strobe.** This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert $\overline{\text{RD}}$ to read from the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-2106xs. |
| $\overline{\text{WR}}$ | I/O/T | **Memory Write Strobe.** This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-2106xs. |
| PAGE | O/T | **DRAM Page Boundary.** The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master |
| ADRCLK | O/T | **Clock Output Reference.** In a multiprocessing system, ADRCLK is output by the bus master. |
| $\overline{\text{SW}}$ | I/O/T | **Synchronous Write Select.** This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s). |

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

## TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE® Emulator uses the IEEE 1149.1JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TRST, TDI, TDO, EMU, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

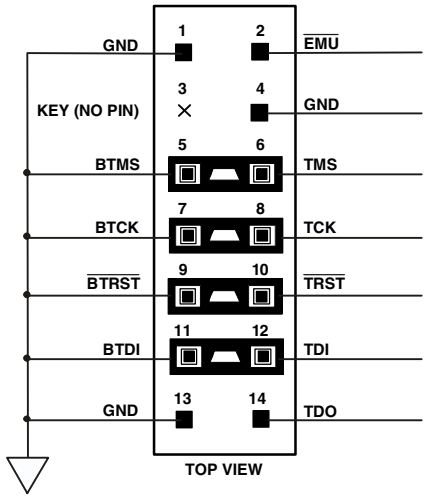



*Figure 5. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)*

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, BTRST, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers on the Bxxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie BTRST to GND and tie or pull up BTCK to $V_{DD}$. The TRST pin must be asserted (pulsed low) after power-up (through BTRST on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 4.

**Table 4. Core Instruction Rate/CLKIN Ratio Selection**

| Signal | Termination |
|---|---|
| TMS | Driven Through 22 Ω Resistor (16 mA Driver) |
| TCK | Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver) |
| TRST[1] | Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled-Up by On-Chip 20 kΩ Resistor) |
| TDI | Driven by 22 Ω Resistor (16 mA Driver) |
| TDO | One TTL Load, Split Termination (160/220) |
| CLKIN | One TTL Load, Split Termination (160/220) |
| EMU | Active Low 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP) |

[1] TRST is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and EMU should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-2106xs (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x User's Manual*, Revision 2.1.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, EMU and TRST are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference*.

# ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

## OPERATING CONDITIONS (3.3 V)

| Parameter | Description | A Grade Min | A Grade Max | C Grade Min | C Grade Max | K Grade Min | K Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.15 | 3.45 | 3.15 | 3.45 | 3.15 | 3.45 | V |
| $T_{CASE}$ | Case Operating Temperature | –40 | +85 | –40 | +100 | –40 | +85 | °C |
| $V_{IH}1$[1] | High Level Input Voltage @ $V_{DD}$ = Max | 2.0 | $V_{DD}$ + 0.5 | 2.0 | $V_{DD}$ + 0.5 | 2.0 | $V_{DD}$ + 0.5 | V |
| $V_{IH}2$[2] | High Level Input Voltage @ $V_{DD}$ = Max | 2.2 | $V_{DD}$ + 0.5 | 2.2 | $V_{DD}$ + 0.5 | 2.2 | $V_{DD}$ + 0.5 | V |
| $V_{IL}$[1, 2] | Low Level Input Voltage @ $V_{DD}$ = Min | –0.5 | +0.8 | –0.5 | +0.8 | –0.5 | +0.8 | V |

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

## ELECTRICAL CHARACTERISTICS (3.3 V)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$[1, 2] | High Level Output Voltage | @ $V_{DD}$ = Min, $I_{OH}$ = –2.0 mA | 2.4 | | V |
| $V_{OL}$[1, 2] | Low Level Output Voltage | @ $V_{DD}$ = Min, $I_{OL}$ = 4.0 mA | | 0.4 | V |
| $I_{IH}$[3, 4] | High Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 10 | µA |
| $I_{IL}$[3] | Low Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 10 | µA |
| $I_{ILP}$[4] | Low Level Input Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 150 | µA |
| $I_{OZH}$[5, 6, 7, 8] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 10 | µA |
| $I_{OZL}$[5, 9] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 10 | µA |
| $I_{OZHP}$[9] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ Max | | 350 | µA |
| $I_{OZLC}$[7] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 1.5 | mA |
| $I_{OZLA}$[10] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 1.5 V | | 350 | µA |
| $I_{OZLAR}$[8] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 4.2 | mA |
| $I_{OZLS}$[6] | Three-State Leakage Current | @ $V_{DD}$ = Max, $V_{IN}$ = 0 V | | 150 | µA |
| $C_{IN}$[11, 12] | Input Capacitance | $f_{IN}$ = 1 MHz, $T_{CASE}$ = 25°C, $V_{IN}$ = 2.5 V | | 4.7 | pF |

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

## EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing ($V_{DD}$)

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

*Example:* Estimate $P_{EXT}$ with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz ($t_{CK}$ = 25 ns)

The $P_{EXT}$ equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$$

Note that the conditions causing a worst-case $P_{EXT}$ are different from those causing a worst-case $P_{INT}$. Maximum $P_{INT}$ cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

**Table 6. External Power Calculations (3.3 V Devices)**

| Pin Type | No. of Pins | % Switching | × C | × f | × $V_{DD}^2$ | = $P_{EXT}$ |
|---|---|---|---|---|---|---|
| Address | 15 | 50 | × 44.7 pF | × 10 MHz | × 10.9 V | = 0.037 W |
| $\overline{MS0}$ | 1 | 0 | × 44.7 pF | × 10 MHz | × 10.9 V | = 0.000 W |
| $\overline{WR}$ | 1 | – | × 44.7 pF | × 20 MHz | × 10.9 V | = 0.010 W |
| Data | 32 | 50 | × 14.7 pF | × 10 MHz | × 10.9 V | = 0.026 W |
| ADDRCLK | 1 | – | × 4.7 pF | × 20 MHz | × 10.9 V | = 0.001 W |
| | | | | | | **$P_{EXT}$ = 0.074 W** |

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed Table 7 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute Maximum Ratings**

| Parameter | ADSP-21060/ADSP-21060C ADSP-21062 5 V | ADSP-21060L/ADSP-21060LC ADSP-21062L 3.3 V |
|---|---|---|
| Supply Voltage ($V_{DD}$) | –0.3 V to +7.0 V | –0.3 V to +4.6 V |
| Input Voltage | –0.5 V to $V_{DD}$ + 0.5 V | –0.5 V to $V_{DD}$ +0.5 V |
| Output Voltage Swing | –0.5 V to $V_{DD}$ + 0.5 V | –0.5 V to $V_{DD}$ + 0.5 V |
| Load Capacitance | 200 pF | 200 pF |
| Storage Temperature Range | –65°C to +150°C | –65°C to +150°C |
| Lead Temperature (5 seconds) | 280°C | 280°C |
| Junction Temperature Under Bias | 130°C | 130°C |

### *Memory Write—Bus Master*

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

**Table 15. Memory Write—Bus Master**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAAK}$ | ACK Delay from Address, Selects[1, 2] | | 14 + 7DT/8 + W | ns |
| $t_{DSAK}$ | ACK Delay from $\overline{WR}$ Low[1] | | 8 + DT/2 + W | ns |
| *Switching Characteristics* | | | | |
| $t_{DAWH}$ | Address Selects to $\overline{WR}$ Deasserted[2] | 17 + 15DT/16 + W | | ns |
| $t_{DAWL}$ | Address Selects to $\overline{WR}$ Low[2] | 3 + 3DT/8 | | ns |
| $t_{WW}$ | $\overline{WR}$ Pulse Width | 12 + 9DT/16 + W | | ns |
| $t_{DDWH}$ | Data Setup Before $\overline{WR}$ High | 7 + DT/2 + W | | ns |
| $t_{DWHA}$ | Address Hold After $\overline{WR}$ Deasserted | 0.5 + DT/16 + H | | ns |
| $t_{DATRWH}$ | Data Disable After $\overline{WR}$ Deasserted[3] | 1 + DT/16 + H | 6 + DT/16 + H | ns |
| $t_{WWR}$ | $\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low | 8 + 7DT/16 + H | | ns |
| $t_{DDWR}$ | Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low | 5 + 3DT/8 + I | | ns |
| $t_{WDE}$ | $\overline{WR}$ Low to Data Enabled | –1 + DT/16 | | ns |
| $t_{SADADC}$ | Address, Selects Setup Before ADRCLK High[2] | 0 + DT/4 | | ns |

W = (number of wait states specified in WAIT register) × $t_{CK}$.
H = $t_{CK}$ (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = $t_{CK}$ (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = $t_{CK}$ (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by $t_{DAAK}$ or $t_{DSAK}$ or synchronous specification $t_{SACKC}$ for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications $t_{SACKC}$ and $t_{HACK}$ must be met for wait state modes external, either, or both (both, after internal wait states have completed).

[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

### *Synchronous Read/Write—Bus Master*

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 30). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

**Table 16. Synchronous Read/Write—Bus Master**

| Parameter | | 5 V and 3.3 V Min | 5 V and 3.3 V Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSDATI}$ | Data Setup Before CLKIN | 3 + DT/8 | | ns |
| $t_{HSDATI}$ | Data Hold After CLKIN | 3.5 – DT/8 | | ns |
| $t_{DAAK}$ | ACK Delay After Address, Selects[1, 2] | | 14 + 7DT/8 + W | ns |
| $t_{SACKC}$ | ACK Setup Before CLKIN[2] | 6.5 + DT/4 | | ns |
| $t_{HACK}$ | ACK Hold After CLKIN | –1 – DT/4 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DADRO}$ | Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1] | | 7 – DT/8 | ns |
| $t_{HADRO}$ | Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN | –1 – DT/8 | | ns |
| $t_{DPGC}$ | PAGE Delay After CLKIN | 9 + DT/8 | 16 + DT/8 | ns |
| $t_{DRDO}$ | $\overline{RD}$ High Delay After CLKIN | –2 – DT/8 | 4 – DT/8 | ns |
| $t_{DWRO}$ | $\overline{WR}$ High Delay After CLKIN | –3 – 3DT/16 | 4 – 3DT/16 | ns |
| $t_{DRWL}$ | $\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN | 8 + DT/4 | 12.5 + DT/4 | ns |
| $t_{SDDATO}$ | Data Delay After CLKIN | | 19 + 5DT/16 | ns |
| $t_{DATTR}$ | Data Disable After CLKIN[3] | 0 – DT/8 | 7 – DT/8 | ns |
| $t_{DADCCK}$ | ADRCLK Delay After CLKIN | 4 + DT/8 | 10 + DT/8 | ns |
| $t_{ADRCK}$ | ADRCLK Period | $t_{CK}$ | | ns |
| $t_{ADRCKH}$ | ADRCLK Width High | ($t_{CK}$/2 – 2) | | ns |
| $t_{ADRCKL}$ | ADRCLK Width Low | ($t_{CK}$/2 – 2) | | ns |

[1] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[2] ACK delay/setup: user must meet $t_{DAAK}$ or $t_{DSAK}$ or synchronous specification $t_{SAKC}$ for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

### *Link Ports —1 × CLK Speed Operation*

**Table 23. Link Ports—Receive**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLDCL}$ | Data Setup Before LCLK Low[1] | 3.5 | | 3 | | ns |
| $t_{HLDCL}$ | Data Hold After LCLK Low | 3 | | 3 | | ns |
| $t_{LCLKIW}$ | LCLK Period (1× Operation) | $t_{CK}$ | | $t_{CK}$ | | ns |
| $t_{LCLKRWL}$ | LCLK Width Low | 6 | | 6 | | ns |
| $t_{LCLKRWH}$ | LCLK Width High | 5 | | 5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DLAHC}$ | LACK High Delay After CLKIN High[2, 3] | 18 + DT/2 | 28.5 + DT/2 | 18 + DT/2 | 28.5 + DT/2 | ns |
| $t_{DLALC}$ | LACK Low Delay After LCLK High | –3 | +13 | –3 | +13 | ns |
| $t_{ENDLK}$ | LACK Enable From CLKIN | 5 + DT/2 | | 5 + DT/2 | | ns |
| $t_{TDLK}$ | LACK Disable From CLKIN | | 20 + DT/2 | | 20 + DT/2 | ns |

[1] For ADSP-21062, specification is 3 ns min.
[2] LACK goes low with $t_{DLALC}$ relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[3] For ADSP-21060C, specification is 18 + DT/2 ns min, 29 + DT/2 ns max.

**Table 24. Link Ports—Transmit**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLACH}$ | LACK Setup Before LCLK High[1] | 18 | | 18 | | ns |
| $t_{HLACH}$ | LACK Hold After LCLK High | –7 | | –7 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DLCLK}$ | Data Delay After CLKIN (1× Operation)[2] | | 15.5 | | 15.5 | ns |
| $t_{DLDCH}$ | Data Delay After LCLK High[3] | | 3 | | 2.5 | ns |
| $t_{HLDCH}$ | Data Hold After LCLK High | –3 | | –3 | | ns |
| $t_{LCLKTWL}$ | LCLK Width Low[4] | ($t_{CK}$/2) – 2 | ($t_{CK}$/2) + 2 | ($t_{CK}$/2) – 1 | ($t_{CK}$/2) + 1.25 | ns |
| $t_{LCLKTWH}$ | LCLK Width High[5] | ($t_{CK}$/2) – 2 | ($t_{CK}$/2) + 2 | ($t_{CK}$/2) – 1.25 | ($t_{CK}$/2) + 1 | ns |
| $t_{DLACLK}$ | LCLK Low Delay After LACK High[6] | ($t_{CK}$/2) + 8.5 | (3 × $t_{CK}$/2) + 17 | ($t_{CK}$/2) + 8 | (3 × $t_{CK}$/2) + 17.5 | ns |
| $t_{ENDLK}$ | LACK Enable From CLKIN | 5 + DT/2 | | 5 + DT/2 | | ns |
| $t_{TDLK}$ | LACK Disable From CLKIN | | 20 + DT/2 | | 20 + DT/2 | ns |

[1] For ADSP-21060L/ADSP-21060LC, specification is 20 ns min.
[2] For ADSP-21060L, specification is 16.5 ns max; for ADSP-21060LC, specification is 16.75 ns max.
[3] For ADSP-21062, specification is 2.5 ns max.
[4] For ADSP-21062, specification is ($t_{CK}$/2) – 1 ns min, ($t_{CK}$/2) + 1.25 ns max; for ADSP-21062L, specification is ($t_{CK}$/2) – 1 ns min, ($t_{CK}$/2) + 1.5 ns max; for ADSP-21060LC specification is ($t_{CK}$/2) – 1 ns min, ($t_{CK}$/2) + 2.25 ns max.
[5] For ADSP-21062, specification is ($t_{CK}$/2) – 1.25 ns min, ($t_{CK}$/2) + 1 ns max; for ADSP-21062L, specification is ($t_{CK}$/2) – 1.5 ns min, ($t_{CK}$/2) + 1 ns max; for ADSP-21060C specification is ($t_{CK}$/2) – 2.25 ns min, ($t_{CK}$/2) + 1 ns max.
[6] For ADSP-21062, specification is ($t_{CK}$/2) + 8.75 ns min, (3 × $t_{CK}$/2) + 17 ns max; for ADSP-21062L, specification is ($t_{CK}$/2) + 8 ns min, (3 × $t_{CK}$/2) + 17 ns max; for ADSP-21060LC specification is ($t_{CK}$/2) + 8 ns min, (3 × $t_{CK}$/2) + 18.5 ns max.

**Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLCK}$ | LACK/LCLK Setup Before CLKIN Low[1] | 10 | | 10 | | ns |
| $t_{HLCK}$ | LACK/LCLK Hold After CLKIN Low[1] | 2 | | 2 | | ns |

[1] Only required for interrupt recognition in the current cycle.

### *Link Ports —2 × CLK Speed Operation*

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$Setup\ Skew = t_{LCLKTWH}\ \text{min} - t_{DLDCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$Hold\ Skew = t_{LCLKTWL}\ \text{min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

Note that link port transfers at 2× CLK speed at 40 MHz ($t_{CK}$ = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz ($t_{CK}$ = 30 ns) work as specified.

**Table 26. Link Ports—Receive**

| Parameter | | 5 V Min | 5 V Max | 3.3 V Min | 3.3 V Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SLDCL}$ | Data Setup Before LCLK Low | 2.5 | | 2.25 | | ns |
| $t_{HLDCL}$ | Data Hold After LCLK Low | 2.25 | | 2.25 | | ns |
| $t_{LCLKIW}$ | LCLK Period (2× Operation) | $t_{CK}/2$ | | $t_{CK}/2$ | | ns |
| $t_{LCLKRWL}$ | LCLK Width Low[1] | 4.5 | | 5.25 | | ns |
| $t_{LCLKRWH}$ | LCLK Width High[2] | 4.25 | | 4 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DLAHC}$ | LACK High Delay After CLKIN High[3] | 18 + DT/2 | 28.5 + DT/2 | 18 + DT/2 | 29.5 + DT/2 | ns |
| $t_{DLALC}$ | LACK Low Delay After LCLK High[4] | 6 | 16 | 6 | 16 | ns |

[1] For ADSP-21060L, specification is 5 ns min.
[2] For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.
[3] LACK goes low with $t_{DLALC}$ relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[4] For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

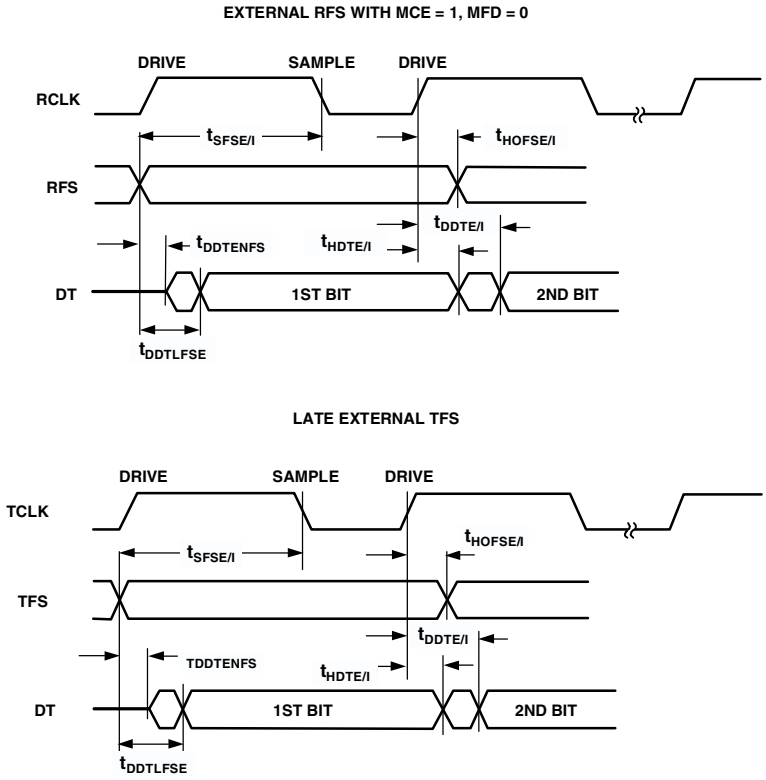



*Figure 26. Serial Ports—External Late Frame Sync*

## TEST CONDITIONS

For the ac signal specifications (timing parameters), see Timing Specifications on Page 21. These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 28.

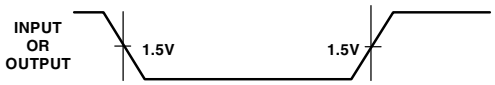



*Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)*

### Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, $C_L$, and the load current, $I_L$. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time $t_{DIS}$ is the difference between $t_{MEASURED}$ and $t_{DECAY}$ as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. $t_{DECAY}$ is calculated with test loads $C_L$ and $I_L$, and with ΔV equal to 0.5 V.

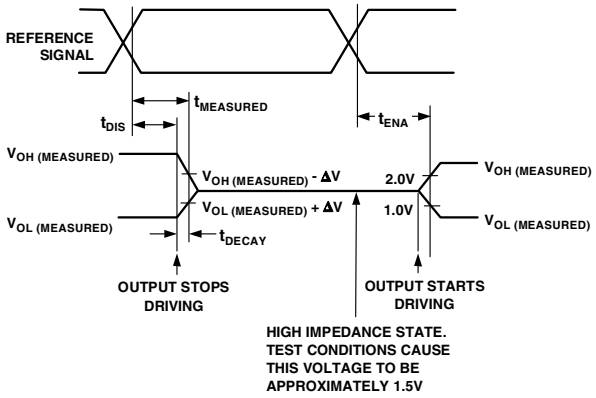



*Figure 29. Output Enable/Disable*

### Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time $t_{ENA}$ is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 29). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

### Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate $t_{DECAY}$ using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. $C_L$ is the total bus capacitance (per data line), and $I_L$ is the total leakage or three-state current (per data line). The hold time will be $t_{DECAY}$ plus the minimum disable time (i.e., $t_{DATRWH}$ for the write cycle).

### Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 30). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 32, Figure 33, Figure 37, and Figure 38 show how output rise time varies with capacitance. Figure 34 and Figure 36 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 32, Figure 33, Figure 37, and Figure 38 may not be linear outside the ranges shown.

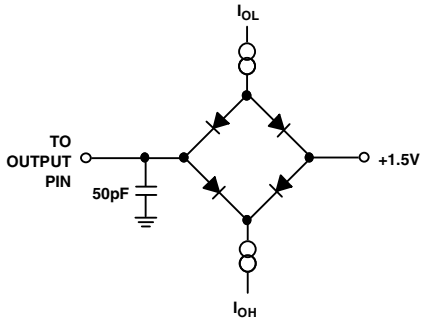



*Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)*

### Output Drive Characteristics

Figure 31 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

***Output Characteristics (5 V)***

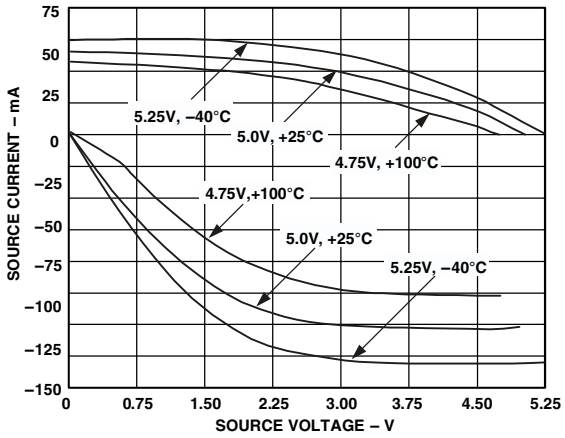



*Figure 31. ADSP-21062 Typical Output Drive Currents ($V_{DD}$ = 5 V)*

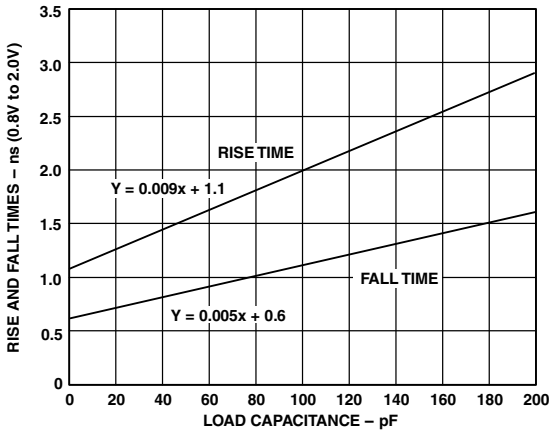



*Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance ($V_{DD}$ = 5 V)*

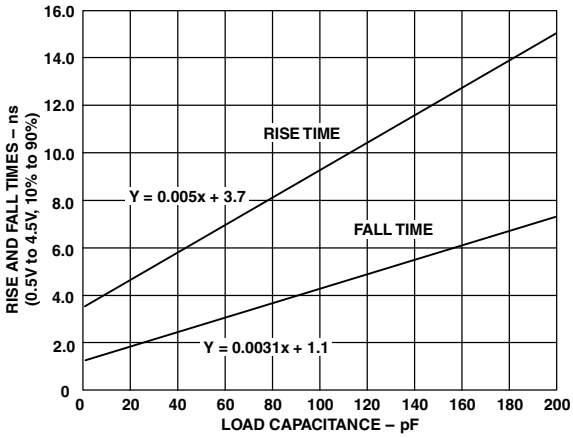



*Figure 32. Typical Output Rise Time (10% to 90% $V_{DD}$) vs. Load Capacitance ($V_{DD}$ = 5 V)*

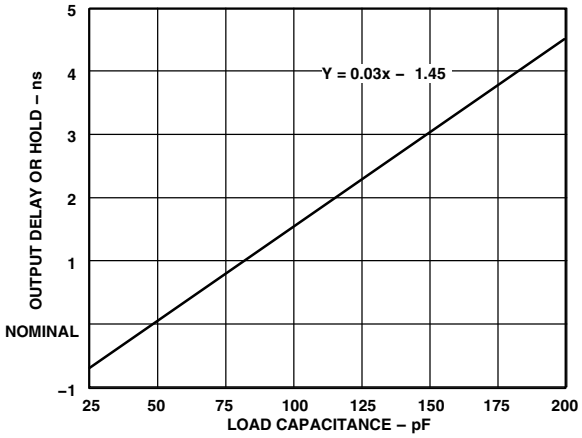



*Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) ($V_{DD}$ = 5 V)*

# 225-BALL PBGA BALL CONFIGURATION

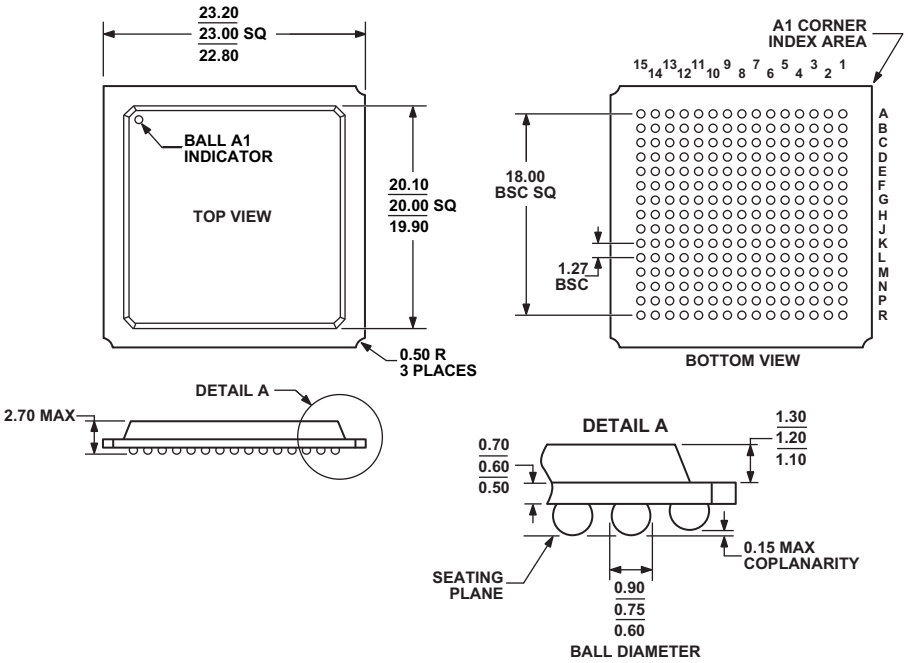
**Table 40. ADSP-2106x 225-Ball Metric PBGA Ball Assignments (B-225-2)**

| Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{BMS}$ | A01 | ADDR25 | D01 | ADDR14 | G01 | ADDR6 | K01 | $\overline{EMU}$ | N01 |
| ADDR30 | A02 | ADDR26 | D02 | ADDR15 | G02 | ADDR5 | K02 | TDO | N02 |
| $\overline{DMAR2}$ | A03 | $\overline{MS2}$ | D03 | ADDR16 | G03 | ADDR3 | K03 | $\overline{IRQ0}$ | N03 |
| DT1 | A04 | ADDR29 | D04 | ADDR19 | G04 | ADDR0 | K04 | $\overline{IRQ1}$ | N04 |
| RCLK1 | A05 | $\overline{DMAR1}$ | D05 | GND | G05 | ICSA | K05 | ID2 | N05 |
| TCLK0 | A06 | TFS1 | D06 | $V_{DD}$ | G06 | GND | K06 | L5DAT1 | N06 |
| RCLK0 | A07 | $\overline{CPA}$ | D07 | $V_{DD}$ | G07 | $V_{DD}$ | K07 | L4CLK | N07 |
| ADRCLK | A08 | $\overline{HBG}$ | D08 | $V_{DD}$ | G08 | $V_{DD}$ | K08 | L3CLK | N08 |
| $\overline{CS}$ | A09 | $\overline{DMAG2}$ | D09 | $V_{DD}$ | G09 | $V_{DD}$ | K09 | L3DAT3 | N09 |
| CLKIN | A10 | $\overline{BR5}$ | D10 | $V_{DD}$ | G10 | GND | K10 | L2DAT0 | N10 |
| PAGE | A11 | $\overline{BR1}$ | D11 | GND | G11 | GND | K11 | L1ACK | N11 |
| $\overline{BR3}$ | A12 | DATA40 | D12 | DATA22 | G12 | DATA8 | K12 | L1DAT3 | N12 |
| DATA47 | A13 | DATA37 | D13 | DATA25 | G13 | DATA11 | K13 | L0DAT3 | N13 |
| DATA44 | A14 | DATA35 | D14 | DATA24 | G14 | DATA13 | K14 | DATA1 | N14 |
| DATA42 | A15 | DATA34 | D15 | DATA23 | G15 | DATA14 | K15 | DATA3 | N15 |
| $\overline{MS0}$ | B01 | ADDR21 | E01 | ADDR12 | H01 | ADDR2 | L01 | $\overline{TRST}$ | P01 |
| $\overline{SW}$ | B02 | ADDR22 | E02 | ADDR11 | H02 | ADDR1 | L02 | TMS | P02 |
| ADDR31 | B03 | ADDR24 | E03 | ADDR13 | H03 | FLAG0 | L03 | EBOOT | P03 |
| $\overline{HBR}$ | B04 | ADDR27 | E04 | ADDR10 | H04 | FLAG3 | L04 | ID0 | P04 |
| DR1 | B05 | GND | E05 | GND | H05 | RPBA | L05 | L5CLK | P05 |
| DT0 | B06 | GND | E06 | $V_{DD}$ | H06 | GND | L06 | L5DAT3 | P06 |
| DR0 | B07 | GND | E07 | $V_{DD}$ | H07 | GND | L07 | L4DAT0 | P07 |
| REDY | B08 | GND | E08 | $V_{DD}$ | H08 | GND | L08 | L4DAT3 | P08 |
| $\overline{RD}$ | B09 | GND | E09 | $V_{DD}$ | H09 | GND | L09 | L3DAT2 | P09 |
| ACK | B10 | GND | E10 | $V_{DD}$ | H10 | GND | L10 | L2CLK | P10 |
| $\overline{BR6}$ | B11 | NC | E11 | GND | H11 | NC | L11 | L2DAT2 | P11 |
| $\overline{BR2}$ | B12 | DATA33 | E12 | DATA18 | H12 | DATA4 | L12 | L1DAT0 | P12 |
| DATA45 | B13 | DATA30 | E13 | DATA19 | H13 | DATA7 | L13 | L0ACK | P13 |
| DATA43 | B14 | DATA32 | E14 | DATA21 | H14 | DATA9 | L14 | L0DAT1 | P14 |
| DATA39 | B15 | DATA31 | E15 | DATA20 | H15 | DATA10 | L15 | DATA0 | P15 |
| $\overline{MS3}$ | C01 | ADDR17 | F01 | ADDR9 | J01 | FLAG1 | M01 | TCK | R01 |
| $\overline{MS1}$ | C02 | ADDR18 | F02 | ADDR8 | J02 | FLAG2 | M02 | $\overline{IRQ2}$ | R02 |
| ADDR28 | C03 | ADDR20 | F03 | ADDR7 | J03 | TIMEXP | M03 | $\overline{RESET}$ | R03 |
| $\overline{SBTS}$ | C04 | ADDR23 | F04 | ADDR4 | J04 | TDI | M04 | ID1 | R04 |
| TCLK1 | C05 | GND | F05 | GND | J05 | LBOOT | M05 | L5DAT0 | R05 |
| RFS1 | C06 | GND | F06 | $V_{DD}$ | J06 | L5ACK | M06 | L4ACK | R06 |
| TFS0 | C07 | $V_{DD}$ | F07 | $V_{DD}$ | J07 | L5DAT2 | M07 | L4DAT1 | R07 |
| RFS0 | C08 | $V_{DD}$ | F08 | $V_{DD}$ | J08 | L4DAT2 | M08 | L3ACK | R08 |
| $\overline{WR}$ | C09 | $V_{DD}$ | F09 | $V_{DD}$ | J09 | L3DAT0 | M09 | L3DAT1 | R09 |
| $\overline{DMAG1}$ | C10 | GND | F10 | $V_{DD}$ | J10 | L2DAT3 | M10 | L2ACK | R10 |
| $\overline{BR4}$ | C11 | GND | F11 | GND | J11 | L1DAT1 | M11 | L2DAT1 | R11 |
| DATA46 | C12 | DATA29 | F12 | DATA12 | J12 | L0DAT0 | M12 | L1CLK | R12 |
| DATA41 | C13 | DATA26 | F13 | DATA15 | J13 | DATA2 | M13 | L1DAT2 | R13 |
| DATA38 | C14 | DATA28 | F14 | DATA16 | J14 | DATA5 | M14 | L0CLK | R14 |
| DATA36 | C15 | DATA27 | F15 | DATA17 | J15 | DATA6 | M15 | L0DAT2 | R15 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DATA42 | DATA44 | DATA47 | $\overline{BR3}$ | PAGE | CLKIN | $\overline{CS}$ | ADRCLK | RCLK0 | TCLK0 | RCLK1 | DT1 | $\overline{DMAR2}$ | ADDR30 | $\overline{BMS}$ | A |
| DATA39 | DATA43 | DATA45 | $\overline{BR2}$ | $\overline{BR6}$ | ACK | $\overline{RD}$ | REDY | DR0 | DT0 | DR1 | $\overline{HBR}$ | ADDR31 | $\overline{SW}$ | $\overline{MS0}$ | B |
| DATA36 | DATA38 | DATA41 | DATA46 | $\overline{BR4}$ | $\overline{DMAG1}$ | $\overline{WR}$ | RFS0 | TFS0 | RFS1 | TCLK1 | $\overline{SBTS}$ | ADDR28 | $\overline{MS1}$ | $\overline{MS3}$ | C |
| DATA34 | DATA35 | DATA37 | DATA40 | $\overline{BR1}$ | $\overline{BR5}$ | $\overline{DMAG2}$ | $\overline{HBG}$ | $\overline{CPA}$ | TFS1 | $\overline{DMAR1}$ | ADDR29 | $\overline{MS2}$ | ADDR26 | ADDR25 | D |
| DATA31 | DATA32 | DATA30 | DATA33 | NC | GND | GND | GND | GND | GND | GND | ADDR27 | ADDR24 | ADDR22 | ADDR21 | E |
| DATA27 | DATA28 | DATA26 | DATA29 | GND | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | GND | ADDR23 | ADDR20 | ADDR18 | ADDR17 | F |
| DATA23 | DATA24 | DATA25 | DATA22 | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | ADDR19 | ADDR16 | ADDR15 | ADDR14 | G |
| DATA20 | DATA21 | DATA19 | DATA18 | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | ADDR10 | ADDR13 | ADDR11 | ADDR12 | H |
| DATA17 | DATA16 | DATA15 | DATA12 | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | ADDR4 | ADDR7 | ADDR8 | ADDR9 | J |
| DATA14 | DATA13 | DATA11 | DATA8 | GND | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | ICSA | ADDR0 | ADDR3 | ADDR5 | ADDR6 | K |
| DATA10 | DATA9 | DATA7 | DATA4 | NC | GND | GND | GND | GND | GND | RPBA | FLAG3 | FLAG0 | ADDR1 | ADDR2 | L |
| DATA6 | DATA5 | DATA2 | L0DAT0 | L1DAT1 | L2DAT3 | L3DAT0 | L4DAT2 | L5DAT2 | L5ACK | LBOOT | TDI | TIMEXP | FLAG2 | FLAG1 | M |
| DATA3 | DATA1 | L0DAT3 | L1DAT3 | L1ACK | L2DAT0 | L3DAT3 | L3CLK | L4CLK | L5DAT1 | ID2 | $\overline{IRQ1}$ | $\overline{IRQ0}$ | TDO | $\overline{EMU}$ | N |
| DATA0 | L0DAT1 | L0ACK | L1DAT0 | L2DAT2 | L2CLK | L3DAT2 | L4DAT3 | L4DAT0 | L5DAT3 | L5CLK | ID0 | EBOOT | TMS | $\overline{TRST}$ | P |
| L0DAT2 | L0CLK | L1DAT2 | L1CLK | L2DAT1 | L2ACK | L3DAT1 | L3ACK | L4DAT1 | L4ACK | L5DAT0 | ID1 | $\overline{RESET}$ | $\overline{IRQ2}$ | TCK | R |

*Figure 39. ADSP-21060/ADSP-21062 PBGA Ball Assignments (Top View, Summary)*

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MS-034-AAJ-2**

*Figure 40. 225-Ball Plastic Ball Grid Array [PBGA]*
*(B-225-2)*
*Dimensions shown in millimeters*

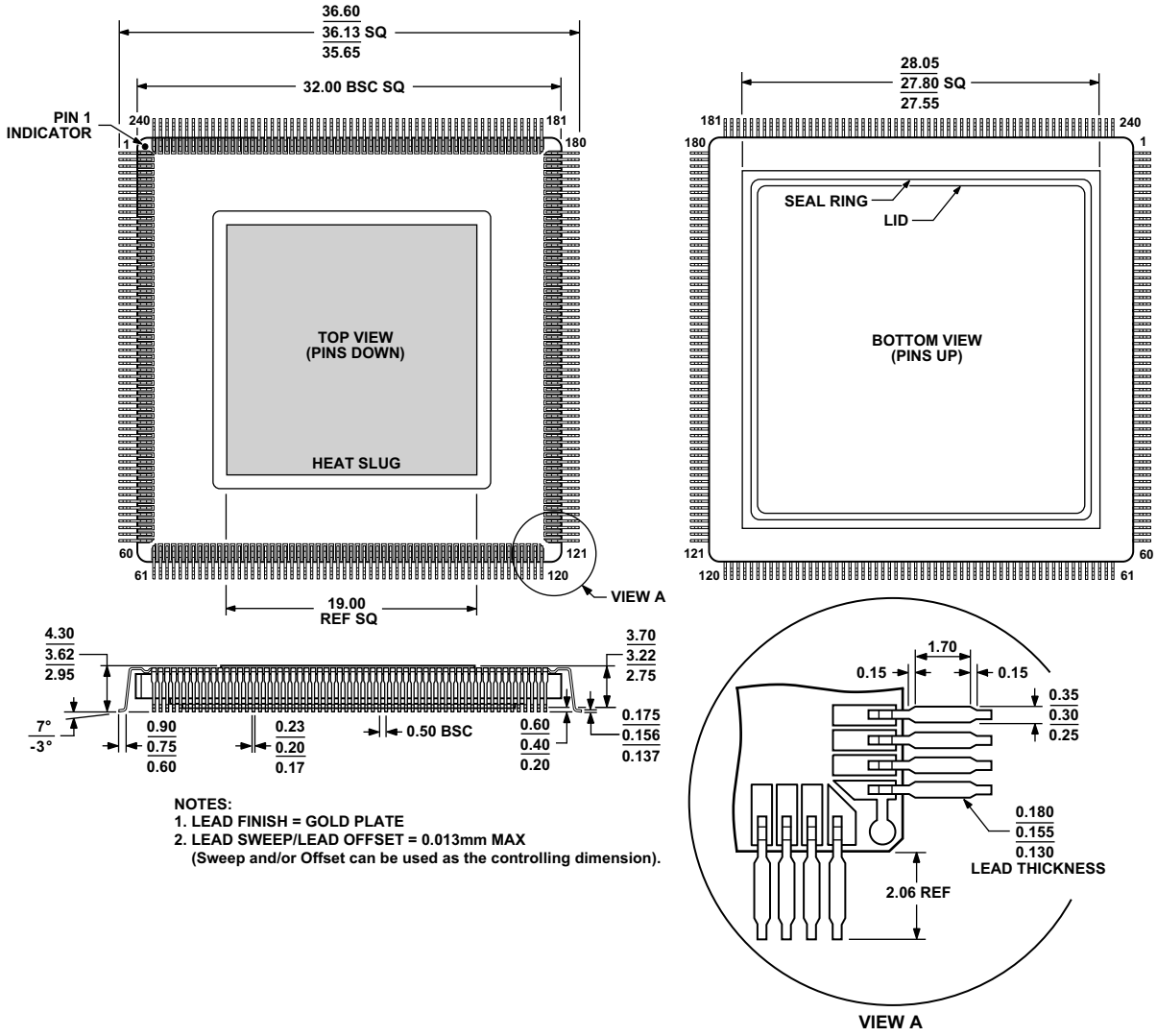



*Figure 42. 240-Lead Ceramic Quad Flat Package, Heat Slug Up [CQFP]*
*(QS-240-2A)*
*Dimensions shown in millimeters*

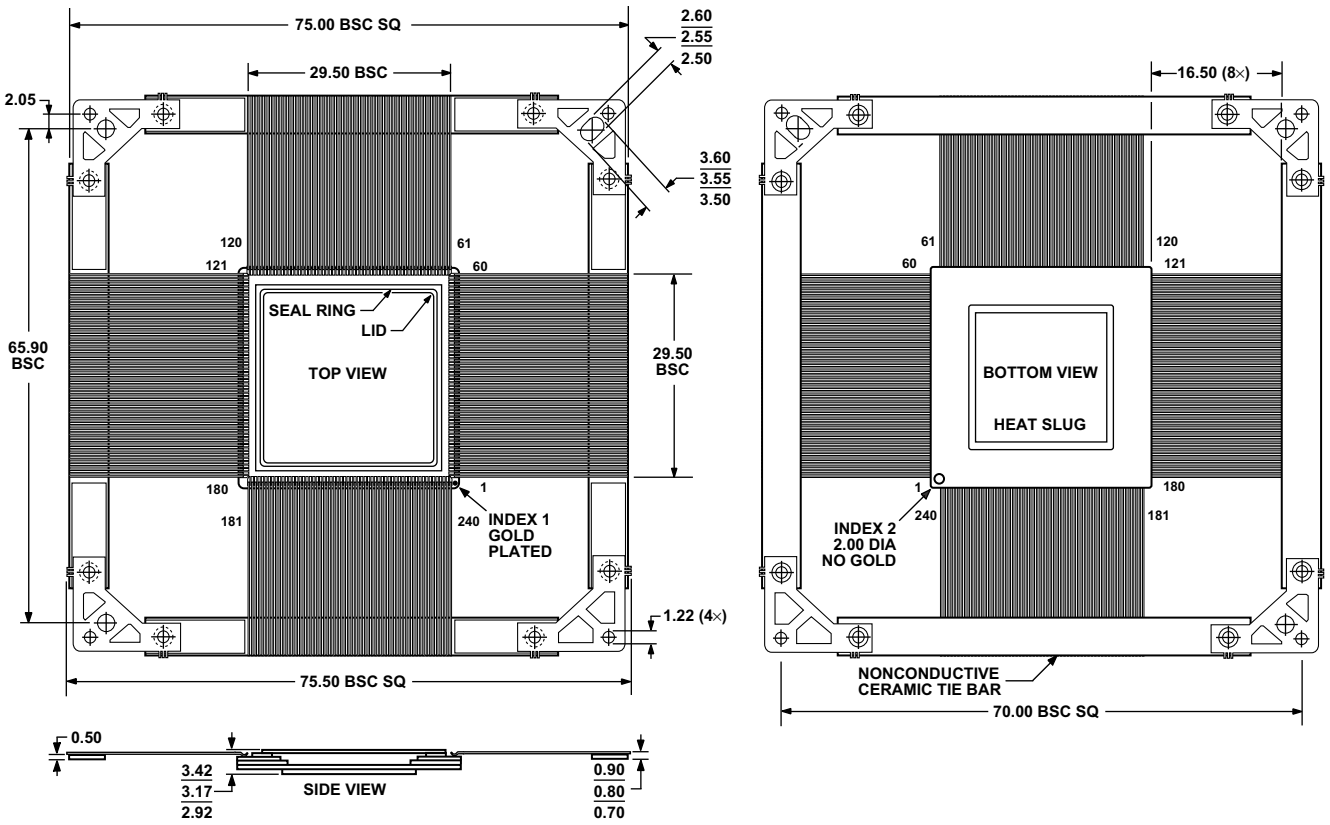



*Figure 45. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Up [CQFP]*
*(QS-240-1B)*
*Dimensions shown in millimeters*

## SURFACE-MOUNT DESIGN

Table 43 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

**Table 43. BGA Data for Use with Surface-Mount Design**

| Package | Ball Attach Type | Solder Mask Opening | Ball Pad Size |
|---|---|---|---|
| 225-Ball Grid Array (PBGA) | Solder Mask Defined | 0.63 mm diameter | 0.76 mm diameter |

## ORDERING GUIDE

| Model | Notes | Temperature Range | Instruction Rate | On-Chip SRAM | Operating Voltage | Package Description | Package Option |
|---|---|---|---|---|---|---|---|
| ASDP-21060CZ-133 | 1, 2 | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CZ-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CW-133 | 1, 2 | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ASDP-21060CW-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21060KS-133 | | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-133 | 2 | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060KBZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LKSZ-133 | 2 | 0°C to 85°C | 33 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKSZ-160 | 2 | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LAB-160 | | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LABZ-160 | 2 | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCB-133 | | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCBZ-133 | 2 | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ASDP-21060LCW-160 | 1, 2 | –40°C to +100°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21062KS-133 | | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-133 | 2 | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062KBZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062CS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062CSZ-160 | 2 | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-133 | 2 | 0°C to 85°C | 33 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LKBZ-160 | 2 | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LAB-160 | | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LABZ-160 | 2 | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LCS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LCSZ-160 | 2 | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |

[1] Model refers to package with formed leads. For model numbers of unformed lead versions (QS-240-1B, QS-240-2B), contact Analog Devices or an Analog Devices sales representative.
[2] RoHS compliant part.