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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	256kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21062csz-160

GENERAL DESCRIPTION

The ADSP-2106x SHARC®—Super Harvard Architecture Computer—is a 32-bit signal processing microcomputer that offers high levels of DSP performance. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 2 shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including up to 4M bit SRAM memory (see Table 1), a host processor interface, DMA controller, serial ports and link port, and parallel bus connectivity for glueless DSP multiprocessing.

Table 2. Benchmarks (at 40 MHz)

Benchmark Algorithm	Speed	Cycles
1024 Point Complex FFT (Radix 4, with reversal)	0.46 µs	18,221
FIR Filter (per tap)	25 ns	1
IIR Filter (per biquad)	100 ns	4
Divide (y/x)	150 ns	6
Inverse Square Root	225 ns	9
DMA Transfer Rate	240 Mbytes/s	

The ADSP-2106x continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1 illustrates the following architectural features:

- Computation units (ALU, multiplier and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Interval timer
- On-chip SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and multiprocessor Interface
- DMA controller
- Serial ports and link ports
- JTAG Test Access Port

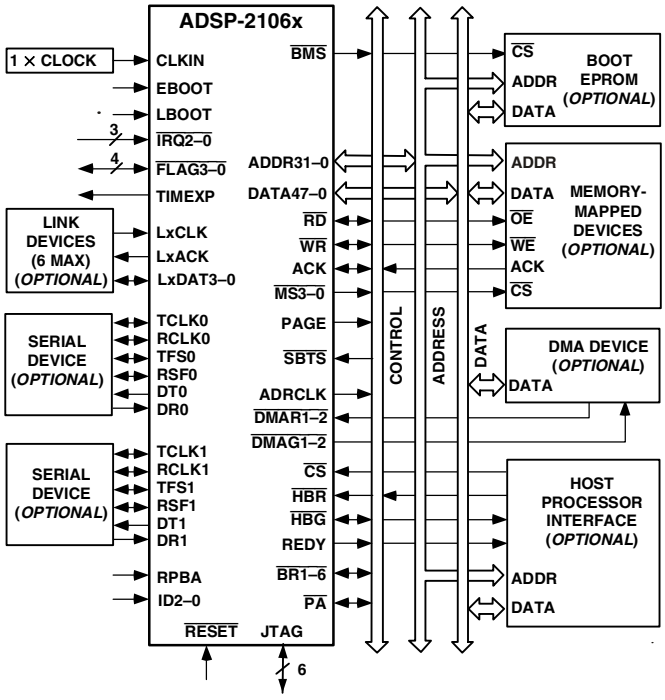

Figure 2. ADSP-2106x System Sample Configuration

SHARC FAMILY CORE ARCHITECTURE

The ADSP-2106x includes the following architectural features of the ADSP-21000 family core.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general–purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

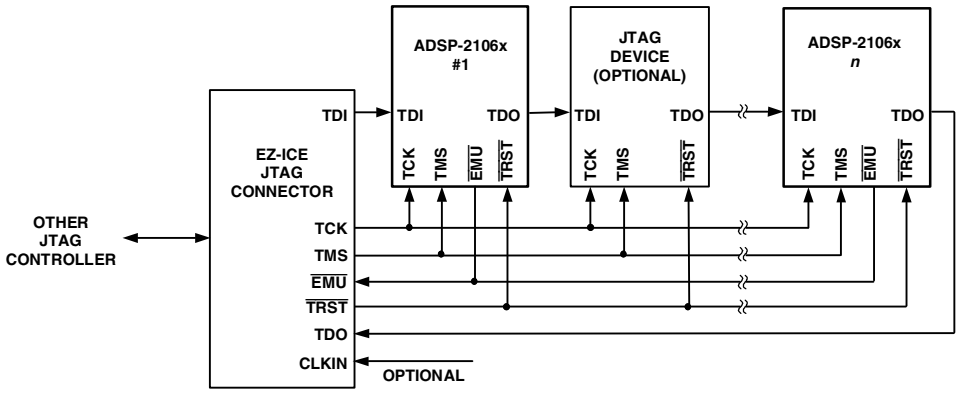

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

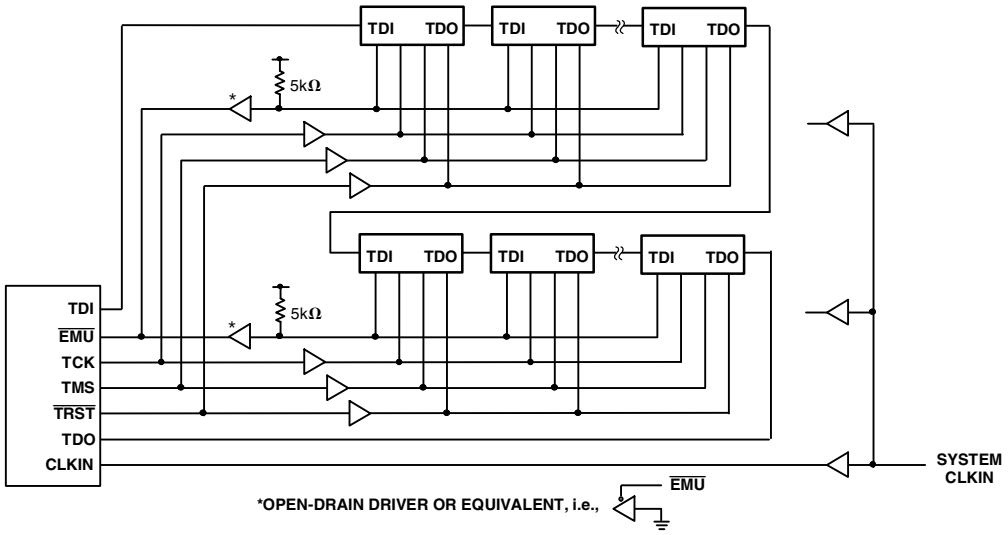

Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where% is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	745	mA
	t_{CK} = 25 ns, V_{DD} = Max	850	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	575	mA
	t_{CK} = 25 ns, V_{DD} = Max	670	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	340	mA
	t_{CK} = 25 ns, V_{DD} = Max	390	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	200	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106x state during execution of IDLE instruction.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	540	mA
	t_{CK} = 25 ns, V_{DD} = Max	600	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	425	mA
	t_{CK} = 25 ns, V_{DD} = Max	475	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	250	mA
	t_{CK} = 25 ns, V_{DD} = Max	275	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	180	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106xL state during execution of IDLE instruction.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

Figure 8 and Table 8 provide information on detail contained within the package marking for the ADSP-2106x processors (actual marking format may vary). For a complete listing of product availability, see Ordering Guide on Page 62.

Figure 8. Typical Package Brand

Table 8. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead (Pb) Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

The ADSP-2106x processors are available at maximum processor speeds of 33 MHz (–133), and 40 MHz (–160). The timing specifications are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating factor enables the calculation for timing specifications within the min to max range of the t_{CK} specification (see Table 9). DT is the difference between the derated CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25 \text{ ns}$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

For voltage reference levels, see Figure 28 on Page 48 under Test Conditions.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices. (O/D) = Open Drain, (A/D) = Active Drive.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 14. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		14 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 48 for the calculation of hold times given capacitive and dc loads.
[4] ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

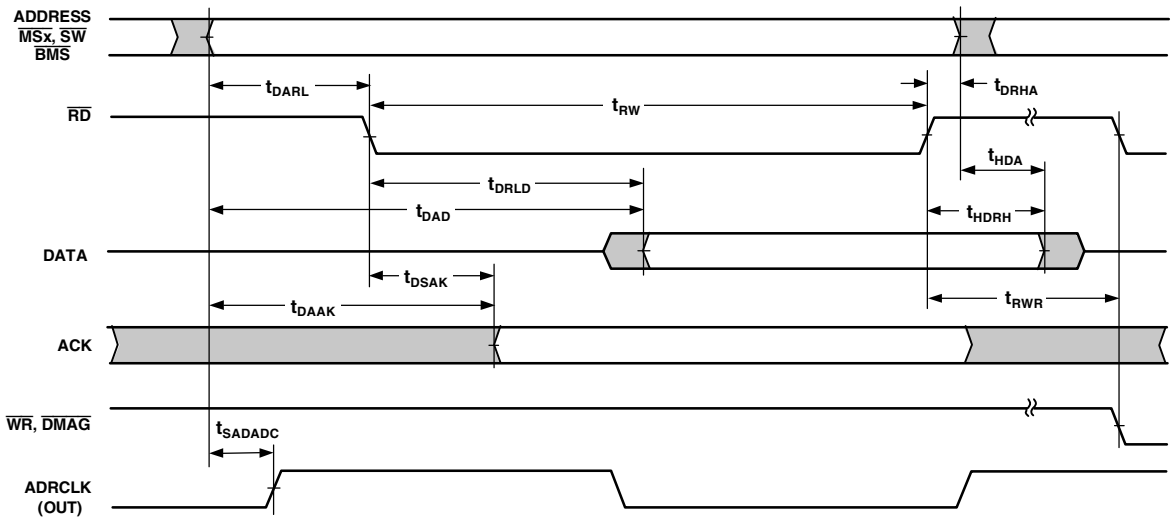

Figure 14. Memory Read—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet the bus slave timing requirements.

Table 17. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	15 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}$/$\overline{WR}$ Low Setup Before CLKIN[1]	9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}$/$\overline{WR}$ Low Hold After CLKIN[2]	–4 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}$/$\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN[3]		18 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[5]		9	ns
t_{ACKTR}	ACK Disable After CLKIN[5]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.
[2] For ADSP-21060C specification is –3.5 – 5DT/16 ns min, 8 + 7DT/16 ns max; for ADSP-21060LC specification is –3.75 – 5DT/16 ns min, 8 + 7DT/16 ns max.
[3] For ADSP-21062/ADSP-21062L/ADSP-21060C specification is 19 + 5DT/16 ns max; for ADSP-21060LC specification is 19.25 + 5DT/16 ns max.
[4] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.
[5] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

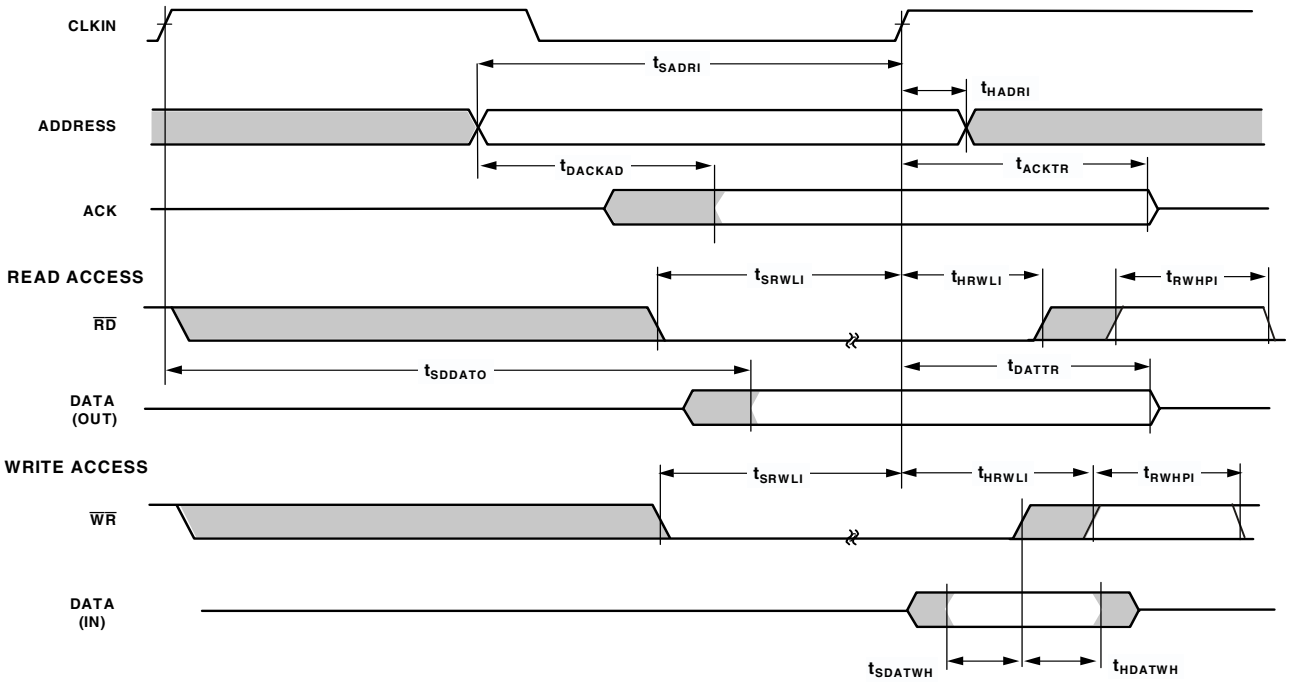

Figure 17. Synchronous Read/Write—Bus Slave

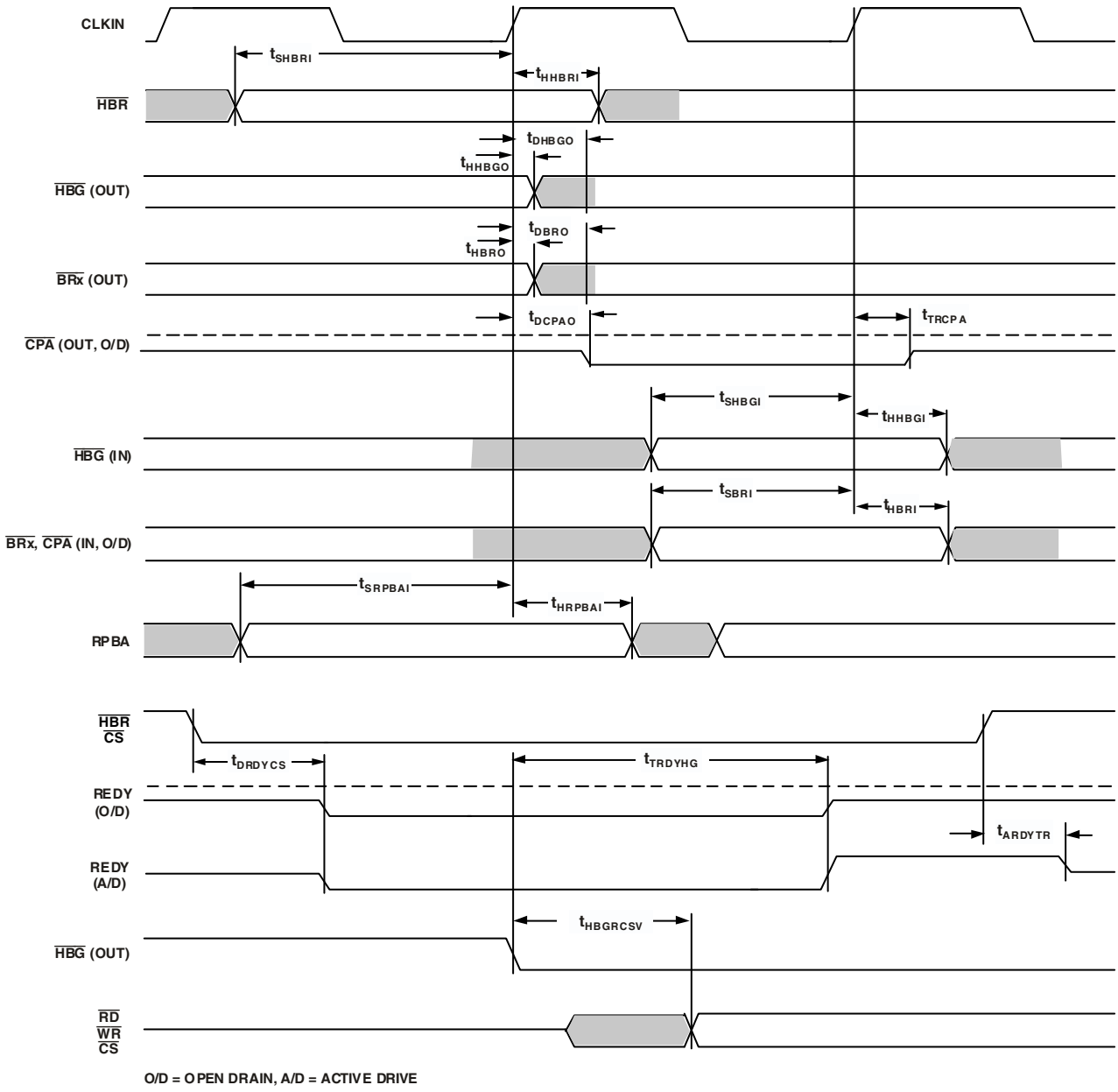

Figure 18. Multiprocessor Bus Request and Host Bus Request

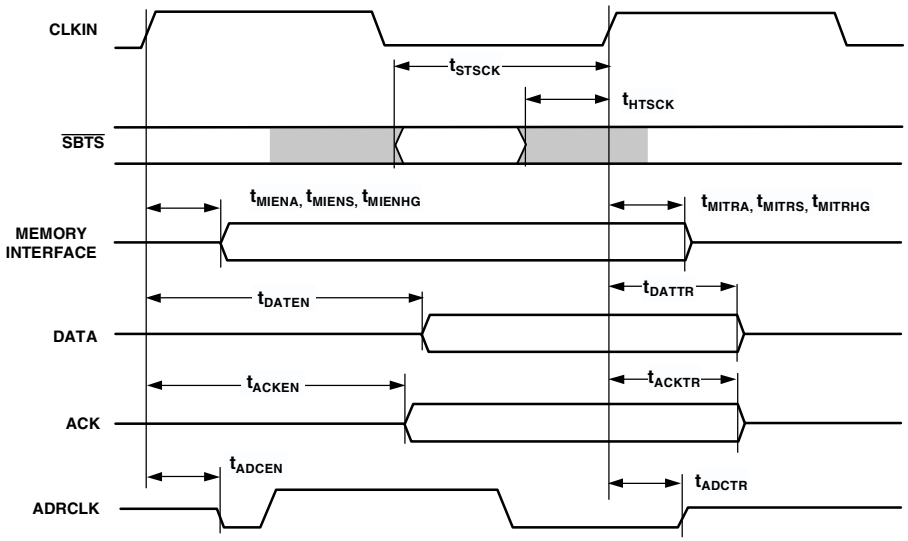

Figure 22. Three-State Timing (Bus Transition Cycle, $\overline{SBTS}$ Assertion)

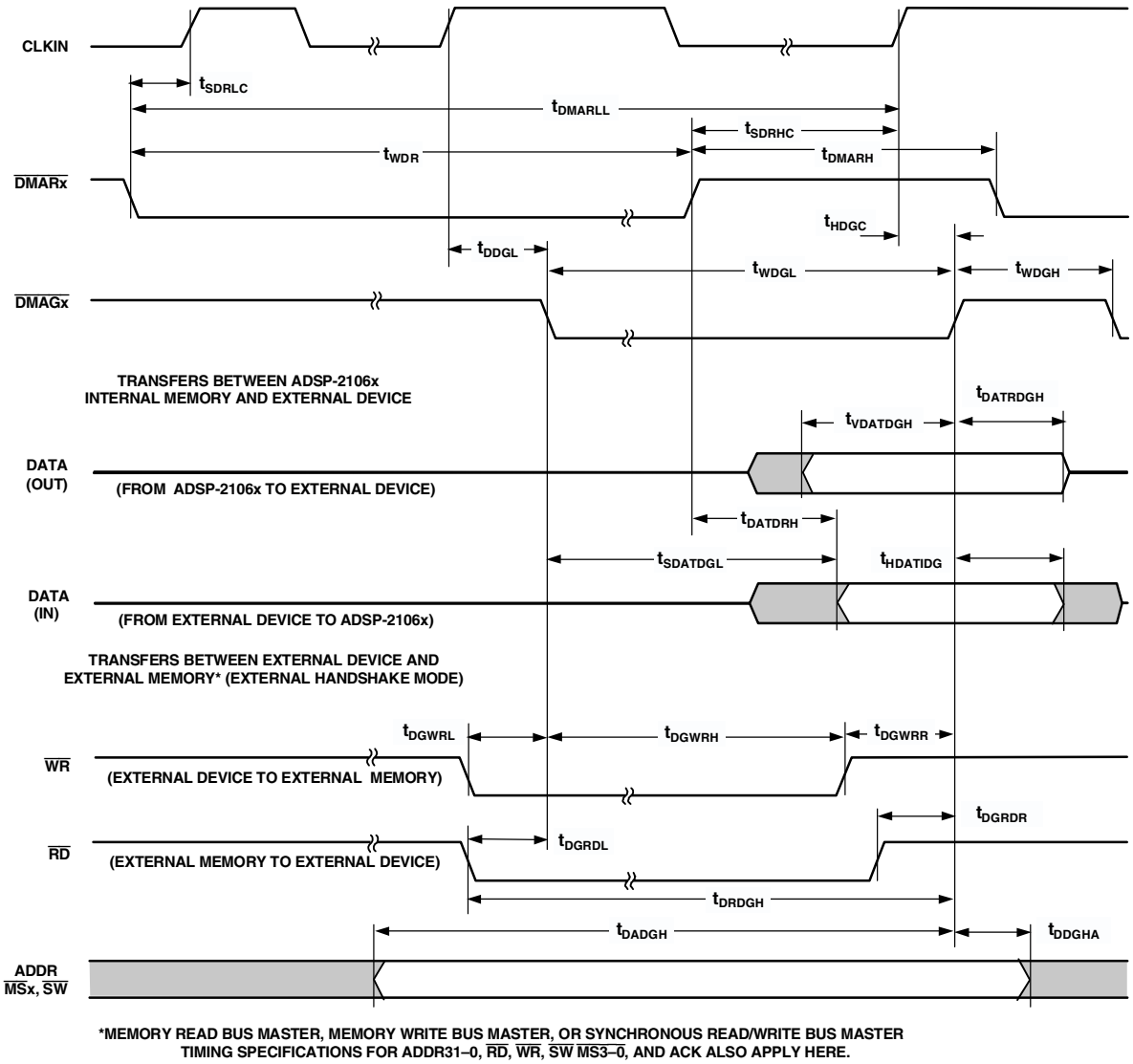

Figure 23. DMA Handshake

Link Ports —1 × CLK Speed Operation

Table 23. Link Ports—Receive

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLDCL}	Data Setup Before LCLK Low[1]	3.5		3		ns
t_{HLDCL}	Data Hold After LCLK Low	3		3		ns
t_{LCLKIW}	LCLK Period (1× Operation)	t_{CK}		t_{CK}		ns
$t_{LCLKRWL}$	LCLK Width Low	6		6		ns
$t_{LCLKRWH}$	LCLK Width High	5		5		ns
Switching Characteristics						
t_{DLAHC}	LACK High Delay After CLKIN High[2, 3]	18 + DT/2	28.5 + DT/2	18 + DT/2	28.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High	–3	+13	–3	+13	ns
t_{ENDLK}	LACK Enable From CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable From CLKIN		20 + DT/2		20 + DT/2	ns

[1] For ADSP-21062, specification is 3 ns min.
[2] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[3] For ADSP-21060C, specification is 18 + DT/2 ns min, 29 + DT/2 ns max.

Table 24. Link Ports—Transmit

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLACH}	LACK Setup Before LCLK High[1]	18		18		ns
t_{HLACH}	LACK Hold After LCLK High	–7		–7		ns
Switching Characteristics						
t_{DLCLK}	Data Delay After CLKIN (1× Operation)[2]		15.5		15.5	ns
t_{DLDCH}	Data Delay After LCLK High[3]		3		2.5	ns
t_{HLDCH}	Data Hold After LCLK High	–3		–3		ns
$t_{LCLKTWL}$	LCLK Width Low[4]	(t_{CK}/2) – 2	(t_{CK}/2) + 2	(t_{CK}/2) – 1	(t_{CK}/2) + 1.25	ns
$t_{LCLKTWH}$	LCLK Width High[5]	(t_{CK}/2) – 2	(t_{CK}/2) + 2	(t_{CK}/2) – 1.25	(t_{CK}/2) + 1	ns
t_{DLACLK}	LCLK Low Delay After LACK High[6]	(t_{CK}/2) + 8.5	(3 × t_{CK}/2) + 17	(t_{CK}/2) + 8	(3 × t_{CK}/2) + 17.5	ns
t_{ENDLK}	LACK Enable From CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable From CLKIN		20 + DT/2		20 + DT/2	ns

[1] For ADSP-21060L/ADSP-21060LC, specification is 20 ns min.
[2] For ADSP-21060L, specification is 16.5 ns max; for ADSP-21060LC, specification is 16.75 ns max.
[3] For ADSP-21062, specification is 2.5 ns max.
[4] For ADSP-21062, specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 1.25 ns max; for ADSP-21062L, specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 1.5 ns max; for ADSP-21060LC specification is (t_{CK}/2) – 1 ns min, (t_{CK}/2) + 2.25 ns max.
[5] For ADSP-21062, specification is (t_{CK}/2) – 1.25 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21062L, specification is (t_{CK}/2) – 1.5 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21060C specification is (t_{CK}/2) – 2.25 ns min, (t_{CK}/2) + 1 ns max.
[6] For ADSP-21062, specification is (t_{CK}/2) + 8.75 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21062L, specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21060LC specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 18.5 ns max.

Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLCK}	LACK/LCLK Setup Before CLKIN Low[1]	10		10		ns
t_{HLCK}	LACK/LCLK Hold After CLKIN Low[1]	2		2		ns

[1] Only required for interrupt recognition in the current cycle.

Link Ports —2 × CLK Speed Operation

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$Setup\ Skew = t_{LCLKTWH}\ \text{min} - t_{DLDCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$Hold\ Skew = t_{LCLKTWL}\ \text{min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

Note that link port transfers at 2× CLK speed at 40 MHz (t_{CK} = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz (t_{CK} = 30 ns) work as specified.

Table 26. Link Ports—Receive

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements						
t_{SLDCL}	Data Setup Before LCLK Low	2.5		2.25		ns
t_{HLDCL}	Data Hold After LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2× Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low[1]	4.5		5.25		ns
$t_{LCLKRWH}$	LCLK Width High[2]	4.25		4		ns
Switching Characteristics						
t_{DLAHC}	LACK High Delay After CLKIN High[3]	18 + DT/2	28.5 + DT/2	18 + DT/2	29.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High[4]	6	16	6	16	ns

[1] For ADSP-21060L, specification is 5 ns min.
[2] For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.
[3] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.
[4] For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

Serial Ports

For serial ports, see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 35, Figure 26, and Figure 25. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 28. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	6.5		ns
t_{SCLKW}	TCLK/RCLK Width[3]	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.
[3] For ADSP-21060/ADSP-21060C/ADSP-21060LC, specification is 9.5 ns min.

Table 29. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 30. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 31. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HDTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

Table 32. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width[2]	$0.5t_{SCLK}$ –2.5	$0.5t_{SCLK}$+2.5	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 0.5_{TSCLK} – 2 ns min, $0.5t_{SCLK}$ + 2 ns max.

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External TCLK[1, 3]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1, 4]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3 DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For ADSP-21060L/ADSP-21060C, specification is 3.5 ns min; for ADSP-21062 specification is 4.5 ns min.
[3] For ADSP-21062L, specification is 16 ns max.
[4] For ADSP-21062L, specification is 7.5 ns max.

Table 34. Serial Ports—GATED SCLK with External TFS (Mesh Multiprocessing)[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{STFSCK}	TFS Setup Before CLKIN	4		ns
t_{HTFSCK}	TFS Hold After CLKIN		$t_{CK}/2$	ns

[1] Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.

Table 35. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1, 2]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1, 3]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.
[2] For ADSP-21062/ADSP-21062L, specification is 12.75 ns max; for ADSP-21060L/ADSP-21060LC, specification is 12.8 ns max.
[3] For ADSP-21060/ADSP-21060C, specification is 3 ns min.

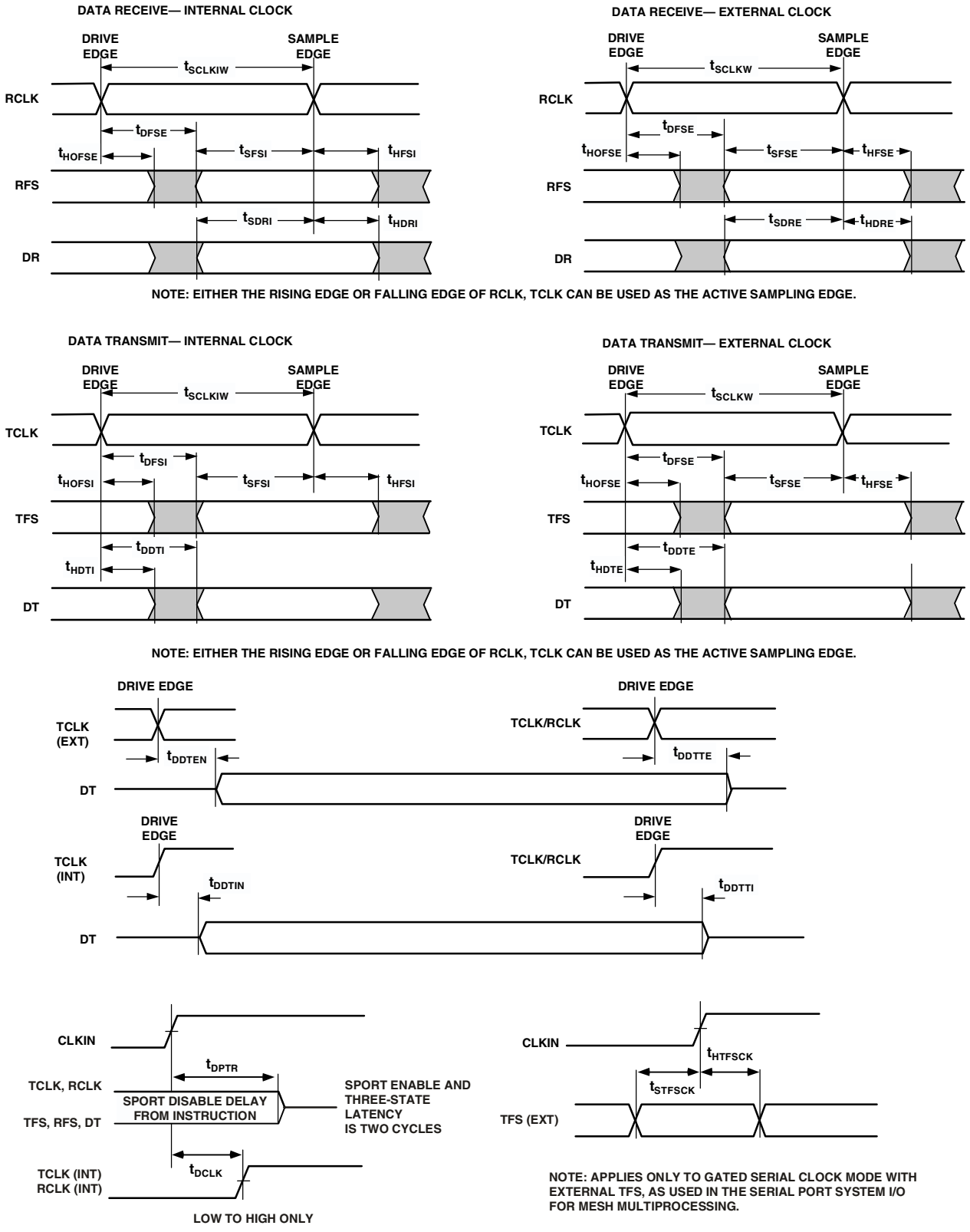

Figure 25. Serial Ports

Output Characteristics (5 V)

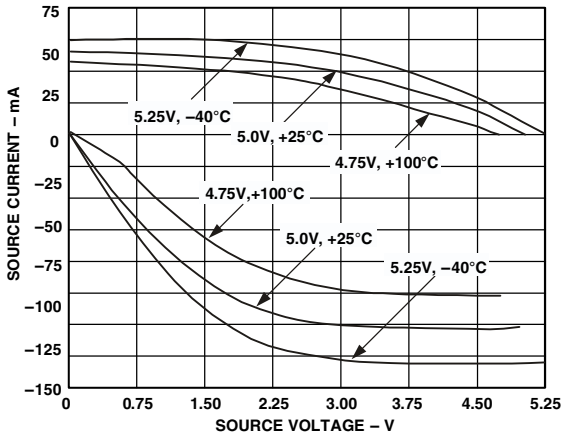

Figure 31. ADSP-21062 Typical Output Drive Currents (V_{DD} = 5 V)

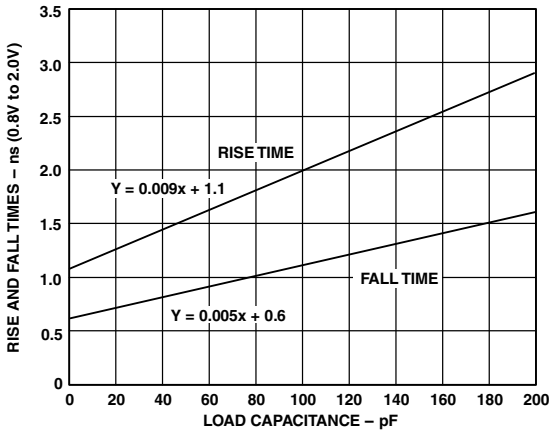

Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

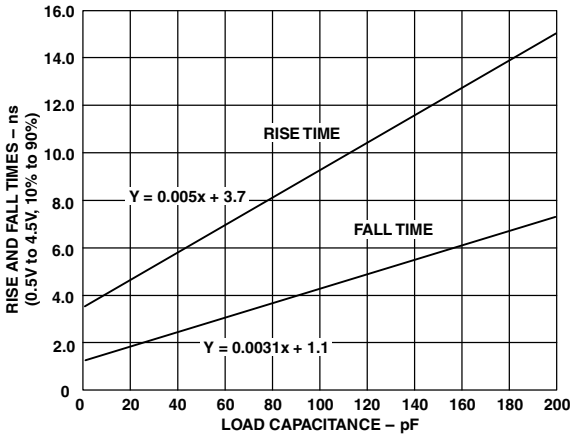

Figure 32. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

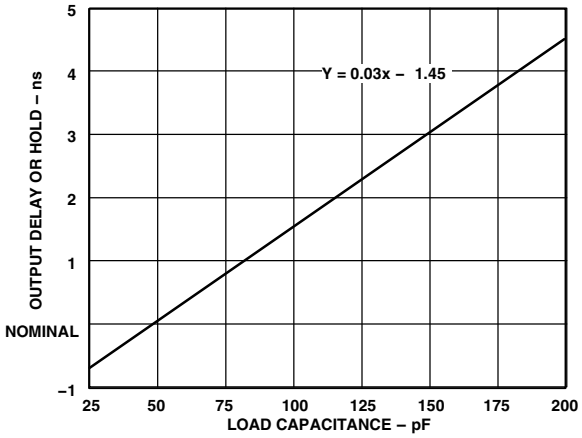

Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

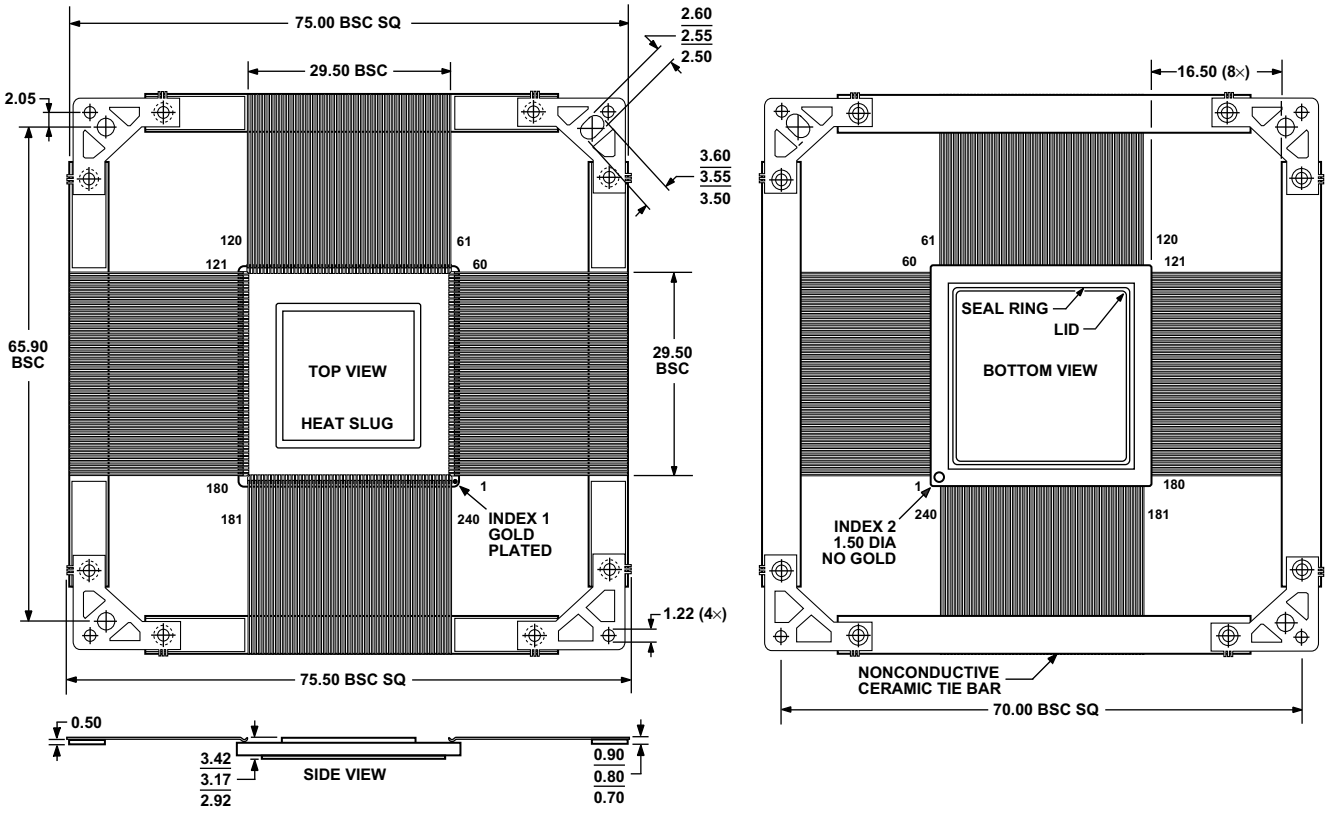

Figure 43. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Down [CQFP]
(QS-240-2B)
Dimensions shown in millimeters

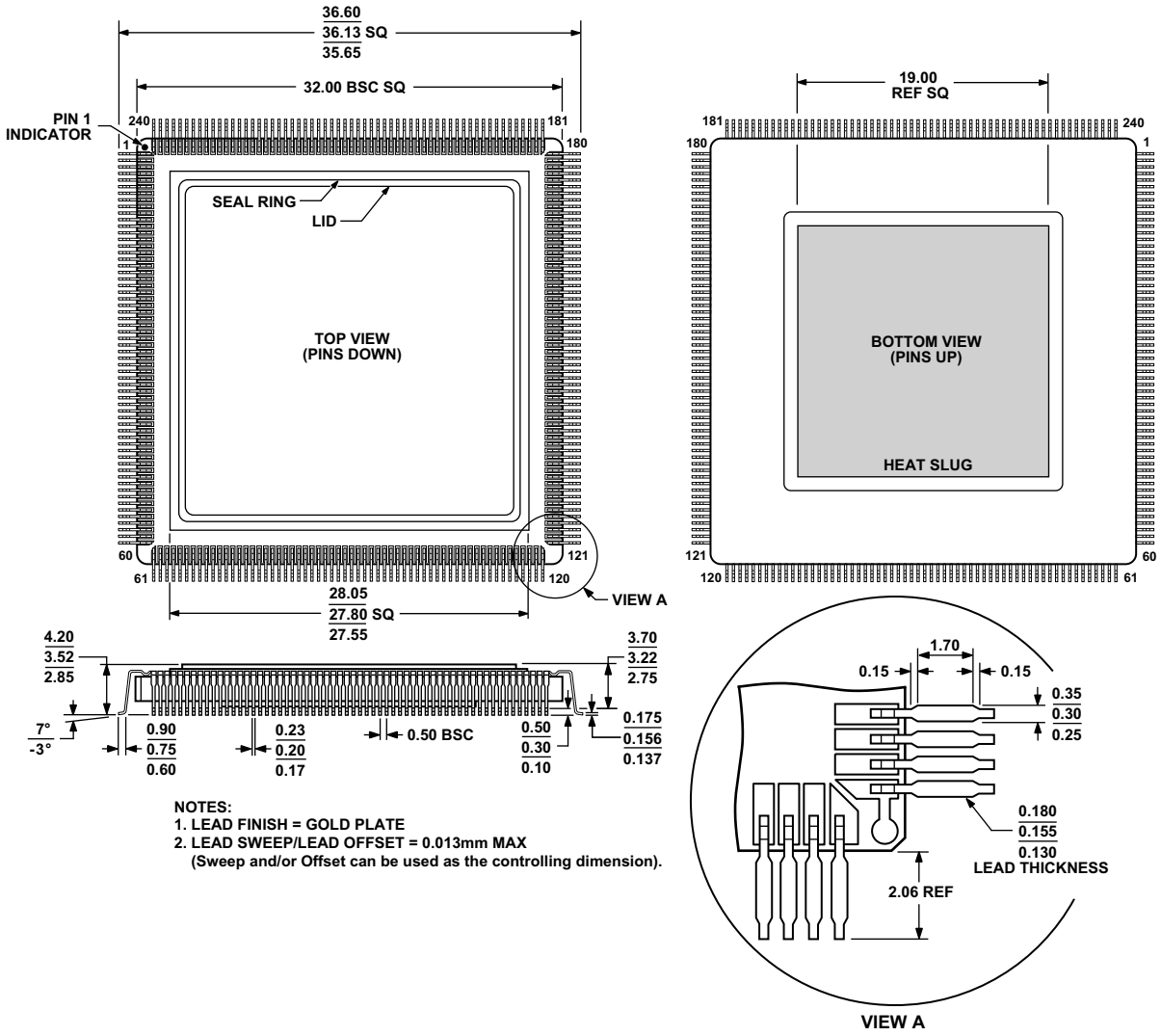

Figure 44. 240-Lead Ceramic Quad Flat Package, Heat Slug Down [CQFP]
(QS-240-1A)
Dimensions shown in millimeters