Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	256kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21062ks-160

PARALLEL COMPUTATIONS

Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch

Multiply with add and subtract for accelerated FFT butterfly computation

UP TO 4M BIT ON-CHIP SRAM

Dual-ported for independent access by core processor and DMA

OFF-CHIP MEMORY INTERFACING

4 gigawords addressable

Programmable wait state generation, page-mode DRAM support

DMA CONTROLLER

10 DMA channels for transfers between ADSP-2106x internal memory and external memory, external peripherals, host processor, serial ports, or link ports

Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

HOST PROCESSOR INTERFACE TO 16- AND 32-BIT MICROPROCESSORS

Host can directly read/write ADSP-2106x internal memory and IOP registers

MULTIPROCESSING

Glueless connection for scalable DSP multiprocessing architecture

Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-2106xs plus host

Six link ports for point-to-point connectivity and array multiprocessing

240 MBps transfer rate over parallel bus

240 MBps transfer rate over link ports

SERIAL PORTS

Two 40 Mbps synchronous serial ports with companding hardware

Independent transmit and receive functions

Table 1. ADSP-2106x SHARC Processor Family Features

Feature	ADSP-21060	ADSP-21062	ADSP-21060L	ADSP-21062L	ADSP-21060C	ADSP-21060LC
SRAM	4M bits	2M bits	4M bits	2M bits	4M bits	4M bits
Operating Voltage	5 V	5 V	3.3 V	3.3 V	5 V	3.3 V
Instruction Rate	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz
Package	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	CQFP	CQFP

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-2106x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2106x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-2106x's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2106x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2106x can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2106x processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21062/ADSP-21062L contains two megabits of on-chip SRAM, and the ADSP-21060/ADSP-21060L contains 4M bits of on-chip SRAM. The internal memory is organized as two equal sized blocks of 1M bit each for the ADSP-21062/ADSP-21062L and two equal sized blocks of 2M bits each for the ADSP-21060/ADSP-21060L. Each can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

On the ADSP-21062/ADSP-21062L, the memory can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 40k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words.

On the ADSP-21060/ADSP-21060L, the memory can be configured as a maximum of 128k words of 32-bit data, 256k words of 16-bit data, 80k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-bit, 32-bit or 48-bit words.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

On-Chip Memory and Peripherals Interface

The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold and disable time requirements.

Host Processor Interface

The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-2106x's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

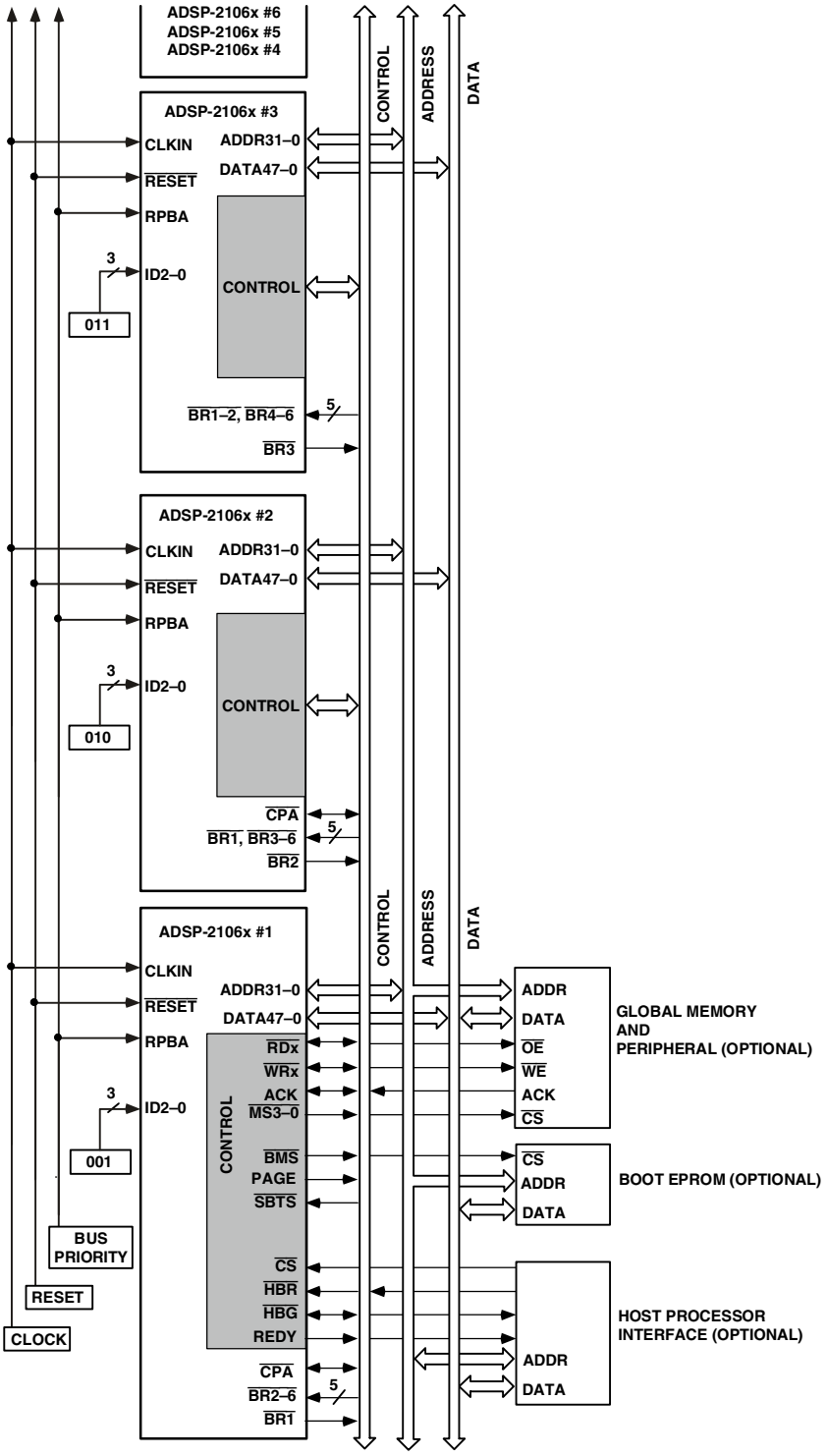

Figure 3. Shared Memory Multiprocessing System

Link Ports

The ADSP-2106x features six 4-bit link ports that provide additional I/O capabilities. The link ports can be clocked twice per cycle, allowing each to transfer eight bits of data per cycle. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems.

The link ports can operate independently and simultaneously, with a maximum data throughput of 240M bytes/s. Link port data is packed into 32- or 48-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory.

Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Program Booting

The internal memory of the ADSP-2106x can be booted at system power-up from an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the BMS (boot memory select), EBOOT (EPROM Boot), and LBOOT (link/host boot) pins. 32-bit and 16-bit host processors can be used for booting. The processor also supports a no-boot mode in which instruction execution is sourced from the external memory.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Table 3. Pin Descriptions (Continued)

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
LxDAT3–0	I/O	**Link Port Data (Link Ports 0–5).** Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
LxCLK	I/O	**Link Port Clock (Link Ports 0–5).** Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
LxACK	I/O	**Link Port Acknowledge (Link Ports 0–5).** Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-2106x is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot.** When LBOOT is high, the ADSP-2106x is configured for link port booting. When LBOOT is low, the ADSP-2106x is configured for host processor booting or no booting. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/OT	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-2106x will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). *EBOOT* *LBOOT* *$\overline{\text{BMS}}$* *Booting Mode* 1 0 Output EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) 0 0 1 (Input) Host Processor 0 1 1 (Input) Link Port 0 0 0 (Input) No Booting. Processor executes from external memory. 0 1 0 (Input) Reserved 1 1 x (Input) Reserved
CLKIN	I	**Clock In.** External clock input to the ADSP-2106x. The instruction cycle rate is equal to CLKIN. CLKIN should not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-2106x to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2106x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O	**Emulation Status.** Must be connected to the ADSP-2106x EZ-ICE target board connector only.
ICSA	O	**Reserved,** leave unconnected.
VDD	P	**Power Supply;** nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices. (30 pins).
GND	G	**Power Supply Return.** (30 pins).
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

ADSP-21060/ADSP-21062 SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (5 V)

Parameter	Description	A Grade		C Grade		K Grade		Unit
		Min	Max	Min	Max	Min	Max	
V_{DD}	Supply Voltage	4.75	5.25	4.75	5.25	4.75	5.25	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2}$–0, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31-0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 31, Output Drive Currents 5 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

EXTERNAL POWER DISSIPATION (5 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 5. External Power Calculations (5 V Devices)

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 25 V	= 0.084 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	–	× 44.7 pF	× 20 MHz	× 25 V	= 0.022 W
Data	32	50	× 14.7 pF	× 10 MHz	× 25 V	= 0.059 W
ADDRCLK	1	–	× 4.7 pF	× 20 MHz	× 25 V	= 0.002 W
						P_{EXT} = 0.167 W

ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade Min	A Grade Max	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	3.15	3.45	3.15	3.45	3.15	3.45	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

Clock Input

Table 9. Clock Input

Parameter		ADSP-21060 ADSP-21062 40 MHz, 5 V Min	ADSP-21060 ADSP-21062 40 MHz, 5 V Max	ADSP-21060 ADSP-21062 33 MHz, 5 V Min	ADSP-21060 ADSP-21062 33 MHz, 5 V Max	ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Min	ADSP-21060L ADSP-21062L 40 MHz, 3.3 V Max	ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Min	ADSP-21060L ADSP-21062L 33 MHz, 3.3 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	25	100	30	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		8.75		8.75[1]		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

[1] For the ADSP-21060LC, this specification is 9.5 ns min.

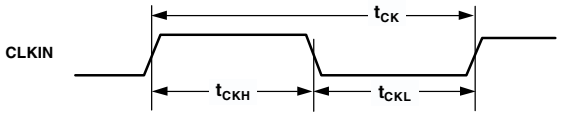

Figure 9. Clock Input

Reset

Table 10. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

[2] Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

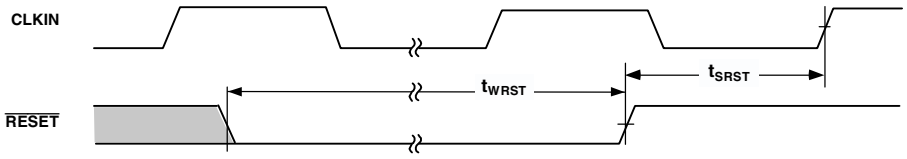

Figure 10. Reset

Interrupts

Table 11. Interrupts

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulse Width[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

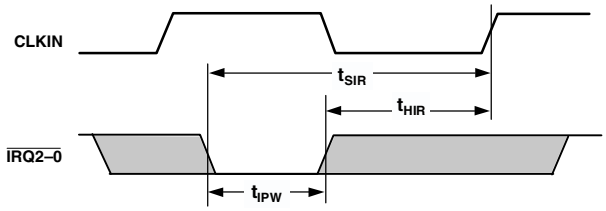

Figure 11. Interrupts

Timer

Table 12. Timer

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

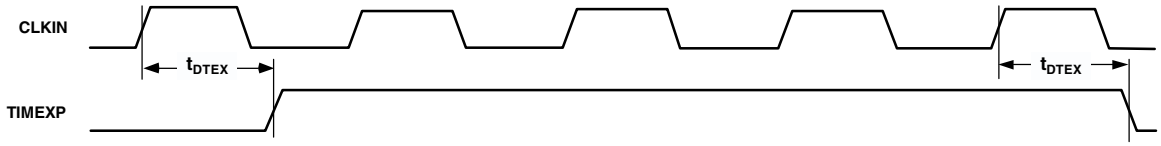

Figure 12. Timer

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 30). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 16. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	3 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[1, 2]		14 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[2]	6.5 + DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		7 – DT/8	ns
t_{HADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	–2 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	–3 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	8 + DT/4	12.5 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.

[2] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

[3] See Example System Hold Time Calculation on Page 48 for calculation of hold times given capacitive and dc loads.

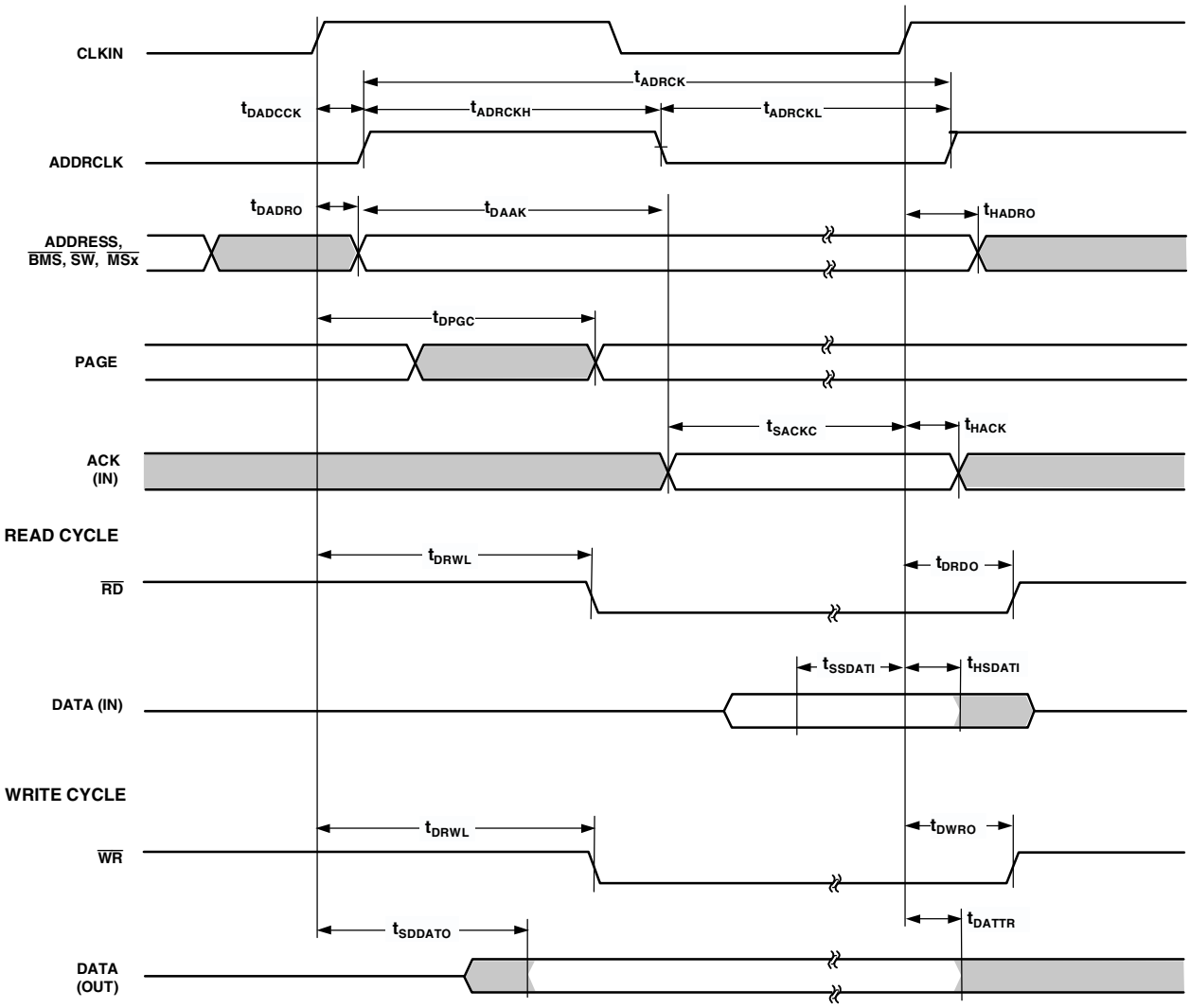

Figure 16. Synchronous Read/Write—Bus Master

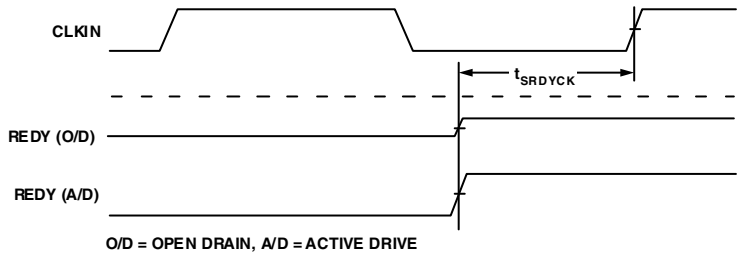

Figure 19. Synchronous REDY Timing

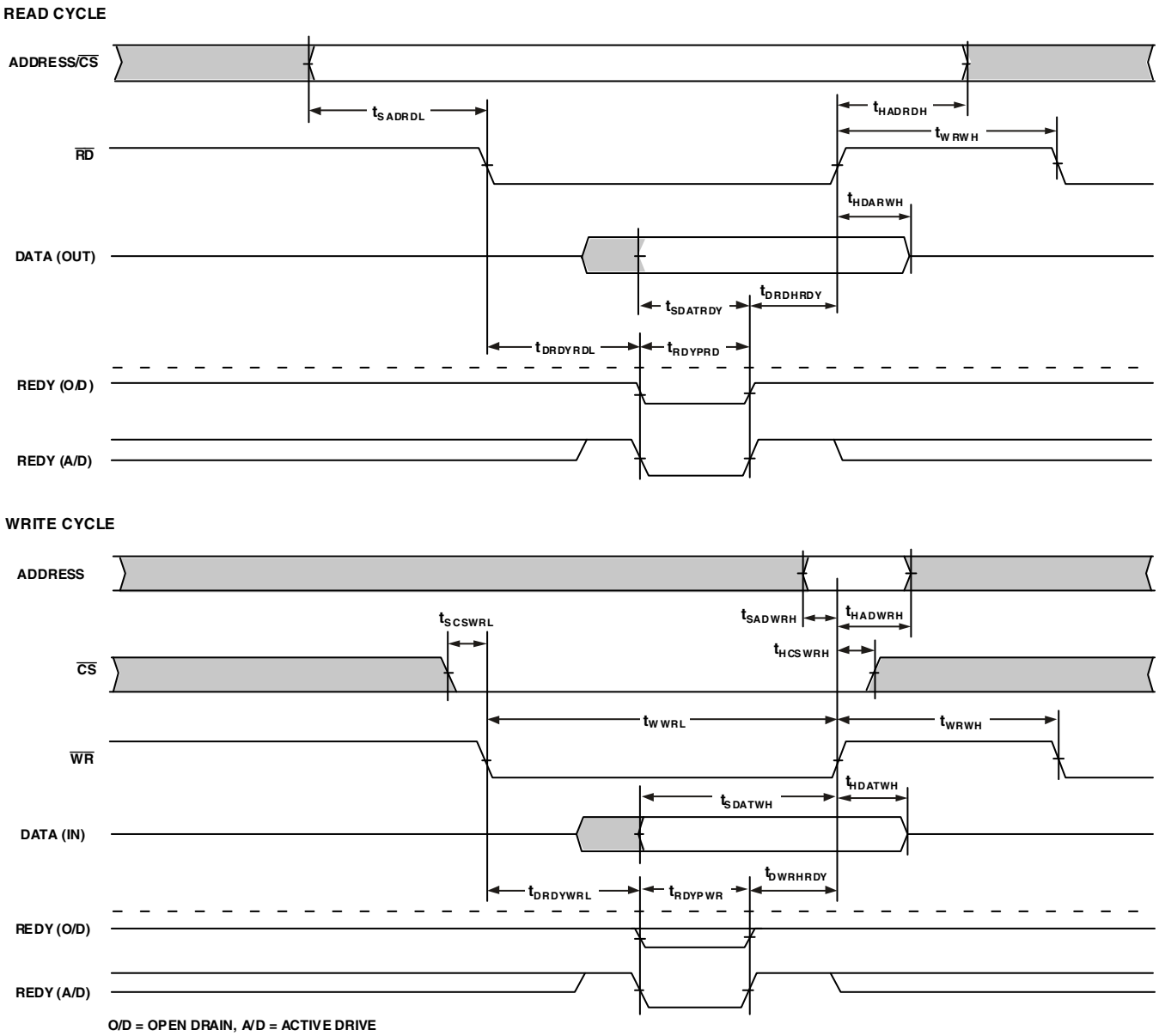

Figure 20. Asynchronous Read/Write—Host to ADSP-2106x

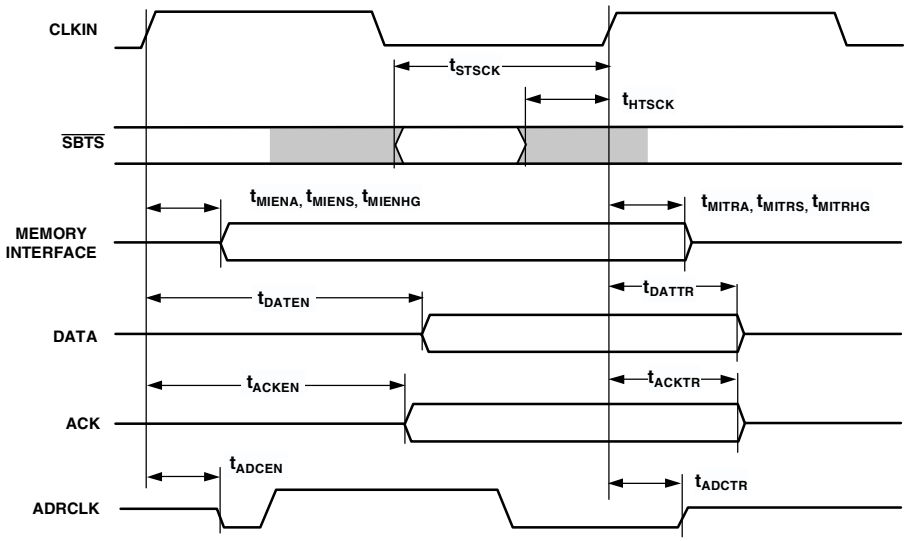

Figure 22. Three-State Timing (Bus Transition Cycle, $\overline{SBTS}$ Assertion)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DATA42	DATA44	DATA47	$\overline{BR3}$	PAGE	CLKIN	$\overline{CS}$	ADRCLK	RCLK0	TCLK0	RCLK1	DT1	$\overline{DMAR2}$	ADDR30	$\overline{BMS}$	A
DATA39	DATA43	DATA45	$\overline{BR2}$	$\overline{BR6}$	ACK	$\overline{RD}$	REDY	DR0	DT0	DR1	$\overline{HBR}$	ADDR31	$\overline{SW}$	$\overline{MS0}$	B
DATA36	DATA38	DATA41	DATA46	$\overline{BR4}$	$\overline{DMAG1}$	$\overline{WR}$	RFS0	TFS0	RFS1	TCLK1	$\overline{SBTS}$	ADDR28	$\overline{MS1}$	$\overline{MS3}$	C
DATA34	DATA35	DATA37	DATA40	$\overline{BR1}$	$\overline{BR5}$	$\overline{DMAG2}$	$\overline{HBG}$	$\overline{CPA}$	TFS1	$\overline{DMAR1}$	ADDR29	$\overline{MS2}$	ADDR26	ADDR25	D
DATA31	DATA32	DATA30	DATA33	NC	GND	GND	GND	GND	GND	GND	ADDR27	ADDR24	ADDR22	ADDR21	E
DATA27	DATA28	DATA26	DATA29	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	GND	ADDR23	ADDR20	ADDR18	ADDR17	F
DATA23	DATA24	DATA25	DATA22	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR19	ADDR16	ADDR15	ADDR14	G
DATA20	DATA21	DATA19	DATA18	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR10	ADDR13	ADDR11	ADDR12	H
DATA17	DATA16	DATA15	DATA12	GND	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GND	ADDR4	ADDR7	ADDR8	ADDR9	J
DATA14	DATA13	DATA11	DATA8	GND	GND	V_{DD}	V_{DD}	V_{DD}	GND	ICSA	ADDR0	ADDR3	ADDR5	ADDR6	K
DATA10	DATA9	DATA7	DATA4	NC	GND	GND	GND	GND	GND	RPBA	FLAG3	FLAG0	ADDR1	ADDR2	L
DATA6	DATA5	DATA2	L0DAT0	L1DAT1	L2DAT3	L3DAT0	L4DAT2	L5DAT2	L5ACK	LBOOT	TDI	TIMEXP	FLAG2	FLAG1	M
DATA3	DATA1	L0DAT3	L1DAT3	L1ACK	L2DAT0	L3DAT3	L3CLK	L4CLK	L5DAT1	ID2	$\overline{IRQ1}$	$\overline{IRQ0}$	TDO	$\overline{EMU}$	N
DATA0	L0DAT1	L0ACK	L1DAT0	L2DAT2	L2CLK	L3DAT2	L4DAT3	L4DAT0	L5DAT3	L5CLK	ID0	EBOOT	TMS	$\overline{TRST}$	P
L0DAT2	L0CLK	L1DAT2	L1CLK	L2DAT1	L2ACK	L3DAT1	L3ACK	L4DAT1	L4ACK	L5DAT0	ID1	$\overline{RESET}$	$\overline{IRQ2}$	TCK	R

Figure 39. ADSP-21060/ADSP-21062 PBGA Ball Assignments (Top View, Summary)

Table 42. ADSP-21060CW/21060LCW CQFP Pin Assignments (QS-240-1A, QS-240-1B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
GND	1	DATA29	41	$\overline{\text{DMAG2}}$	81	ADDR28	121	ADDR5	161	GND	201
DATA0	2	GND	42	ACK	82	$\overline{\text{BMS}}$	122	GND	162	V_{DD}	202
DATA1	3	DATA30	43	CLKIN	83	$\overline{\text{SW}}$	123	ADDR4	163	L4ACK	203
DATA2	4	DATA31	44	GND	84	$\overline{\text{MS0}}$	124	ADDR3	164	L4CLK	204
V_{DD}	5	DATA32	45	V_{DD}	85	$\overline{\text{MS1}}$	125	ADDR2	165	L4DAT0	205
DATA3	6	GND	46	GND	86	$\overline{\text{MS2}}$	126	V_{DD}	166	L4DAT1	206
DATA4	7	V_{DD}	47	$\overline{\text{WR}}$	87	$\overline{\text{MS3}}$	127	ADDR1	167	L4DAT2	207
DATA5	8	V_{DD}	48	$\overline{\text{RD}}$	88	GND	128	ADDR0	168	L4DAT3	208
GND	9	DATA33	49	$\overline{\text{CS}}$	89	ADDR27	129	GND	169	GND	209
DATA6	10	DATA34	50	$\overline{\text{HBG}}$	90	ADDR26	130	FLAG0	170	L3ACK	210
DATA7	11	DATA35	51	REDY	91	ADDR25	131	FLAG1	171	L3CLK	211
DATA8	12	NC	52	ADRCLK	92	V_{DD}	132	FLAG2	172	L3DAT0	212
V_{DD}	13	GND	53	GND	93	GND	133	FLAG3	173	L3DAT1	213
DATA9	14	DATA36	54	V_{DD}	94	V_{DD}	134	ICSA	174	L3DAT2	214
DATA10	15	DATA37	55	V_{DD}	95	ADDR24	135	$\overline{\text{EMU}}$	175	L3DAT3	215
DATA11	16	DATA38	56	RFS0	96	ADDR23	136	TIMEXP	176	V_{DD}	216
GND	17	V_{DD}	57	RCLK0	97	ADDR22	137	TDO	177	NC	217
DATA12	18	DATA39	58	DR0	98	GND	138	V_{DD}	178	L2ACK	218
DATA13	19	DATA40	59	TFS0	99	ADDR21	139	$\overline{\text{TRST}}$	179	L2CLK	219
DATA14	20	DATA41	60	TCLK0	100	ADDR20	140	TDI	180	L2DAT0	220
V_{DD}	21	GND	61	DT0	101	ADDR19	141	TMS	181	L2DAT1	221
DATA15	22	DATA42	62	$\overline{\text{CPA}}$	102	V_{DD}	142	TCK	182	L2DAT2	222
DATA16	23	DATA43	63	GND	103	V_{DD}	143	$\overline{\text{IRQ0}}$	183	L2DAT3	223
DATA17	24	DATA44	64	RFS1	104	ADDR18	144	$\overline{\text{IRQ1}}$	184	V_{DD}	224
GND	25	V_{DD}	65	RCLK1	105	ADDR17	145	$\overline{\text{IRQ2}}$	185	GND	225
DATA18	26	DATA45	66	DR1	106	ADDR16	146	EBOOT	186	GND	226
DATA19	27	DATA46	67	TFS1	107	GND	147	$\overline{\text{RESET}}$	187	L1ACK	227
DATA20	28	DATA47	68	TCLK1	108	ADDR15	148	RPBA	188	L1CLK	228
V_{DD}	29	GND	69	DT1	109	ADDR14	149	LBOOT	189	L1DAT0	229
DATA21	30	V_{DD}	70	$\overline{\text{HBR}}$	110	V_{DD}	150	ID0	190	L1DAT1	230
DATA22	31	GND	71	$\overline{\text{DMAR1}}$	111	ADDR13	151	ID1	191	L1DAT2	231
DATA23	32	$\overline{\text{BR1}}$	72	$\overline{\text{DMAR2}}$	112	ADDR12	152	ID2	192	L1DAT3	232
GND	33	$\overline{\text{BR2}}$	73	$\overline{\text{SBTS}}$	113	ADDR11	153	GND	193	V_{DD}	233
DATA24	34	$\overline{\text{BR3}}$	74	GND	114	GND	154	L5ACK	194	L0ACK	234
DATA25	35	$\overline{\text{BR4}}$	75	ADDR31	115	ADDR10	155	L5CLK	195	L0CLK	235
DATA26	36	$\overline{\text{BR5}}$	76	ADDR30	116	ADDR9	156	L5DAT0	196	L0DAT0	236
V_{DD}	37	$\overline{\text{BR6}}$	77	ADDR29	117	ADDR8	157	L5DAT1	197	L0DAT1	237
V_{DD}	38	V_{DD}	78	V_{DD}	118	V_{DD}	158	L5DAT2	198	L0DAT2	238
DATA27	39	PAGE	79	V_{DD}	119	ADDR7	159	L5DAT3	199	L0DAT3	239
DATA28	40	$\overline{\text{DMAG1}}$	80	GND	120	ADDR6	160	V_{DD}	200	GND	240

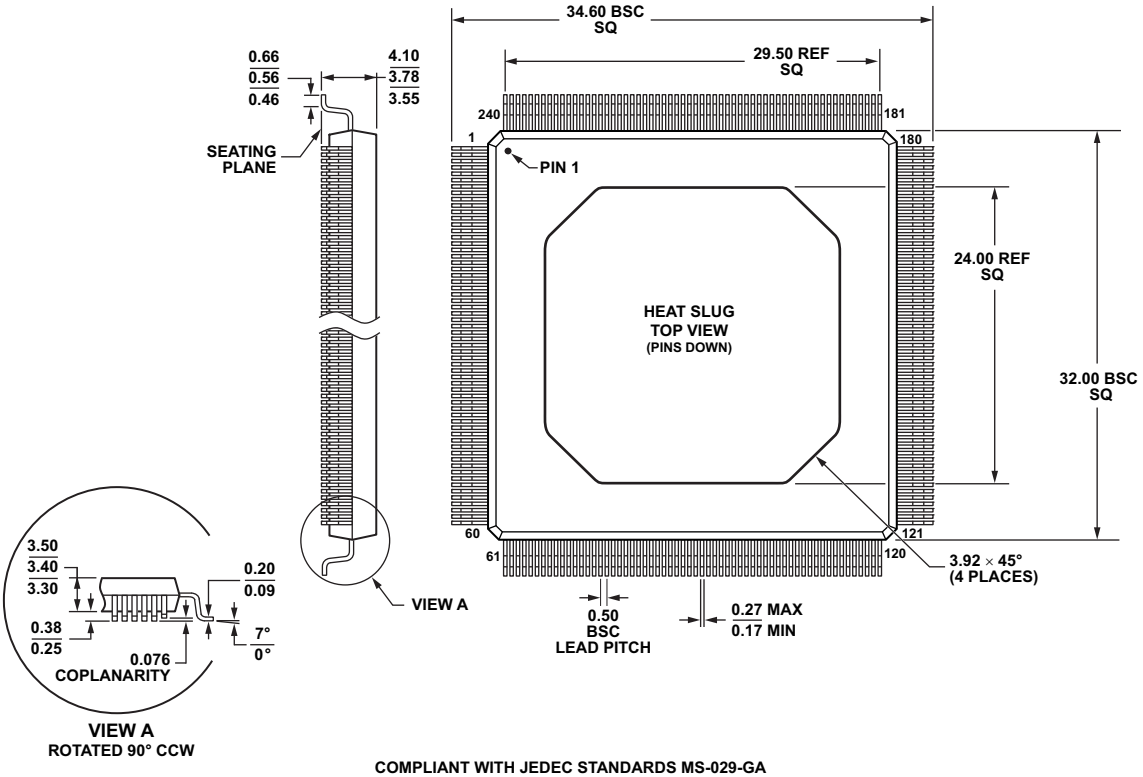

Figure 41. 240-Lead Metric Quad Flat Package, Thermally Enhanced "PowerQuad" [MQFP_PQ4]
(SP-240-2)
Dimensions shown in millimeters

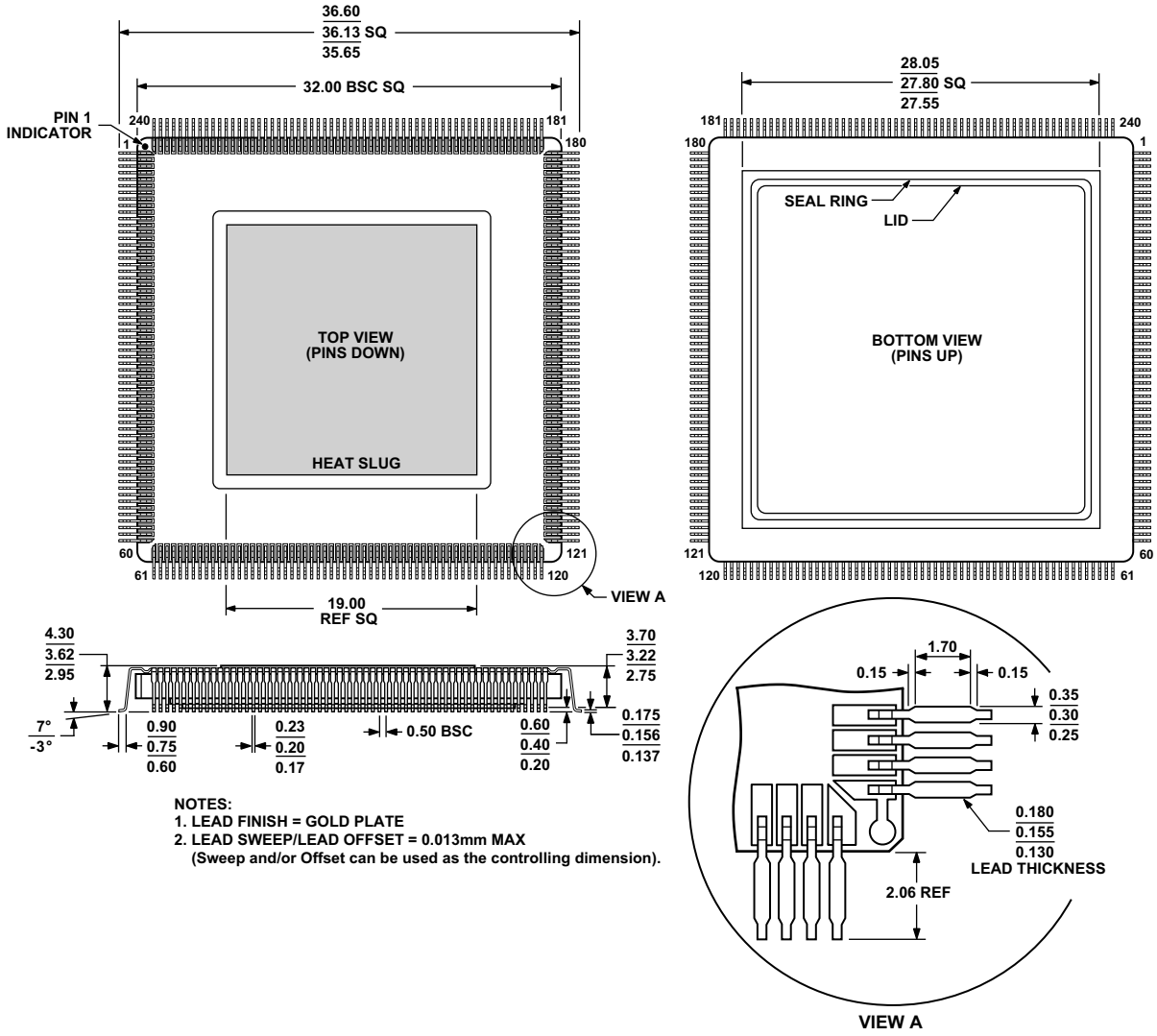

Figure 42. 240-Lead Ceramic Quad Flat Package, Heat Slug Up [CQFP]
(QS-240-2A)
Dimensions shown in millimeters

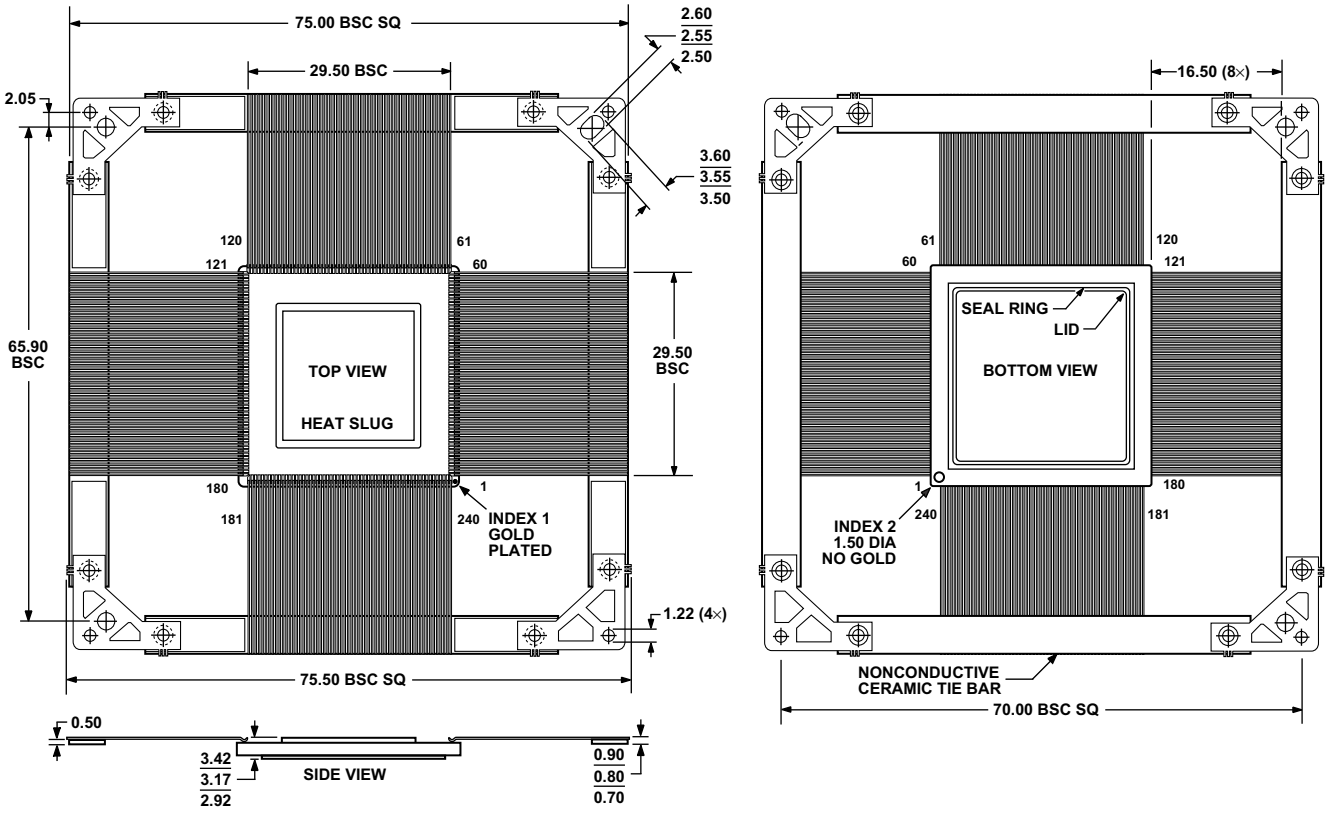

Figure 43. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Down [CQFP]
(QS-240-2B)
Dimensions shown in millimeters