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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	256kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21062ksz-160

PARALLEL COMPUTATIONS

Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch

Multiply with add and subtract for accelerated FFT butterfly computation

UP TO 4M BIT ON-CHIP SRAM

Dual-ported for independent access by core processor and DMA

OFF-CHIP MEMORY INTERFACING

4 gigawords addressable

Programmable wait state generation, page-mode DRAM support

DMA CONTROLLER

10 DMA channels for transfers between ADSP-2106x internal memory and external memory, external peripherals, host processor, serial ports, or link ports

Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

HOST PROCESSOR INTERFACE TO 16- AND 32-BIT MICROPROCESSORS

Host can directly read/write ADSP-2106x internal memory and IOP registers

MULTIPROCESSING

Glueless connection for scalable DSP multiprocessing architecture

Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-2106xs plus host

Six link ports for point-to-point connectivity and array multiprocessing

240 MBps transfer rate over parallel bus

240 MBps transfer rate over link ports

SERIAL PORTS

Two 40 Mbps synchronous serial ports with companding hardware

Independent transmit and receive functions

Table 1. ADSP-2106x SHARC Processor Family Features

Feature	ADSP-21060	ADSP-21062	ADSP-21060L	ADSP-21062L	ADSP-21060C	ADSP-21060LC
SRAM	4M bits	2M bits	4M bits	2M bits	4M bits	4M bits
Operating Voltage	5 V	5 V	3.3 V	3.3 V	5 V	3.3 V
Instruction Rate	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz	33 MHz 40 MHz
Package	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	MQFP_PQ4 PBGA	CQFP	CQFP

GENERAL DESCRIPTION

The ADSP-2106x SHARC®—Super Harvard Architecture Computer—is a 32-bit signal processing microcomputer that offers high levels of DSP performance. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 2 shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including up to 4M bit SRAM memory (see Table 1), a host processor interface, DMA controller, serial ports and link port, and parallel bus connectivity for glueless DSP multiprocessing.

Table 2. Benchmarks (at 40 MHz)

Benchmark Algorithm	Speed	Cycles
1024 Point Complex FFT (Radix 4, with reversal)	0.46 μs	18,221
FIR Filter (per tap)	25 ns	1
IIR Filter (per biquad)	100 ns	4
Divide (y/x)	150 ns	6
Inverse Square Root	225 ns	9
DMA Transfer Rate	240 Mbytes/s	

The ADSP-2106x continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1 illustrates the following architectural features:

- Computation units (ALU, multiplier and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Interval timer
- On-chip SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and multiprocessor Interface
- DMA controller
- Serial ports and link ports
- JTAG Test Access Port

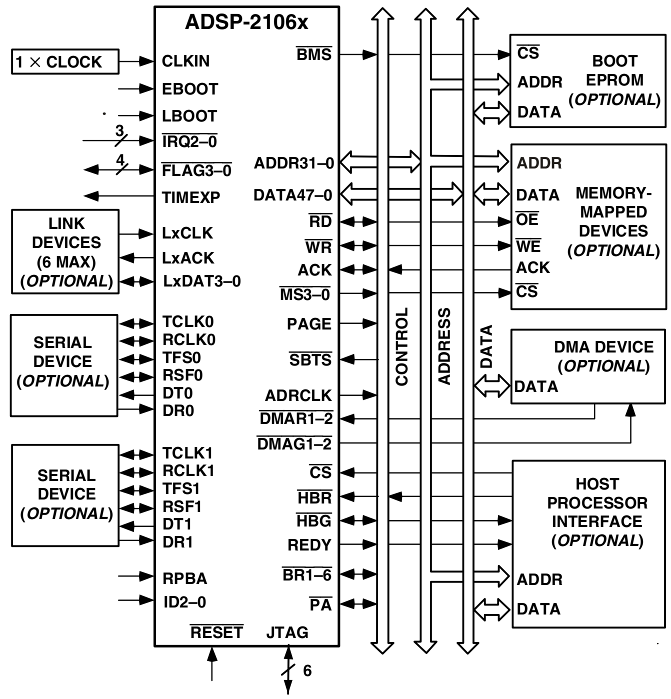

Figure 2. ADSP-2106x System Sample Configuration

SHARC FAMILY CORE ARCHITECTURE

The ADSP-2106x includes the following architectural features of the ADSP-21000 family core.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general–purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

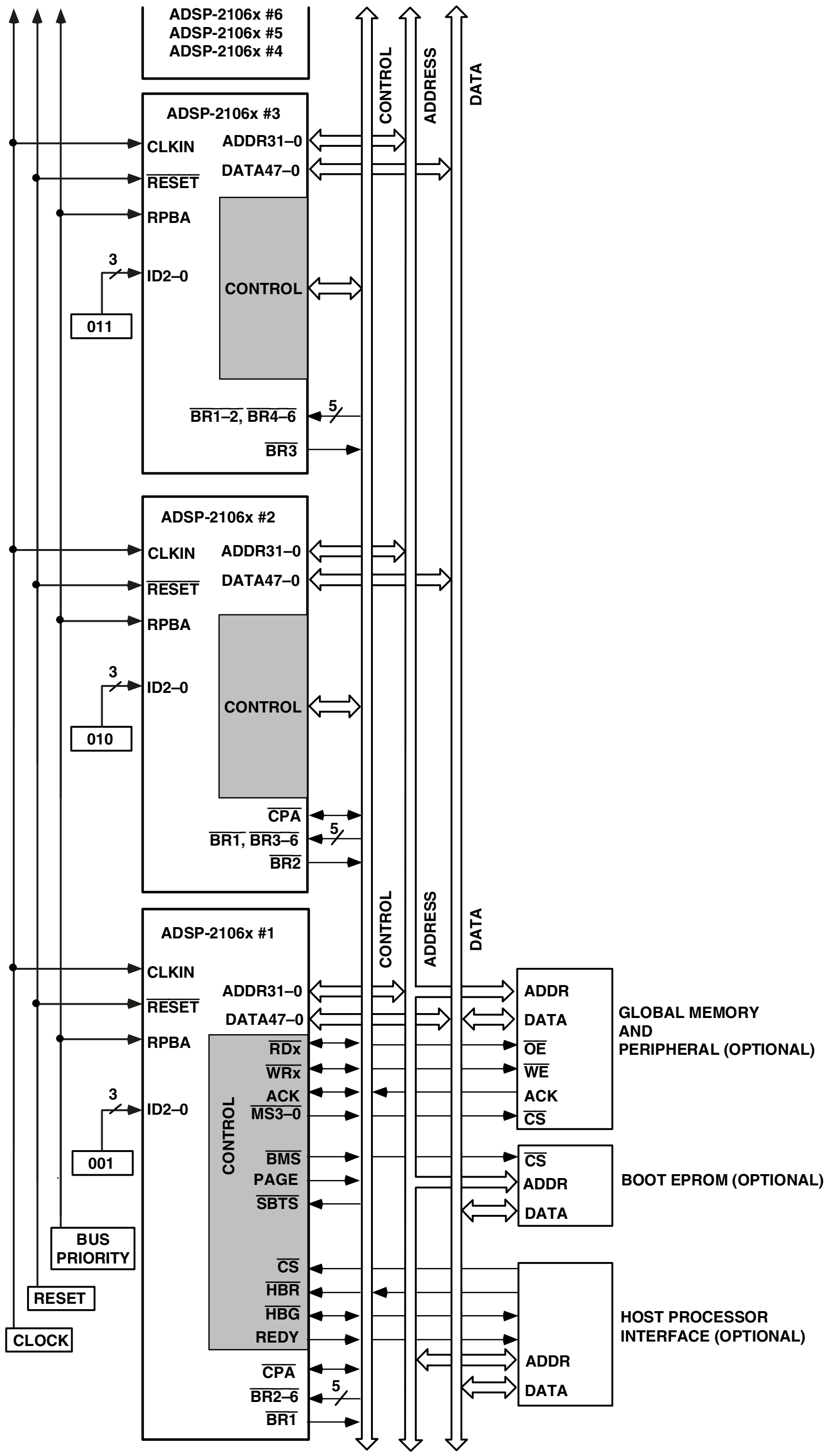

Figure 3. Shared Memory Multiprocessing System

PIN FUNCTION DESCRIPTIONS

The ADSP-2106x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31–0, DATA47–0, FLAG3–0, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, LxDAT3–0, LxCLK, LxACK, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 3. Pin Descriptions

Pin	Type	Function
ADDR31–0	I/O/T	**External Bus Address.** The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
DATA47–0	I/O/T	**External Bus Data.** The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47–8 of the bus. 16-bit short word data is transferred over bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23–16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS3–0}}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The $\overline{\text{MS3–0}}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{\text{MS3–0}}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{\text{MS0}}$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{\text{MS3–0}}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert $\overline{\text{RD}}$ to read from the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-2106x's internal memory. In a multiprocessing system, $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

ADSP-21060/ADSP-21062 SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (5 V)

Parameter	Description	A Grade Min	A Grade Max	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.75	5.25	4.75	5.25	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	μA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	μA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31-0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See Figure 31, Output Drive Currents 5 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios.

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 Per Cycle (DM and PM)	1 Per Cycle (DM)	None
Internal Memory DMA	1 Per Cycle	1 Per 2 Cycles	1 Per 2 Cycles

To estimate power consumption for a specific application, use the following equation where% is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = Power\ Consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	745	mA
	t_{CK} = 25 ns, V_{DD} = Max	850	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	575	mA
	t_{CK} = 25 ns, V_{DD} = Max	670	mA
$I_{DDINLOW}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	340	mA
	t_{CK} = 25 ns, V_{DD} = Max	390	mA
I_{DDIDLE} Supply Current (Idle)[3]	V_{DD} = Max	200	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] Idle denotes ADSP-2106x state during execution of IDLE instruction.

ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade Min	A Grade Max	C Grade Min	C Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	3.15	3.45	3.15	3.45	3.15	3.45	V
T_{CASE}	Case Operating Temperature	–40	+85	–40	+100	–40	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: DATA47–0, ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, ACK, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2–0}}$, FLAG3–0, $\overline{\text{HGB}}$, $\overline{\text{CS}}$, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{BR6–1}}$, ID2–0, RPBA, $\overline{\text{CPA}}$, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, EBOOT, LBOOT, $\overline{\text{BMS}}$, TMS, TDI, TCK, $\overline{\text{HBR}}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	μA
I_{OZL}[5, 9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	μA
I_{OZHP}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	μA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[10]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	μA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	μA
C_{IN}[11, 12]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–0, ADDR31–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, ADRCLK, $\overline{\text{SW}}$, ACK, FLAG3–0, TIMEXP, $\overline{\text{HBG}}$, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BR6–1}}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3–0, LxCLK, LxACK, $\overline{\text{BMS}}$, TDO, $\overline{\text{EMU}}$, ICSA.

[2] See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2–0}}$, $\overline{\text{HBR}}$, $\overline{\text{CS}}$, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, ID2–0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{\text{RESET}}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{\text{TRST}}$, TMS, TDI.

[5] Applies to three-statable pins: DATA47–0, ADDR31–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, ADRCLK, $\overline{\text{SW}}$, ACK, FLAG3–0, $\overline{\text{HBG}}$, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BMS}}$, $\overline{\text{BR6–1}}$, TFSx, RFSx, TDO, $\overline{\text{EMU}}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106x is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{\text{CPA}}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2–0 = 001 and another ADSP-2106xL is not requesting bus mastership).

[9] Applies to three-statable pins with internal pull-downs: LxDAT3–0, LxCLK, LxACK.

[10] Applies to ACK pin when keeper latch enabled.

[11] Applies to all signal pins.

[12] Guaranteed but not tested.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

Figure 8 and Table 8 provide information on detail contained within the package marking for the ADSP-2106x processors (actual marking format may vary). For a complete listing of product availability, see Ordering Guide on Page 62.

Figure 8. Typical Package Brand

Table 8. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead (Pb) Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

The ADSP-2106x processors are available at maximum processor speeds of 33 MHz (–133), and 40 MHz (–160). The timing specifications are based on a CLKIN frequency of 40 MHz t_{CK} = 25 ns). The DT derating factor enables the calculation for timing specifications within the min to max range of the t_{CK} specification (see Table 9). DT is the difference between the derated CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25\text{ ns}$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

For voltage reference levels, see Figure 28 on Page 48 under Test Conditions.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices. (O/D) = Open Drain, (A/D) = Active Drive.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Flags

Table 13. Flags

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	8 + 5DT/16		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	0 – 5DT/16		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RD}/\overline{WR}$ Low[1]		5 + 7DT/16	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RD}/\overline{WR}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		16	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	4		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	3		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable		14	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

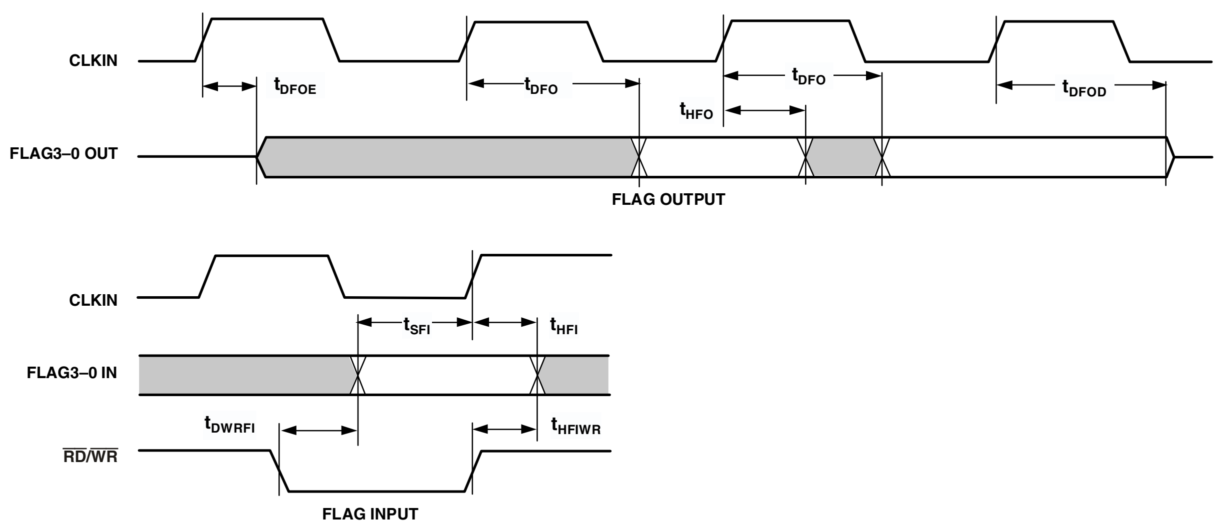

Figure 13. Flags

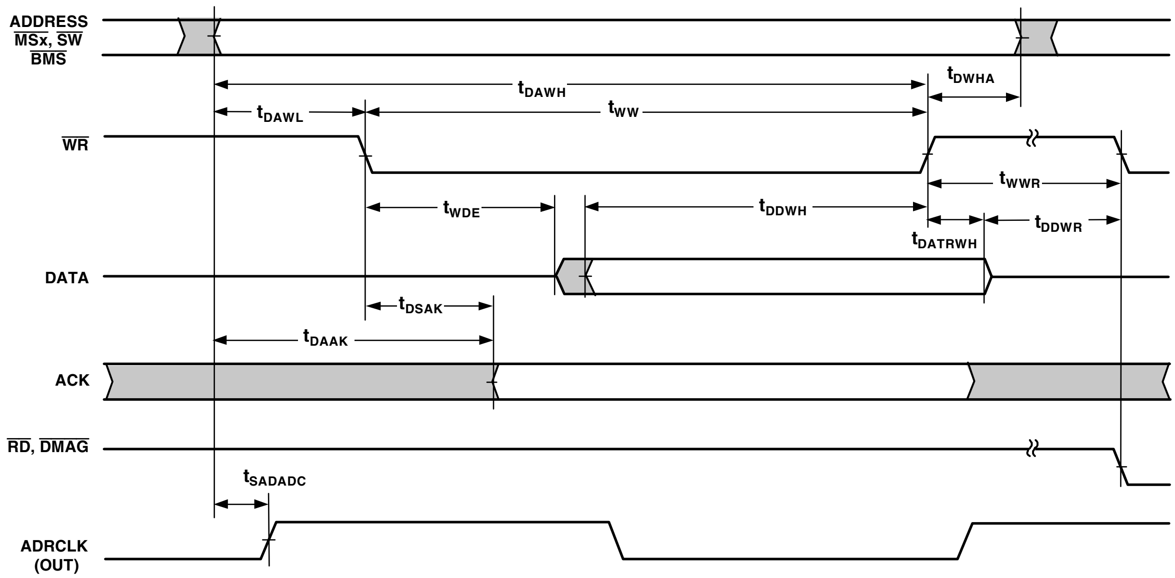

Figure 15. Memory Write—Bus Master

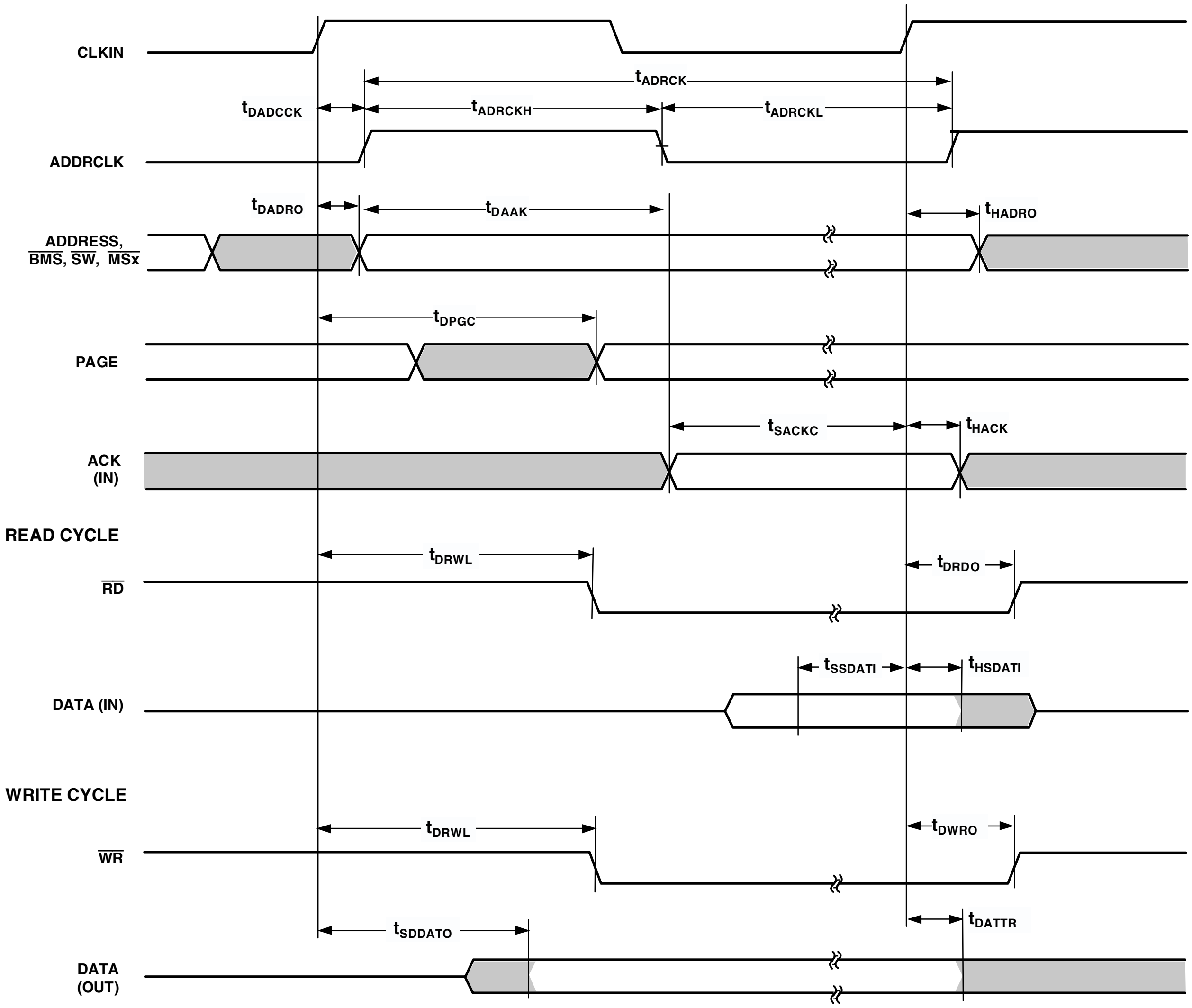

Figure 16. Synchronous Read/Write—Bus Master

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{\text{BRx}}$) or a host processor, both synchronous and asynchronous ($\overline{\text{HBR}}$, $\overline{\text{HBG}}$).

Table 18. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{\text{HBG}}$ Low to $\overline{\text{RD}}$/$\overline{\text{WR}}$/$\overline{\text{CS}}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{\text{HBR}}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{\text{HBR}}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{\text{HBG}}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{\text{HBG}}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{\text{BRx}}$, $\overline{\text{CPA}}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{\text{BRx}}$, $\overline{\text{CPA}}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	21 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{\text{HBG}}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{\text{HBG}}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{\text{BRx}}$ Delay After CLKIN		7 – DT/8	ns
t_{HBRO}	$\overline{\text{BRx}}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{\text{CPA}}$ Low Delay After CLKIN[4]		8 – DT/8	ns
t_{TRCPA}	$\overline{\text{CPA}}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ Low[5, 6]		8.5	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{\text{HBG}}$[6, 7]	44 + 23DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{\text{CS}}$ or $\overline{\text{HBR}}$ High[6]		10	ns

[1] For first asynchronous access after $\overline{\text{HBR}}$ and $\overline{\text{CS}}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{\text{RD}}$ or $\overline{\text{WR}}$ goes low or by $t_{HBGRCSV}$ after $\overline{\text{HBG}}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{\text{HBG}}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual, Revision* 2.1.

[2] Only required for recognition in the current cycle.

[3] $\overline{\text{CPA}}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For ADSP-21060LC, specification is 8.5 – DT/8 ns max.

[5] For ADSP-21060L, specification is 9.5 ns max, For ADSP-21060LC, specification is 11.0 ns max, For ADSP-21062L, specification is 8.75 ns max.

[6] (O/D) = open drain, (A/D) = active drive.

[7] For ADSP-21060C/ADSP-21060LC, specification is 40 + 23DT/16 ns min.

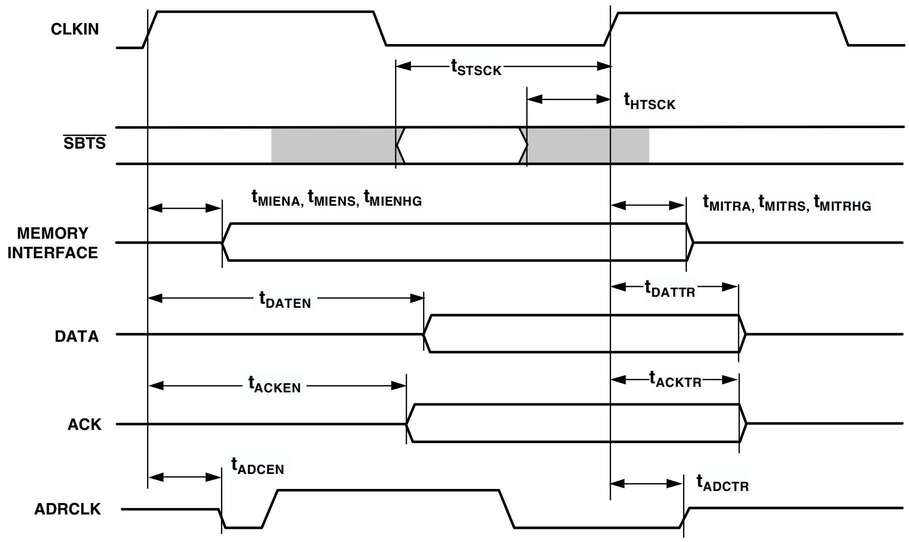

Figure 22. Three-State Timing (Bus Transition Cycle, $\overline{SBTS}$ Assertion)

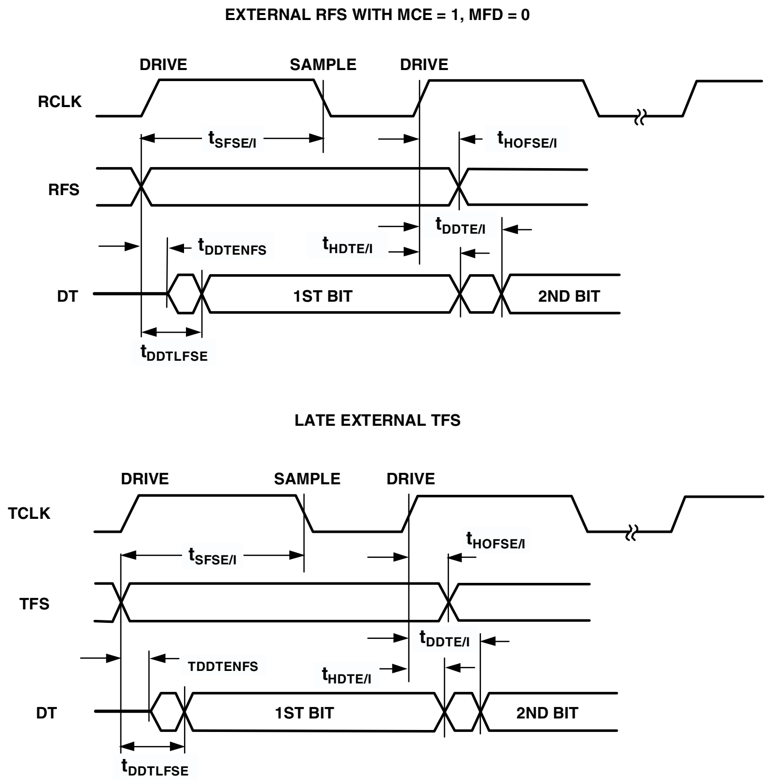

Figure 26. Serial Ports—External Late Frame Sync

Output Characteristics (5 V)

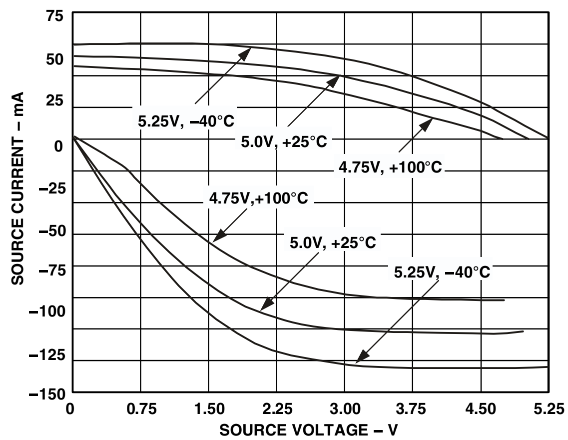

Figure 31. ADSP-21062 Typical Output Drive Currents (V_{DD} = 5 V)

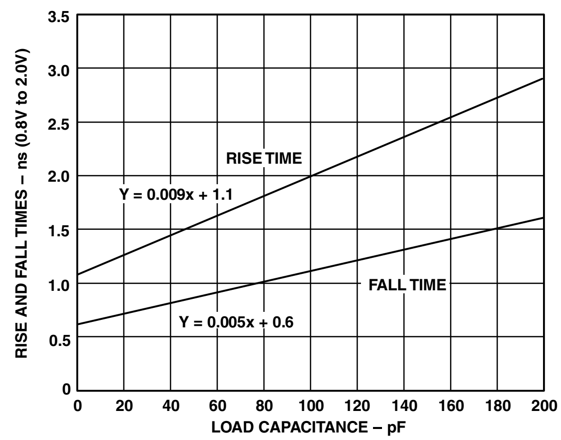

Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

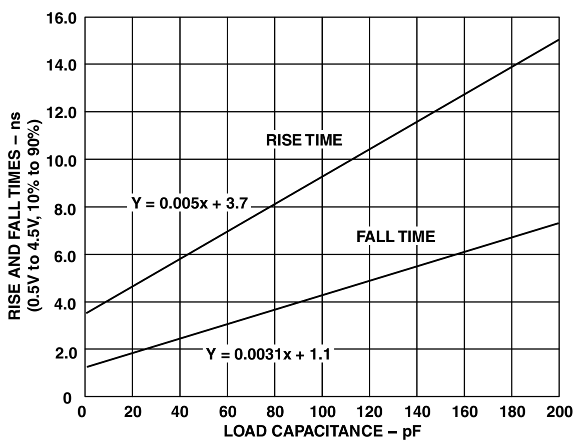

Figure 32. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

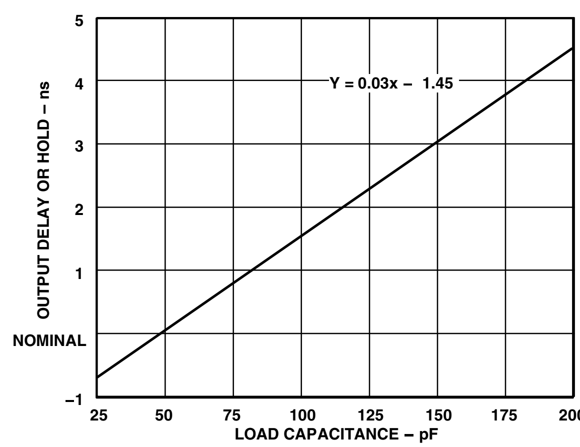

Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

Output Characteristics (3.3 V)

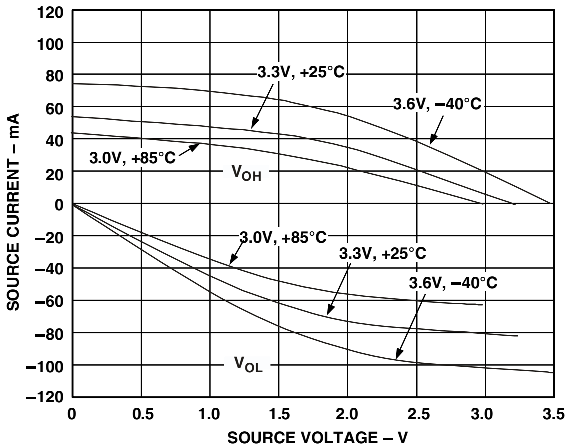

Figure 35. ADSP-21062 Typical Output Drive Currents (V_{DD} = 3.3 V)

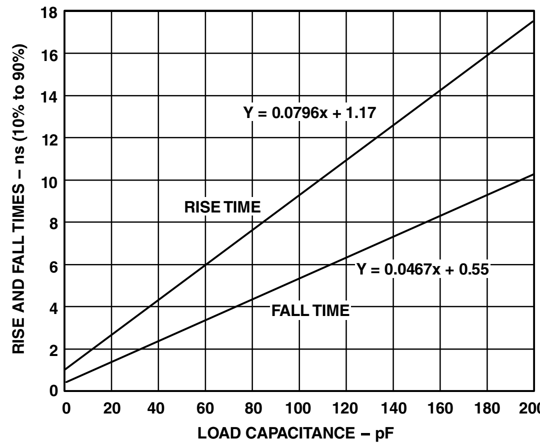

Figure 37. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

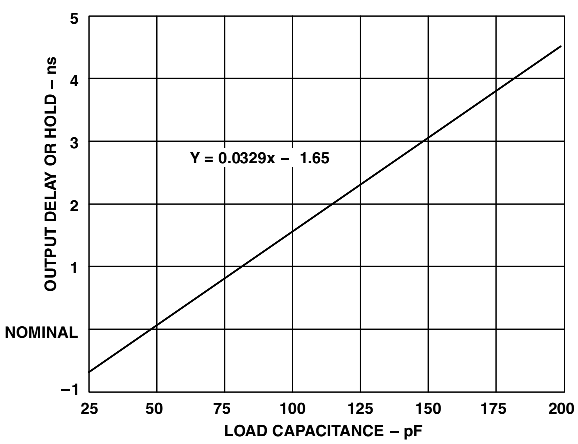

Figure 36. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

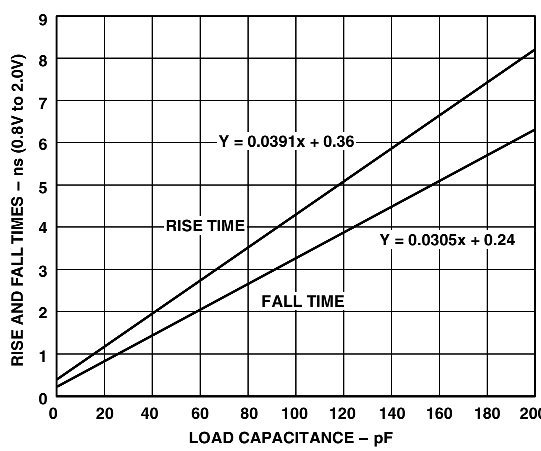

Figure 38. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	L2DAT0	201
$\overline{\text{TRST}}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	L2CLK	202
V_{DD}	3	$\overline{\text{GND}}$	43	DR0	83	DATA39	123	DATA12	163	L2ACK	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{\text{EMU}}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	L3DAT3	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	L3DAT2	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	L3DAT1	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	L3DAT0	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	L3CLK	210
FLAG0	11	ADDR26	51	$\overline{\text{HBG}}$	91	DATA34	131	DATA6	171	L3ACK	211
GND	12	ADDR27	52	$\overline{\text{CS}}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{\text{RD}}$	93	V_{DD}	133	DATA5	173	L4DAT3	213
ADDR1	14	$\overline{\text{MS3}}$	54	$\overline{\text{WR}}$	94	V_{DD}	134	DATA4	174	L4DAT2	214
V_{DD}	15	$\overline{\text{MS2}}$	55	GND	95	GND	135	DATA3	175	L4DAT1	215
ADDR2	16	$\overline{\text{MS1}}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	L4DAT0	216
ADDR3	17	$\overline{\text{MS0}}$	57	GND	97	DATA31	137	DATA2	177	L4CLK	217
ADDR4	18	$\overline{\text{SW}}$	58	CLKIN	98	DATA30	138	DATA1	178	L4ACK	218
GND	19	$\overline{\text{BMS}}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{\text{DMAG2}}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{\text{DMAG1}}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	L0DAT3	182	L5DAT3	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	L0DAT2	183	L5DAT2	223
ADDR8	24	ADDR29	64	$\overline{\text{BR6}}$	104	V_{DD}	144	L0DAT1	184	L5DAT1	224
ADDR9	25	ADDR30	65	$\overline{\text{BR5}}$	105	DATA26	145	L0DAT0	185	L5DAT0	225
ADDR10	26	ADDR31	66	$\overline{\text{BR4}}$	106	DATA25	146	L0CLK	186	L5CLK	226
GND	27	GND	67	$\overline{\text{BR3}}$	107	DATA24	147	L0ACK	187	L5ACK	227
ADDR11	28	$\overline{\text{SBTS}}$	68	$\overline{\text{BR2}}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{\text{DMAR2}}$	69	$\overline{\text{BR1}}$	109	DATA23	149	L1DAT3	189	ID2	229
ADDR13	30	$\overline{\text{DMAR1}}$	70	GND	110	DATA22	150	L1DAT2	190	ID1	230
V_{DD}	31	$\overline{\text{HBR}}$	71	V_{DD}	111	DATA21	151	L1DAT1	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	L1DAT0	192	LBOOT	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	L1CLK	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	L1ACK	194	$\overline{\text{RESET}}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{\text{IRQ2}}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{\text{IRQ1}}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	L2DAT3	198	$\overline{\text{IRQ0}}$	238
V_{DD}	39	$\overline{\text{CPA}}$	79	DATA42	119	DATA15	159	L2DAT2	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	L2DAT1	200	TMS	240

OUTLINE DIMENSIONS

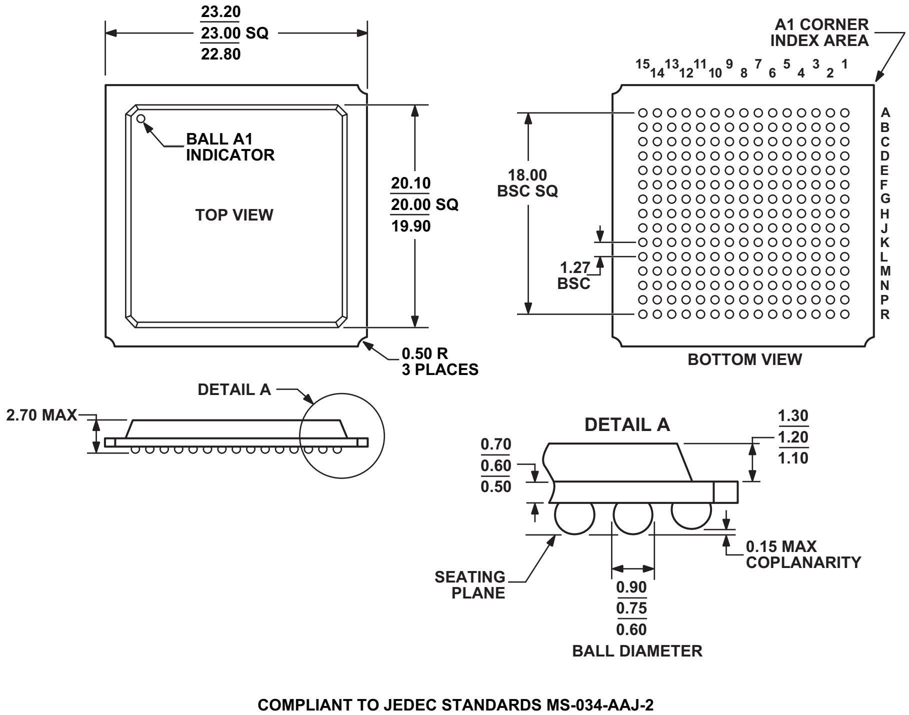

Figure 40. 225-Ball Plastic Ball Grid Array [PBGA]
(B-225-2)
Dimensions shown in millimeters

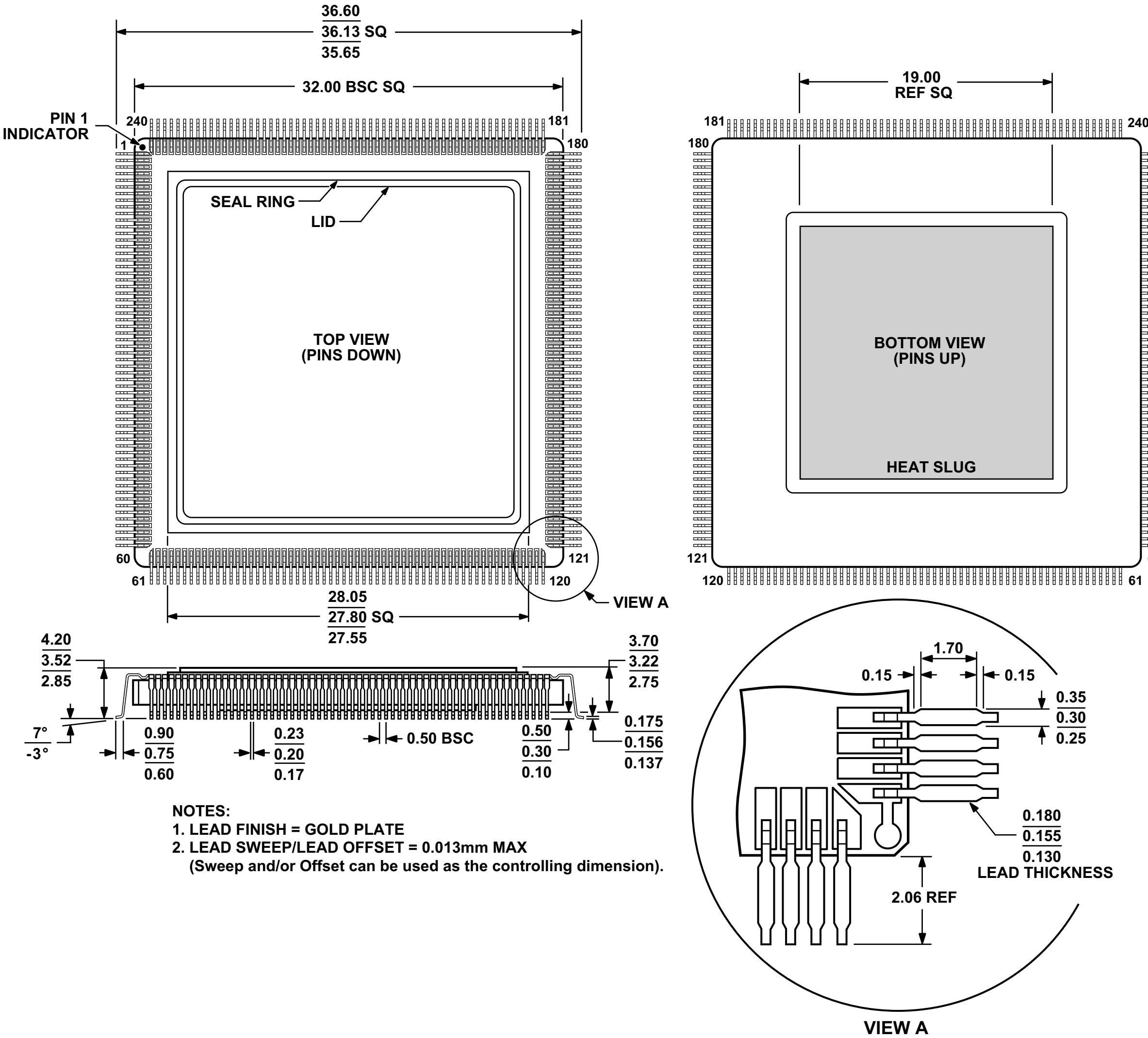

Figure 44. 240-Lead Ceramic Quad Flat Package, Heat Slug Down [CQFP]
(QS-240-1A)
Dimensions shown in millimeters