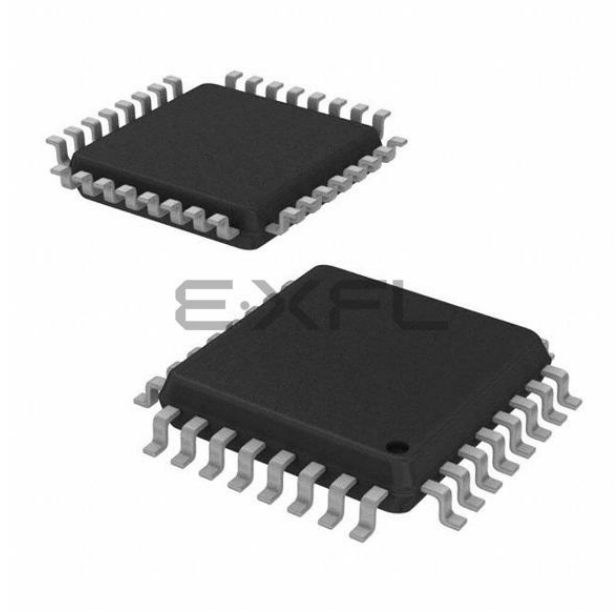

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	12KB (6K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8011vfae

1.7 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8013 or 56F8011. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-2 56F8013/56F8011 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F801X Peripheral Reference Manual	Detailed description of peripherals of the 56F801X family of devices	MC56F8000RM
56F801X Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F801x family of devices	56F801XBLUG
56F8013/56F8011 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8013
Errata	Details any chip issues that might be present	MC56F8013E MC56F8011E

1.8 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

2.2 56F8013/56F8011 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD}	26	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{SS}	13	Supply	Supply	**V_{SS}** — These pins provide ground for chip logic and I/O drivers.
V_{SS}	27			
V_{DDA}	8	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	9	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	25	Supply	Supply	**V_{CAP}** — Connect a 2.2 µF or greater bypass capacitor between this pin and VSS_IO, which is required by the internal voltage regulator for proper chip operation. See **Section 10.2.1**.
GPIOB6	1	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(RXD)		Input		**Receive Data** — SCI receive data input.
(SDA[1])		Input/ Output		**Serial Data** — This pin serves as the I^2C serial data line.
(CLKIN)		Input		**Clock Input** — This pin serves as an optional external clock input. After reset, the default state is GPIOB6. The alternative peripheral functionality is controlled via the SIM (See **Section 6.3.8**) and the CLKMODE bit of the OCCS Oscillator Control Register.

1. This signal is also brought out on the GPIOB1 pin.

Return to Table 2-2

Table 2-3 56F8013/56F8011 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB7	3	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TXD)		Output		**Transmit Data** — SCI transmit data output or transmit / receive in single wire operation.
(SCL[2])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB7. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
2. This signal is also brought out on the GPIOB0 pin.				
$\overline{\text{RESET}}$	15	Input	Input with internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks.
(GPIOA7)		Input/Open Drain Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOB4	19	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(T0)		Input/ Output		**T0** — Timer, Channel 0
(CLKO)		Output		**Clock Output** — This is a buffered clock signal. Using the SIM_CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled (logic 0), CLK_MSTR (system clock), IPBus clock, or oscillator output. See **Section 6.3.7**. After reset, the default state is GPIOB4. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.

Return to Table 2-2

3.5 Pin Descriptions

3.5.1 External Reference (GPIOB6 / RXD / SDA / CLKIN)

After reset, the internal relaxation oscillator is selected as the clock source for the chip. The user then has the option of switching to an external clock reference if desired by enabling the PRECS bit in the OCCS Oscillator Control register.

Part 4 Memory Map

4.1 Introduction

The 56F8013/56F8011 device is a 16-bit motor-control chip based on the 56800E core. It uses a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM is used in both spaces and Flash memory is used only in Program space.

This section provides memory maps for:

- Program Address Space, including the Interrupt Vector Table
- Data Address Space, including the EOnCE Memory and Peripheral Memory Maps

On-chip memory sizes for the device are summarized in **Table 4-1.** Flash memories' restrictions are identified in the "Use Restrictions" column of **Table 4-1.**

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8013	56F8011	Use Restrictions
Program Flash (PFLASH)	8k x 16	*6k x 16*	Erase / Program via Flash interface unit and word writes to CDBW
Unified RAM (ram)	2k x 16	*1k x 16*	Usable by both the Program and Data memory spaces

4.2 Interrupt Vector Table

Table 4-2 provides the 56F8013/56F8011's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts will be serviced before level 2, and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the Vector Base Address (VBA). Please see **Section 5.5.6** for the reset value of the VBA.

By default, VBA = 0, and the reset address and COP reset address will correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 4-2 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
Timer	38	0-2	P:$4C	Timer Channel 2
Timer	39	0-2	P:$4E	Timer Channel 3
ADC	40	0-2	P:$50	ADCA Conversion Complete
ADC	41	0-2	P:$52	ADCB Conversion Complete
ADC	42	0-2	P:$54	ADC Zero Crossing or Limit Error
PWM	43	0-2	P:$56	Reload PWM
PWM	44	0-2	P:$58	PWM Fault
SWILP	45	-1	P:$5A	SW Interrupt Low Priority

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to the reset value, the first two locations of the vector table will overlay the chip reset addresses.

4.3 Program Map

The Program Memory map is shown in **Table 4-3**.

Table 4-3 Program Memory Map for 56F8013[1]

Begin/End Address	Memory Allocation
P: $FF FFFF P: $00 8800	RESERVED
P: $00 87FF P: $00 8000	On-Chip RAM[2] 4KB
P: $00 7FFF P: $00 2000	RESERVED
P: $00 1FFF P: $00 0000	Internal Program Flash 16KB Cop Reset Address = $00 0002 Boot Location = $00 0000

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Data space starting at address X: $00 0000; see **Figure 4-1**.

Table 4-18 GPIOA Registers Address Map (GPIOA_BASE = $00 F100)

Register Acronym	Address Offset	Register Description
GPIOA_PUPEN	$0	Pull-up Enable Register
GPIOA_DATA	$1	Data Register
GPIOA_DDIR	$2	Data Direction Register
GPIOA_PEREN	$3	Peripheral Enable Register
GPIOA_IASSRT	$4	Interrupt Assert Register
GPIOA_IEN	$5	Interrupt Enable Register
GPIOA_IEPOL	$6	Interrupt Edge Polarity Register
GPIOA_IPEND	$7	Interrupt Pending Register
GPIOA_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOA_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOA_RDATA	$A	Raw Data Register
GPIOA_DRIVE	$B	Drive Strength Control Register

Table 4-19 GPIOB Registers Address Map (GPIOB_BASE = $00 F110)

Register Acronym	Address Offset	Register Description
GPIOB_PUPEN	$0	Pull-up Enable Register
GPIOB_DATA	$1	Data Register
GPIOB_DDIR	$2	Data Direction Register
GPIOB_PEREN	$3	Peripheral Enable Register
GPIOB_IASSRT	$4	Interrupt Assert Register
GPIOB_IEN	$5	Interrupt Enable Register
GPIOB_IEPOL	$6	Interrupt Edge Polarity Register
GPIOB_IPEND	$7	Interrupt Pending Register
GPIOB_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOB_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOB_RDATA	$A	Raw Data Register
GPIOB_DRIVE	$B	Drive Strength Control Register

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following table defines the nesting requirements for each priority level.

Table 5-1 Interrupt Mask Bit Definition

SR[9]	SR[8]	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes Fast Interrupts before the core does.

A Fast Interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIM*n* register to the appropriate vector number
3. Setting the FIVAL*n* and FIVAH*n* registers with the address of the code for the Fast Interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a Fast Interrupt. The ITCN takes the vector address from the appropriate FIVALn and FIVAHn registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector adddress and if it is not a JSR, the core starts its Fast Interrupt handling.

5.5.3.8 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	ADCA_CC IPL		TMR_3 IPL		TMR_2 IPL		TMR_1 IPL		TMR_0 IPL		I2C_ADDR IPL		0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.5.4.1 ADCA Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.4.2 Timer Channel 3 Interrupt Priority Level (TMR_3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.4.3 Timer Channel 2 Interrupt Priority Level (TMR_2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.5.8 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.5.8.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15—0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.5.9 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.5.9.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.5.9.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.5.10 Fast Interrupt 1 Match Register (FIM1)

Base + $9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1					
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-12 Fast Interrupt 1 Match Register (FIM1)

5.5.10.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.5.10.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 1. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast

6.2 Features

The SIM has the following features:

- Reset sequencing
- Core and peripheral clock control and distribution
- Stop/Wait mode control
- System status
- Power control
- Control I/O multiplexing
- System bus clocks with pipeline hold-off support
- System clocks for non-pipelined interfaces
- Peripheral clocks for Quad Timer and PWM with high-speed (3X) option
- Power-saving clock gating for peripherals
- Three power modes (Run, Wait, Stop) to control power utilization
  - Stop mode shuts down the 56800E core, system clock, and peripheral clock
  - Wait mode shuts down the 56800E core and unnecessary system clock operation
  - Run mode supports full part operation
- Controls, with write protection, the enable/disable of 56800E core WAIT and STOP instructions
- Controls, with write protection, the enable/disable of Large Regulator Standby mode
- Controls to route functional signals to selected peripherals and I/O pads
- Controls deassertion sequence of internal resets
- Software-initiated reset
- Four 16-bit registers reset only by a Power-On Reset usable for general-purpose software control
- Timer channel Stop mode clocking controls
- SCI Stop mode clocking control to support LIN Sleep mode stop recovery
- Short addressing location control
- Registers for containing the JTAG ID of the chip
- Controls output to CLKO pin

- 1 = Timer Channel 3 enabled in Stop mode

6.3.1.2 Timer Channel 2 Stop Disable (TC2_SD)—Bit 14

This bit enables the operation of the Timer Channel 2 peripheral clock in Stop mode.

- 0 = Timer Channel 2 disabled in Stop mode
- 1 = Timer Channel 2 enabled in Stop mode

6.3.1.3 Timer Channel 1 Stop Disable (TC1_SD)—Bit 13

This bit enables the operation of the Timer Channel 1 peripheral clock in Stop mode.

- 0 = Timer Channel 1 disabled in Stop mode
- 1 = Timer Channel 1 enabled in Stop mode

6.3.1.4 Timer Channel 0 Stop Disable (TC0_SD)—Bit 12

This bit enables the operation of the Timer Channel 0 peripheral clock in Stop mode.

- 0 = Timer Channel 0 disabled in Stop mode
- 1 = Timer Channel 0 enabled in Stop mode

6.3.1.5 SCI Stop Disable (SCI_SD)—Bit 11

This bit enables the operation of the SCI peripheral clock in Stop mode. This is recommended for use in LIN mode so that the SCI can generate interrupts and recover from Stop mode while the LIN interface is in Sleep mode and using Stop mode to reduce power consumption.

- 0 = SCI disabled in Stop mode
- 1 = SCI enabled in Stop mode

6.3.1.6 Reserved—Bit 10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.1.7 Timer Channel 3 Input (TC3_INP)—Bit 9

This bit selects the input of Timer Channel 3 to be from the PWM Sync signal or GPIO pin.

- 1 = Timer Channel 3 Input from PWM sync signal
- 0 = Timer Channel 3 Input controlled by SIM_GPS register CFG_B3 and CFG_A5 fields

6.3.1.8 Reserved—Bits 8–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.1.9 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.3.1.10 Software Reset (SWRST)—Bit 4

Writing 1 to this field will cause the part to reset.

- 01001 = Reserved for factory test—OCCS MSTR OSC clock
- 01011 = Reserved for factory test—ADC clock
- 01100 = Reserved for factory test—JTAG TCLK
- 01101 = Reserved for factory test—Continuous peripheral clock
- 01110 = Reserved for factory test—Continuous inverted peripheral clock
- 01111 = Reserved for factory test—Continuous high-speed peripheral clock

6.3.8 SIM GPIO Peripheral Select Register (SIM_GPS)

All of the peripheral pins on the 56F8013/56F8011 share their Input/Output (I/O) with GPIO ports. To select peripheral or GPIO control, program corresponding bit in the GPIOx_PEREN register in GPIO module. See the 56F801x Peripheral Reference Manual for detail. In some cases, there are two possible peripherals as well as the GPIO functionality available for control of the I/O. In these cases, the SIM_GPS register is used to determine which peripheral has control when the corresponding I/O pin is configured in peripheral mode.

As shown in **Figure 6-9**, the GPIO Peripheral Enable Register (PEREN) has the final control over which pin controls the I/O. SIM_GPS simply decides which peripheral will be routed to the I/O when PEREN = 1.

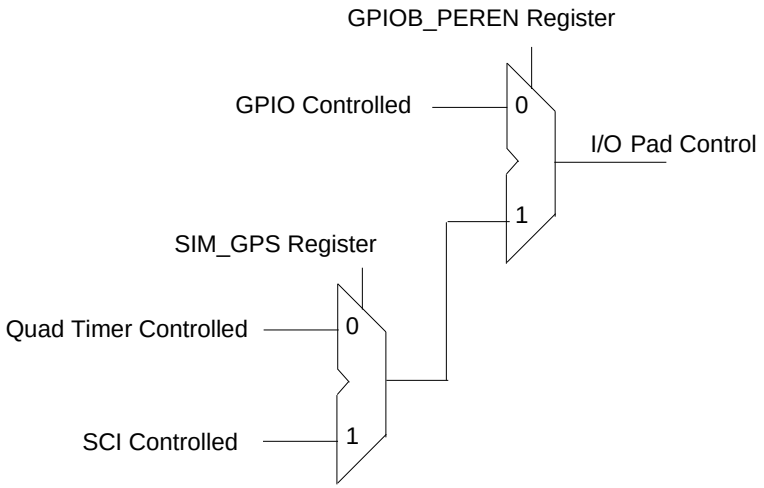

Figure 6-9 Overall Control of Pads Using SIM_GPS Control

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TCR	PCR	0	0	CFG_B7	CFG_B6	CFG_B5	CFG_B4	CFG_B3	CFG_B2	CFG_B1	CFG_B0	CFG_A5		CFG_A4	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-10 GPIO Peripheral Select Register (SIM_GPS)

6.3.8.1 Quad Timer Clock Rate (TCR)—Bit 15

This bit selects the clock speed for the Quad Timermodule.

- 0 = Quad Timer module clock rate equals system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer module clock rate equals three times system clock rate, to a maximum 96MHz

Note: This bit should only be changed while the TMR module's clock is disabled. See **Section 6.3.9**.

Note: High-speed clocking is only available when the PLL is being used.

Note: If the PWM sync signal pulse is used as input to Timer 3 (See SIM_CTRL: TC3_INP, **Section 6.3.1.7**), then the clocks of the Quad Timer and PWM must be related, as shown in **Table 6-2**.

6.3.8.2 PWM Clock Rate (PCR)—Bit 14

This bit selects the clock speed for the PWM module.

- 0 = PWM module clock rate equals system clock rate, to a maximum 32MHz (default)
- 1 = PWM module clock rate equals three times system clock rate, to a maximum 96MHz

Note: This bit should only be changed while the PWM module's clock is disabled. See **Section 6.3.9**.

Note: High-speed clocking is only available when the PLL is being used.

Note: If the PWM sync signal is used as input to Timer 3 (See SIM_CTRL: TC3_INP, **Section 6.3.1.7**), then the clocks of the Quad Timer and PWM must be related, as shown in **Table 6-2**.

Table 6-2 Allowable Quad Timer and PWM Clock Rates when Using PWM Reload Pulse

		Quad Timer	
Clock Speed		1X	3X
PWM	1X	OK	OK
	3X	NO	OK

6.3.8.3 Reserved—Bits 13–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.3.8.4 Configure GPIOB7 (CFG_B7)—Bit 11

This bit selects the alternate function for GPIOB7.

- 0 = TXD — SCI Transmit Data (default)
- 1 = SCL — I2C Serial Clock

6.3.8.5 Configure GPIOB6 (CFG_B6)—Bit 10

This bit selects the alternate function for GPIOB6.

All peripherals, except the COP/watchdog timer, run at the system clock (peripheral bus) frequency[1], which is the same as the main processor frequency in this architecture. The COP timer runs at MSTR_OSC / 1024. The maximum frequency of operation is SYS_CLK = 32MHz. The only exception is the Quad Timer and PWM, which can be configured to operate at three times the system bus rate using TCR and PCR controls, provided the PLL is active and selected.

6.6 Resets

The SIM supports four sources of reset, as shown in **Figure 6-15**. The two asynchronous sources are the external reset pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing the SIM_CTRL register in **Section 6.3.1**, and the COP reset. The SIM uses these to generate resets for the internal logic. These are outlined in **Table 6-4**. The first column lists the four primary resets which are calculated. The JTAG circuitry is reset by the Power-On Reset. Columns two through five indicate which reset sources trigger these reset signals. The last column provides additional detail.

Table 6-4 Primary System Resets

	Reset Sources				
Reset Signal	**POR**	**External**	**Software**	**COP**	**Comments**
EXTENDED_POR	X				Stretched version of $\overline{\text{POR}}$. Relevant 64 Relaxation Oscillator Clock cycles after $\overline{\text{POR}}$ deasserts.
CLKGEN_RST	X	X	X	X	Released 32 Relaxation Oscillator Clock cycles after all reset sources have released.
PERIP_RST	X	X	X	X	Releases 32 Relaxation Oscillator Clock cycles after the CLKGEN_$\overline{\text{RST}}$ is released.
CORE_RST	X	X	X	X	Releases 32 SYS_CLK periods after PERIP_$\overline{\text{RST}}$ is released.

Figure 6-15 provides a graphic illustration of the details in **Table 6-4**. Note that the POR_Delay blocks use the Relaxation Oscillator Clock as their time base since other system clocks are inactive during this phase of reset.

1. The Quad Timer and PWM modules can be operated at three times the IPBus clock frequency.

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOB_PUPEN	R	0	0	0	0	0	0	0	0	PU							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOB_DATA	R	0	0	0	0	0	0	0	0	D							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$2	GPIOB_DDIR	R	0	0	0	0	0	0	0	0	DD							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOB_PEREN	R	0	0	0	0	0	0	0	0	PE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$4	GPIOB_IASSRT	R	0	0	0	0	0	0	0	0	IA							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOB_IEN	R	0	0	0	0	0	0	0	0	IEN							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOB_IEPOL	R	0	0	0	0	0	0	0	0	IEPOL							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOB_IPEND	R	0	0	0	0	0	0	0	0	IPR							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOB_IEDGE	R	0	0	0	0	0	0	0	0	IES							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOB_PPOUTM	R	0	0	0	0	0	0	0	0	OEN							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOB_RDATA	R	0	0	0	0	0	0	0	0	RAW DATA							
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOB_DRIVE	R	0	0	0	0	0	0	0	0	DRIVE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-2 GPIOB Register Map Summary

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOC_PUPEN	R	0	0	0	0	0	0	0	0	PU							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOC_DATA	R	0	0	0	0	0	0	0	0	D							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOC_DDIR	R	0	0	0	0	0	0	0	0	DD							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOC_PEREN	R	0	0	0	0	0	0	0	0	PE							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$4	GPIOC_IASSRT	R	0	0	0	0	0	0	0	0	IA							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOC_IEN	R	0	0	0	0	0	0	0	0	IEN							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOC_IEPOL	R	0	0	0	0	0	0	0	0	IEPOL							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOC_IPEND	R	0	0	0	0	0	0	0	0	IPR							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOC_IEDGE	R	0	0	0	0	0	0	0	0	IES							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOC_PPOUTM	R	0	0	0	0	0	0	0	0	OEN							
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOC_RDATA	R	0	0	0	0	0	0	0	0	RAW DATA							
		W																
		RS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
$B	GPIOC_DRIVE	R	0	0	0	0	0	0	0	0	DRIVE							
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-3 GPIOC Register Map Summary

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 10-1 Absolute Maximum Ratings

(V_{SS} = 0V, V_{SSA} = 0V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		- 0.3	4.0	V
ADC High Voltage Reference	V_{REFH}		- 0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		- 0.3	0.3	V
Input Voltage Range (Digital inputs)	V_{IN}	Pin Groups 1, 2	- 0.3	6.0	V
Input Voltage Range (ADC inputs)[1]	V_{INA}	Pin Group 3	- 0.3	4.0	V
Input clamp current, per pin (V_{IN} < 0)[2]	V_{IC}		-	-20	mA
Output clamp current, per pin (V_O < 0)[2]	V_{OC}		-	-20	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	-0.3	4.0	V
Output Voltage Range (Open Drain mode)	V_{OUTOD}	Pin Groups 1, 2	-0.3	6.0	V
Ambient Temperature (Automotive)	T_A		-40	125	°C
Ambient Temperature (Industrial)	T_A		-40	105	°C
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. Pin Group 3 can tolerate 6V for less than 5 seconds when they are configured as ADC inputs or during reset. Pin Group 3 can tolerate 6V if they are configured as GPIO.
2. Continuous input current per pin is -2 mA

Table 10-4 Recommended Operating Conditions

(V_{REFL} = 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3	3.3	3.6	V
ADC Supply voltage	V_{DDA}		3	3.3	3.6	V
ADC High Voltage Reference	V_{REFH}		3	—	V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 8 0	—	 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2	—	5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3	—	0.8	V
Output Source Current High (at V_{OH} min.) When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —	 — —	 -4 -8	mA
Output Source Current Low (at V_{OL} max.) When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —	 — —	 4 8	mA
Ambient Operating Temperature (Automotive)	T_A		-40	—	125	°C
Ambient Operating Temperature (Industrial)	T_A		-40	—	105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 105°C	10,000	—	—	Cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15	—	—	Years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	Years

Note: Total chip source or sink current cannot exceed 50mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC analog inputs

5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.
7. For device S56F8013MFA00E, input leakage current is ± 1μA.
8. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC.

10.15 Equivalent Circuit for ADC Inputs

Figure 10-17 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}\text{-}V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}\text{-}V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase.

One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.